Preliminary Datasheet AV6302

Wireless Audio Receiver

General Description

The AV6301 / 6302 chipset is optimized for building wireless gaming headsets and point to multi-point audio distribution solutions such as rear speakers and subwoofers in home theater systems.The chipset is comprised of two ICs: AV6301 (sender) and AV6302 (client). These devices share the VMI RF Protocol and may be mixed and matched with other VMI chips (AV6200 / AV6201 / AV6202).

The AV63xx family expands the capabilities of Avnera's world-class VMI wireless audio protocol by providing increased signal routing flexibility to accommodate a wide range of gaming headset applications. The AV6301 / 02 chipset achieves the goal of enabling a single core design to service multiple game platforms (PC or Console), External Digital Signal Processing (DSP) is also easily supported for all gaming platforms.

The chip set provides all functions necessary to complete a bidirectional wireless audio link with high quality voice and music performance. Operation in the worldwide 2.4 GHz spectrum addresses the need for global application.

System / Chipset Features

- ✓ Stereo audio path: >93 dB SNR, 20 kHz BW
- ✓ Mono voice path: >70 dB SNR, 6.5 kHz voice BW with on chip MIC path (>93 dB SNR with external 16 ADC)
- ✓ Over-the-air (OTA) serial interface: >2 kbps, bi-directional, full duplex
- ✓ Advanced forward error correction coding, error detection, and audio-specific error concealment
- ✓ Diversity antenna support
- ✓ Low and Fixed Latency: <16 ms,
- ✓ Long Range: 15m (non-line-of-site)
- ✓ Auto search/sync/standby/wake-up/shutdown
- ✓ All Voltage Regulators on-chip
- ✓ Interoperability with AV6200 and AV6201

AV6302

The core functionality of the AV6302 is identical to that of the AV6301 and it integrates all of the same functions. To minimize external Bill of Materials (BOM) for a complete headset client the AV6302 integrates additional analog functions. SPI and TWI interfaces are retained as well as a full USB transceiver. Enumeration as a high current device during charging as well as simplified field update of firmware on the Headset is enabled.

A complete battery charging system is added to the significant power management functions already on chip. The battery charger includes a temperature monitor and is compliant with Lithium Ion and Lithium polymer battery types.

An Integrated high quality audio CODEC directly drives on-chip low impedance headphone amplifiers and interfaces to electret and condenser microphone transducers. On-chip audio DSP, for both the stereo forward audio path and mono microphone path, performs fully programmable functions including gain control, equalization and compression, providing the headset designer with the essential tools to create custom voicing across Headset models or applications.

18 General purpose I/O ports are available, including support for LEDs and Encoders. In addition, a 3 channel general purpose ADC is provided that can support up to 2 potentiometers.

A unique feature of the AV6302 Client chip is its ability to accept I2S input in addition to Microphone input for advanced routing of Chat and Microphone signals. Advanced audio routing options include the ability to utilize the microphone preamp, gain control and DSP before outputting the signal to an I2S out. This is a key feature when interfacing to XBOX controller radios.

AV6302 Features

- ✓ On Chip Audio Codec includes Data-Converters, microphone amplifier and headphone amplifiers
- ✓ Audio DSP: EQ, gain control, mix-back, muting
- ✓ Complete Battery Charging System
- ✓ USB HID interface for USB compliant charging and firmware update
- ✓ Noise Gates on Mic and Chat paths
- ✓ 18 General Purpose I/O pins with support for:
  - ✓ Master and Slave SPI and TWI interfaces
  - ✓ 3 PWM outputs
  - ✓ 2 Rotary Encoder Inputs
  - ✓ 1 Stereo I2s Out
  - ✓ 1 mono I2S In
  - ✓ 1 mono I2S Out
- ✓ 3 Channel General Purpose ADC
  - ✓ 3 Dedicated Analog inputs
  - ✓ Supports 2 potentiometers - game and chat levels

Applications

PC Game Wireless Headset

Game Console Wireless Headset

I2S based Wireless Audio

Wireless Rear Speakers

Wireless Subwoofer

Packaging

The AV6302 is available in an 8 x 8 mm, 56 pin QFN package and is rated for operation over the commercial temperature range (0 to 70 degrees C)

Revision History

Revision	Change Summary	Release Date
0.1	Preliminary release of datasheet	9/29/11
0.2	Audio Routing Diagram Update. Package Drawing Update. Pin Description minor updates. Add Selector Grid	10/28/11
0.3	Update Selector Grid, Update to Front page general description and Features.	11/4/11

Table of Contents

General Description 1
System / Chipset Features 1
AV6302 1
AV6302 Features 2
Applications 2
Packaging 2
Revision History 3
Table 0-1 AV6xxx Selection Grid 5
1 REFERENCE DIAGRAMS 6
1.1 Wireless Headset Solution 6
1.2 Functional Diagram 7
1.3 Audio Signal Routing Diagram 7
1.4 Application Circuit - Universal Wireless Gaming Headset 8
2 PIN INFORMATION 9
2.1 Pin Diagram 9
2.2 PIN DESCRIPTION 10
3 ELECTRICAL SPECIFICATIONS 12
3.1 Absolute Maximum Ratings 12
3.2 DC Electrical Characteristics 13
3.3 Electrical Characteristics – Voltage Supervisory Circuit 13
3.4 Electrical Characteristics – RF Receiver 14
3.5 Electrical Characteristics – RF Transmitter 14
3.6 Electrical Characteristics – End-to-end Audio Characteristics 15
3.7 Electrical Characteristics – Audio DAC and Headphone Amp 15
3.8 Electrical Characteristics – MIC pre-amp and Voice ADC 16
3.9 Electrical Characteristics – Battery Charger 16
4 PACKAGE INFORMATION 17
4.1 Package Drawing and Details 17
4.2 Package Marking 18
5 CONTACT INFO & LEGAL DISCLAIMER 19

List of Tables

Table 0-1 AV6xxx Selection Grid 5
Table 2-1 AV6302 Pin Description 10
Table 3-1 AV6302 Absolute Maximum Ratings 12
Table 3-2 AV6302 DC Electrical Characteristics 13
Table 3-3 AV6302 Electrical Characteristics - Voltage Supervisory 13
Table 3-4 AV6302 Electrical Characteristics - RF Receiver 14
Table 3-5 AV6302 Electrical Characteristics - RF Transmitter 14
Table 3-6 AV6302 Electrical Characteristics – End-to-end Audio Characteristics 15
Table 3-7 AV6302 Electrical Characteristics - Audio DAC and Headphone Amp 15
Table 3-8 AV6302 Electrical Characteristics - MIC pre-amp and Voice ADC 16
Table 3-9 AV6302 Electrical Characteristics - Battery Charger 16

List of Figures

Figure 1-1 AV6302 Universal Gaming Headset 6
Figure 1-2 AV6302 Block Diagram 7
Figure 1-3 AV6302 Audio Routing Diagram 7
Figure 1-4 AV6302 Application Circuit 8
Figure 2-1 AV6302 Pin Diagram 9
Figure 4-1 56 pin QFN Mechanical Drawing 17
Figure 4-2 Package Marking Layout 18

Table 0-1 AV6xxx Selection Grid

Part Number	AV6200	AV6201	AV6301	AV6200	AV6202	AV6302
Role	**Sender**			**Receiver**		
I2S IN	Yes	No	Yes	Yes	No	Yes
I2S Out	Yes	No	Yes	Yes	Yes	Yes
USB Port	No	Audio / HID	Audio / HID	No	HID	HID
MIC Amp	No	No	No	No	Yes	Yes
Headphone Driver Amp	No	No	No	No	Yes	Yes
Battery Charger	No	No	No	No	Yes	Yes
General Purpose ADCs	0	0	0	0	0	3
Button Support	Yes	Yes	Yes	Yes	Yes	Yes
Rotary Encoder Support	No	No	No	No	Yes	Yes
LED Support	Yes	Yes	Yes	Yes	Yes	Yes
I2S Loop-Back (external DSP)	No	No	Yes	No	No	No
MIC path input to I2S out	N/A	N/A	N/A	N/A	No	Yes
MIC Side-tone Mix	N/A	N/A	N/A	N/A	Yes	Yes
Game / Chat Mix on TX	N/A	No	Yes	N/A	N/A	N/A
Game / Chat Mix at RX	N/A	N/A	N/A	No	No	Yes

1 REFERENCE DIAGRAMS

1.1 Wireless Headset Solution

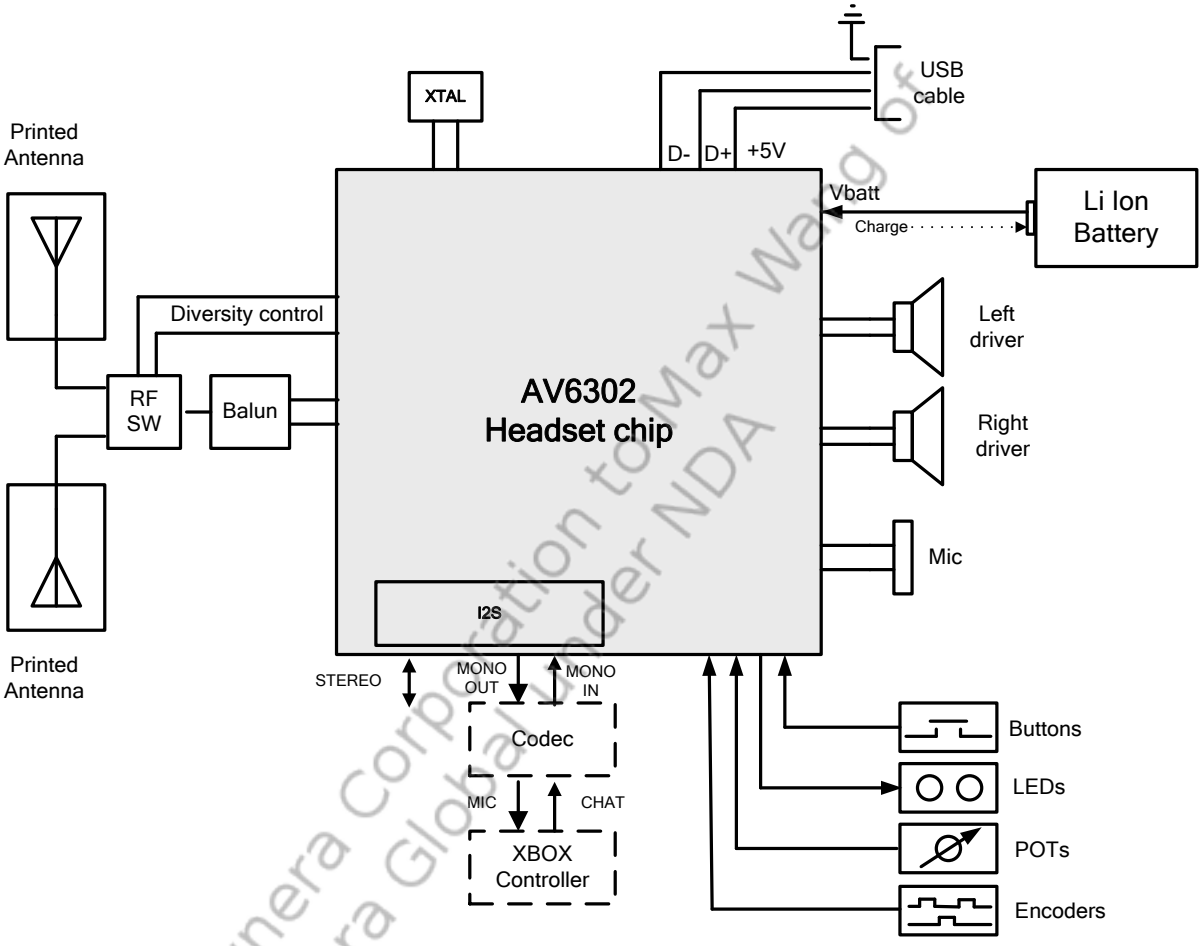


Figure 1-1 AV6302 Universal Gaming Headset

1.2 Functional Diagram

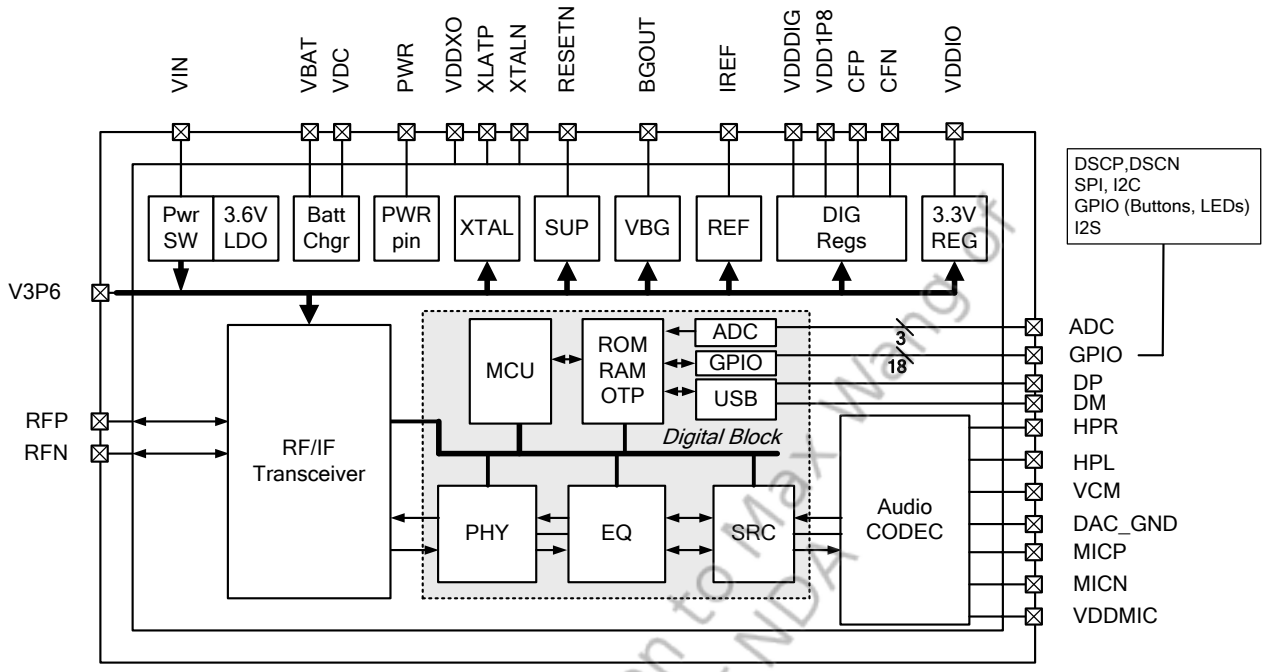


Figure 1-2 AV6302 Block Diagram

1.3 Audio Signal Routing Diagram

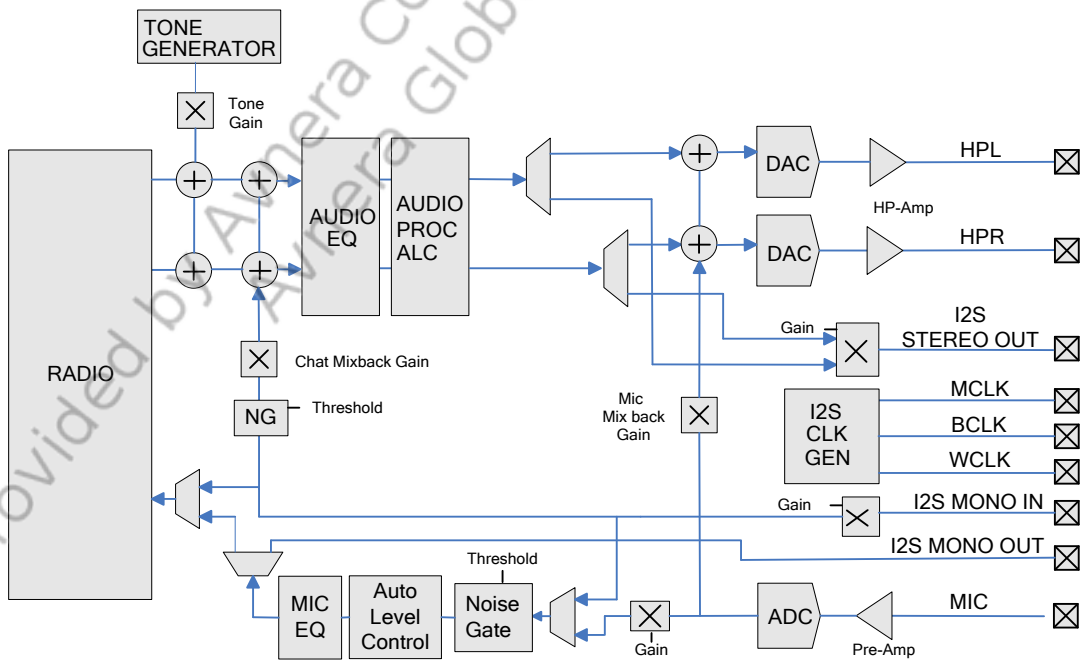


Figure 1-3 AV6302 Audio Routing Diagram

1.4 Application Circuit - Universal Wireless Gaming Headset

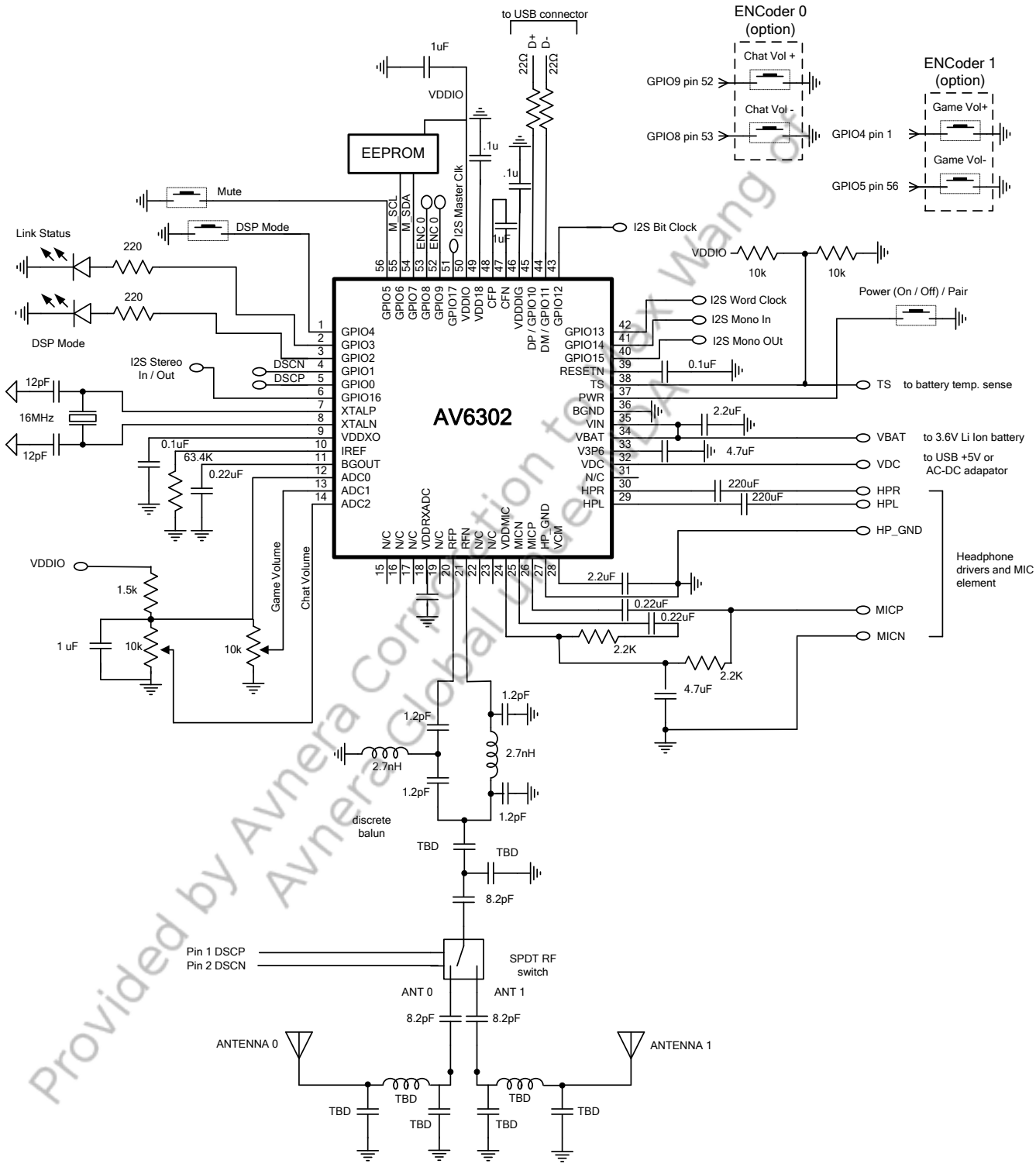


Figure 1-4 AV6302 Application Circuit

2 PIN INFORMATION

2.1 Pin Diagram

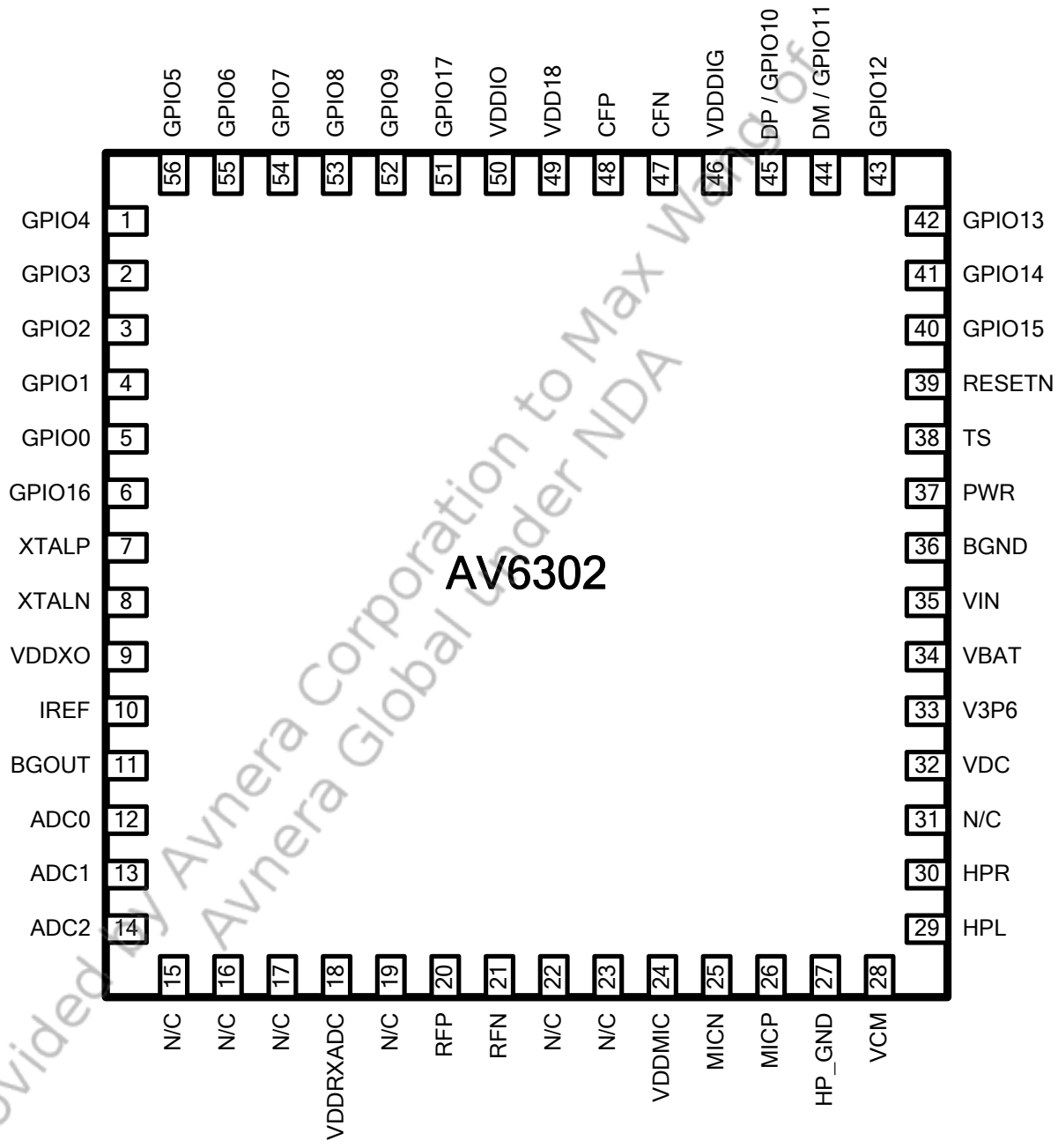


Figure 2-1 AV6302 Pin Diagram

2.2 PIN DESCRIPTION

Table 2-1 AV6302 Pin Description

Pin No.	Symbol	Pin Type	Description
1	GPIO4 S_MOSI (SPI Slave) S_SDA (TWI Slave) ENC1A	Digital I/O	GPIO port 4; usage is programmable to GPIO OR to S_MOSI OR to S_SDA OR to Encoder resource # 1 (A)
2	GPIO3 S_SCLK (SPI Slave) UART_RX PWM1	Digital I/O	GPIO port 3; usage is programmable to GPIO OR to S_SCLK OR to UART Receiver OR to PWM resource # 1
3	GPIO2 S_SSB (SPI Slave) UART_TX PWM0	Digital I/O	GPIO port 2; usage is programmable to GPIO OR to S_SSB OR to The UART Transmitter OR to PWM resource # 0
4	GPIO1 DSCN PA_EN	Digital Output	GPIO port 1; Usage is programmable to GPIO OR to Diversity Switch – OR to Power Amp Enable
5	GPIO0 DSCP DSC	Digital Output	GPIO port 0; Usage is programmable to GPIO OR to Diversity Switch + OR to DSC
6	GPIO16 I2S STEREO OUT CEN PWM2	Digital Output	GPIO port 16; Usage is programmable to GPIO OR to I2S port 0 Stereo Out OR to CEN OR to PWM resource #2
7	XTALP	Analog input	External crystal input
8	XTALN	Analog input	External crystal input
9	VDDXO	Analog	Crystal oscillator regulator bypass pin
10	IREF	Analog pin	Reference current setting resistor connection
11	BGOUT	Analog bypass	Bandgap reference bypass and resistor pin
12	ADC0	Analog Input	Muxed ADC port 0
13	ADC1	Analog Input	Muxed ADC port 1
14	ADC2	Analog Input	Muxed ADC port 2
15-17, 19, 22-23, 31, 51	N/C	-	No connection – Do Not Ground
18	VDDRXADC	Bypass	Bypass pin for Receiver IF Data Converter
20	RFP	RF I/O	RF input/output positive
21	RFN	RF I/O	RF input/output negative
24	VDDMIC	Analog bypass	Microphone supply voltage bypass
25	MICN	Analog input	Microphone pre-amp negative input
26	MICP	Analog input	Microphone pre-amp positive input
27	HP_GND	Analog ground	Headphone ground
28	VCM	Analog bypass	Headphone/DAC common mode bypass pin
29	HPL	Analog output	Headphone left
30	HPR	Analog output	Headphone right
32	VDC	Supply pin	5V input supply voltage from +5V AC/DC adaptor
33	V3P6	Bypass	Bypass pin for 3.6V main regulator
34	VBAT	Bypass	Li Ion battery or regulator output connection
35	VIN	Analog	Input voltage for the chip
36	BGND		Connect directly to Ground
37	PWR	Digital input	Power on/off pin
38	TS	Analog input	Temperature sense for battery charger
39	RESETN	Digital input	RESET signal; active low; 3.3V CMOS I/O
40	GPIO15	Digital I/O	GPIO port 15; usage is programmable to GPIO OR to

Pin No.	Symbol	Pin Type	Description
	I2S MONO OUT ENC1B PWM2		I2S Port 1 Mono Out Data OR to Encoder resource #1 (B) OR to PWM resource # 2
41	GPIO14 I2S MONO IN ENC1A PWM0	Digital I/O	GPIO port 14; usage is programmable to GPIO OR to I2S Port 2 Mono In Data OR to Encoder resource #1 (A) OR to PWM resource # 0
42	GPIO13 WCLK ENC0B PWM2	Digital I/O	GPIO port 12; usage is programmable to GPIO OR to I2S Word Clock OR to Encoder resource #0 (B) OR to PWM resource #2
43	GPIO12 BCLK ENC0A PWM1	Digital I/O	GPIO port 12; usage is programmable to GPIO OR to I2S Bit Clock OR to Encoder resource #0 (A) OR to PWM resource #1
44	DM	Digital I/O	USB minus i/O
45	DP	Digital I/O	USB plus I/O
46	VDDDIG	Bypass	Bypass pin for 1.35V digital core regulator
47	CFN	Analog	Switching regulator capacitor positive
48	CFP	Analog	Switching regulator capacitor negative
49	VDD18	Bypass	Bypass pin for 1.8V digital regulator (LDO)
50	VDDIO	Bypass	Bypass pin for 3.3V digital I/O regulator
51	GPIO17 MCLK PWM1 PWM2	Digital I/O	GPIO port 17; usage is programmable to GPIO or to I2S Master Clock OR to PWM resource #1 OR to PWM resource #2
52	GPIO9 M_SSB (SPI Master) ENC0B MICIN	Digital I/O	GPIO port 9; usage is programmable to GPIO or to M-SSB OR to Encoder resource # 0 (B) OR to Digital Microphone Signal Input
53	GPIO8 M_SCLK (SPI Master) ENC0A MICCLK	Digital I/O	GPIO port 8; usage is programmable to GPIO OR to M_SCLK OR to Encoder resource # 0 (A) OR to Digital Microphone Clock Input
54	GPIO7 M_MOSI (SPI Master) M_SDA (TWI Master) SDA (TWI)	Digital I/O	GPIO port 7; usage is programmable to GPIO OR to M-MOSI OR to M_SDA OR to SDA
55	GPIO6 M_MISO (SPI Master) M_SCL (TWI Master) SCL (TWI)	Digital I/O	GPIO port 6; usage is programmable to GPIO OR to M_MISO OR to M_SCL OR to SCL
56	GPIO5 S_MISO (SPI Slave) S_SCL (TWI Slave) ENC1B	Digital I/O	GPIO port 5; usage is programmable to GPIO OR to S_MISO OR to S_SCL OR to Encoder resource # 1 (B)

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

The Absolute Maximum Rating (AMR) corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown). Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

Table 3-1 AV6302 Absolute Maximum Ratings

CONDITION	MIN	MAX	Units
Supply (relative to AGND and DGND)			
VDC	-0.3	6.0	V
VIN, VBAT	-0.3	4.5	V
Input Voltage Range – Digital Inputs	-0.3	3.6	V
Input Voltage Range – Analog Inputs	-0.3	3.6	V
Short circuit to GND (any pin)	--	continuous	
Operating Temperature	-40	+85	ºC
Storage Temperature	-40	+100	ºC
Lead Temperature (10s)	--	+300	ºC
Static Discharge Voltage – HBM (All pins)	3000		V
Static Discharge Voltage – MM	300		V

Note:

1) HBM = ESD Human Body Model; C = 100pF, R = 1kΩ
2) MM = ESD Machine Model; C = 100pF; R = 300Ω

3.2 DC Electrical Characteristics

Operating Conditions: VDC = 4.4V to 5.5V or VIN = 3.2V to 4.3V, VDDIO = 3.3V, T_A = 0ºC to +70 ºC; Typical specifications at T_A = 25ºC, VDC = 5.0V or VIN=3.6V.

Table 3-2 AV6302 DC Electrical Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDC Supply Voltage Input		4.4	5.0	5.5	V
VIN Supply Voltage Range		3.2	3.6	4.3	V
VBAT Voltage Input Range		0		4.3	V
V3P6	Internally regulated voltage		3.6		V
VDDIO (Digital 3.3V I/O) Reg. Voltage	Internally regulated voltage		3.3		V
VDDDIG (Digital Core) Reg. Voltage	Internally regulated voltage		1.35		V
VDD1P8	Internally regulated voltage		1.8		V
Supply Current (I_{VIN})	Shutdown Mode (PWR pin active)		25	50	uA
	Client Sleep Mode		1.2		uA
	Client No audio (header only) Link mode		16	19	mA
	Client Std. Headset Link Mode		46	55	mA
CMOS I/O Logic Levels – 3.3V I/O					
Input Voltage Logic Low, V_{IL}	V_{VDDIO} = 3.3V			0.8	V
Input Voltage Logic High, V_{IH}	V_{VDDIO} = 3.3V	2.0			V
Output Voltage Logic Low, V_{OL}	V_{VDDIO} = 3.3V ; I_{LOAD}=1mA			0.4	V
Output Voltage Logic High, V_{OH}	V_{VDDIO} = 3.3V; I_{LOAD}=1mA	2.9			V
PWR pin – headset chip					
Low threshold				0.6	V
High threshold		1.2			V
PWR pin current source			4		uA
GPIO Pin source current				3.0	mA

3.3 Electrical Characteristics – Voltage Supervisory Circuit

Operating Conditions: VDC = 4.4V to 5.5V or VIN = 3.2V to 4.3V, VDDIO = 3.3V, TA = 0ºC to +70 ºC; Typical specifications at TA = 25ºC, VDC = 5.0V or VIN = 3.6V.

Table 3-3 AV6302 Electrical Characteristics - Voltage Supervisory

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Monitor Low Thres. (assert reset)	Monitoring the voltage on V3P6		2.7		V
Voltage Monitor High Thres. (de-assert reset)	Monitoring the voltage on V3P6		3.0		V
Brownout bandwidth	Monitoring the voltage on V3P6		100		kHz
Reset Threshold (assert)			2.2		V
Reset Threshold (de-assert)			1.2		V
RESETN Minimum Time	0.1uF external capacitor		11		ms
VDC_OK threshold	Rising falling		4.1 3.9		V V

3.4 Electrical Characteristics – RF Receiver

Operating Conditions: VDC = 4.4V to 5.5V, VDDIO = 3.3V, T_A = 0ºC to +70 ºC; RF Channel Freq = 2403.35-2477.35MHz, measured at the single-ended input of the RF balun (with external impedance matching). Typical specifications at T_A = 25ºC, VDC = 5.0V or VIN=3.6V.

Table 3-4 AV6302 Electrical Characteristics - RF Receiver

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RF Channel Frequency Range	LO frequency (driving the mixers) RF carrier frequency	2402 2403.35		2478 2479.35	MHz MHz
Modulated Signal Offset from LO			1.35		MHz
Sensitivity (Note 1)	T_A=25ºC, LNA = High gain mode; max IF gain	-86	-89		dBm
Max input signal (desired signal) (Note 1)	T_A=25ºC, LNA = low gain mode; min IF gain		-5		dBm
Input Blocker Level – High Gain mode	> 2MHz offset		-45		dBm
Out-of-band blocker level	<2400 MHz; >2483.5 MHz		TBD		dBm
Spurious RF outputs	<2400 MHz >2483.5 MHz		-75 -75		dBm dBm

Note 1: Sensitivity and max signal level are defined as the onset of 0.2% BLER Block Error Rate.

3.5 Electrical Characteristics – RF Transmitter

Operating Conditions: VDC = 4.4V to 5.5V, VDDIO = 3.3V, T_A = 0ºC to +70 ºC; RF Channel Freq = 2403.35-2477.35MHz, measured at the single-ended input of the RF balun (with external impedance matching). Typical specifications at T_A = 25ºC, VDC = 5.0V or VIN=3.6V.

Table 3-5 AV6302 Electrical Characteristics - RF Transmitter

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RF Channel Frequency Range	LO frequency (driving the mixers) RF carrier frequency	2402 2403.35		2478 2479.35	MHz MHz
Modulated Signal Offset from LO			1.35		MHz
Modulated Signal Bandwidth	-10dB point		1.8		MHz
Output Power	Pi/4 DQPSK modulated signal ACPR: Adj $\leq$ -23dBc, Alt $\leq$ -30dBc		+2		dBm
Output harmonics	2nd harmonic, P_{out} = 0dBm 3rd harmonic, P_{out} = 0dBm		-52 -50		dBm dBm
Out-of-band Spurious Output	RF < 2390MHz, > 2483.5MHz, 1MHz RBW		<-62		dBm
Output Noise Floor	RF < 2390MHz, > 2483.5MHz, 1MHz RBW		<-62		dBm

3.6 Electrical Characteristics – End-to-end Audio Characteristics

Operating Conditions: VDC = 4.4V to 5.5V or VIN = 3.2V to 4.3V, VDDIO = 3.3V, TA = 0ºC to +70 ºC; Typical specifications at TA = 25ºC, VDC = 5.0V or VIN=3.6V.

Table 3-6 AV6302 Electrical Characteristics – End-to-end Audio Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SNR	Headset Mode – Forward stereo path		96		dB
	Headset Mode – Reverse mono path		68		dB
Audio Bandwidth	End-to-end audio BW; 0.1dB point		20		kHz
Voice Bandwidth	End-to-end audio BW; 0.1dB point		6.5		kHz
Audio Latency	AV6301 USB to AV6202 analog output AV6301 to AV6302 I2S output		<16 <16		msec msec
Voice Latency	AV6302 analog input to AV6301 USB output		<16		msec

3.7 Electrical Characteristics – Audio DAC and Headphone Amp

Operating Conditions: VDC = 4.4V to 5.5V or VIN = 3.2V to 4.3V, VDDIO = 3.3V, TA = 0ºC to +70 ºC; Typical specifications at TA = 25ºC, VDC = 5.0V or VIN=3.6V.

Table 3-7 AV6302 Electrical Characteristics - Audio DAC and Headphone Amp

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Full scale output voltage swing	0dB FS, sine wave, gain = 0dB		2.0		Vpp
SNR (A-weighted)	I2S test signal input		96		dB
Dynamic Range	I2S test signal input		96		dB
Total Harmonic Distortion	1kHz, R_L=32Ω, 0dB FS, P_O=1mW, gain=0dB 1kHz, R_L=32Ω, -3dB FS, P_O=10mW, gain=0dB 1kHz, R_L=32Ω, -13dB FS, P_O=1mW, gain=0dB		-60 -70 -80		dBc dBc dBc
Full power bandwidth (-1dB point)	0dB FS, sine wave, gain = 0dB		20		kHz
Bandwidth (-1dB point)	I2S test signal input		20		kHz
Max Output Power	R_L=32Ω, signal=FS, gain=0dB, THD < 10% R_L=16Ω, signal=FS, gain=0dB		15 30		mW mW
DAC Channel Separation	1kHz, -3dB FS and no signal		70		dB
Output Voltage Noise	20Hz – 20kHz; all zeros signal Mute activated		15 10		µVrms µVrms

3.8 Electrical Characteristics – MIC pre-amp and Voice ADC

Operating Conditions: VDC = 4.4V to 5.5V or VIN = 3.2V to 4.3V, VDDIO = 3.3V, TA = 0ºC to +70 ºC; Typical specifications at TA = 25ºC, VDC = 5.0V or VIN=3.6V.

Table 3-8 AV6302 Electrical Characteristics - MIC pre-amp and Voice ADC

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Max Input Signal Level	Max gain setting Min gain setting		4 450		mVrms mVrms
SNR	A-weighted, 0dB gain, f_S=16ksps		68		dB
Dynamic Range	A-weighted, 0dB gain, f_S=16ksps		68		dB
THD	-3dB input, 0dB gain		-60		dBc
Bandwidth (-1dB)	I2S test output		6.5		kHz
Input Equivalent Noise			TBD		µVrms
Input Resistance		TBD		TBD	Ω
Input Capacitance			TBD		pF
MIC Gain range	Min to max gain range	34	TBD		dB
MIC Gain Steps	Combination of coarse and fine register setting		1		dB

3.9 Electrical Characteristics – Battery Charger

Operating Conditions: T_A= 0ºC to +70 ºC, $V_{DC} \geq V_{BAT}$ + 0.3V; Typical specifications at T_A = 25ºC, V_{DC} = 5.0V

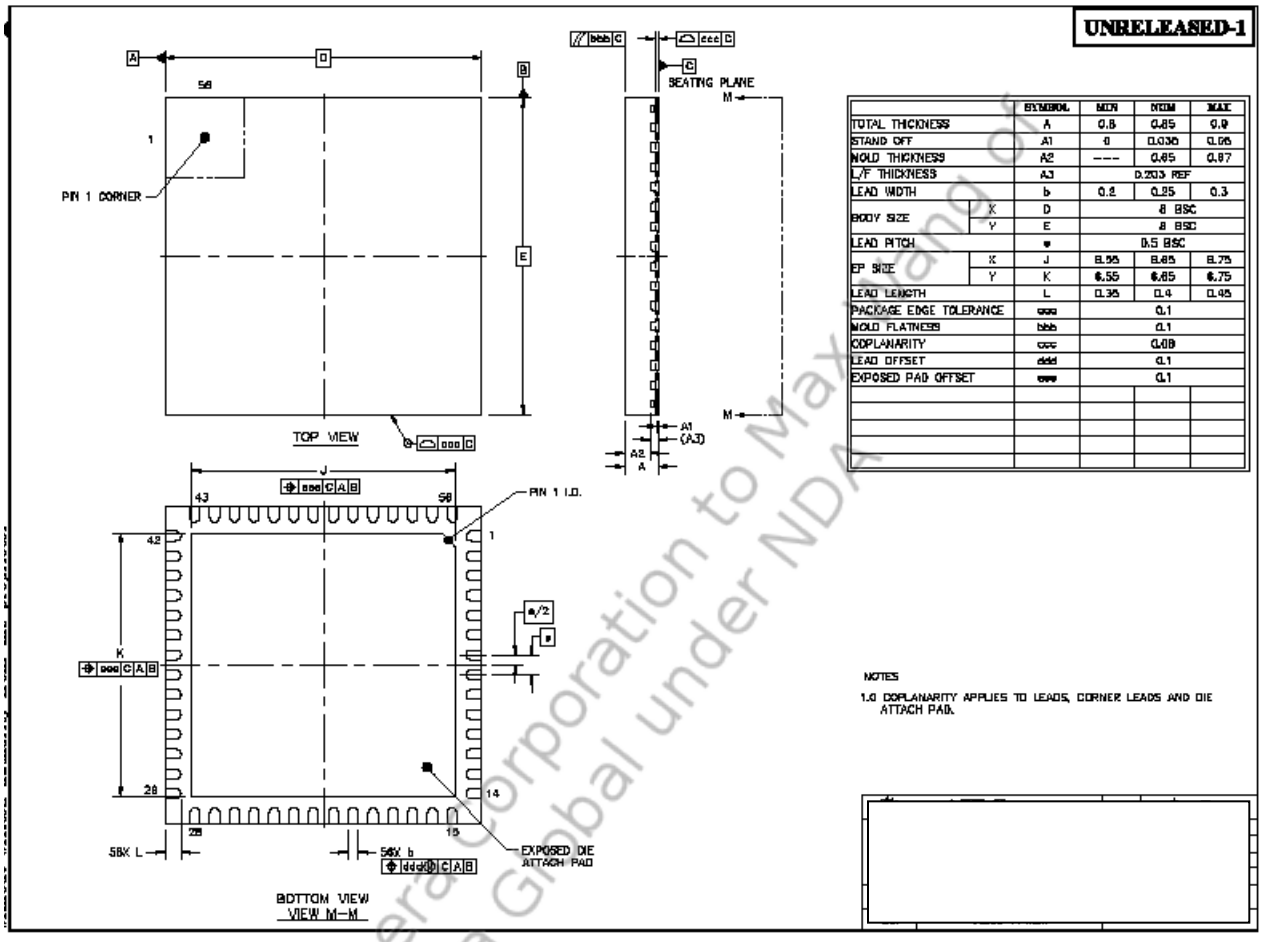
Table 3-9 AV6302 Electrical Characteristics - Battery Charger

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDC Input Voltage Range	V_{VDC} input	4.4	5.0	5.5	V
Maximum I_{CH} (Note 1)	Deep-discharged battery state; V_{BAT} < 3.15V		500	680	mA
Temperature Sense Shutoff Voltage	High Low		V_{DDIO} *0.8 V_{DDIO} * 0.5		V
Temperature Sense Threshold	High, Rising High, Falling Low, Falling Low, Rising		V_{DDIO}*0.80 V_{DDIO}*0.76 V_{DDIO}*0.50 V_{DDIO}*0.52		V V V V

Notes:
Note 1: Maximum constant charge current is relative to $V_{DC} – V_{BAT}$ and T_A

4 PACKAGE INFORMATION

4.1 Package Drawing and Details



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	6.55	6.65	6.75
	Y	K	6.55	6.65	6.75
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 4-1 56 pin QFN Mechanical Drawing

4.2 Package Marking

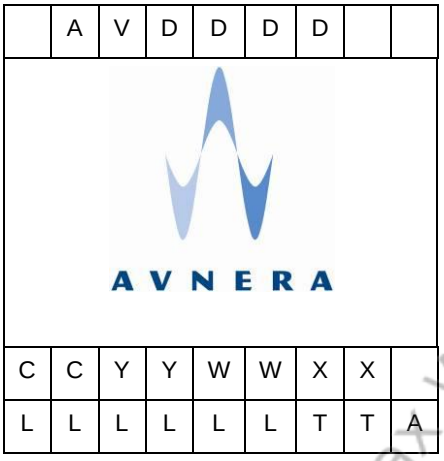


Figure 4-2 Package Marking Layout

Abbreviations:

AVDDDD	Product number (i.e. AV6302)
CC	Country Code (i.e. MY for Malaysia)
YY	2 digit year code
WW	2 digit work week
XX	Production revision
LLLLLL	Silicon Lot number
TT	Wafer split (1 by default)
A	Assembly Lot

5 CONTACT INFO & LEGAL DISCLAIMER

Avnera Corporation
16505 Bethany Court, Suite 100
Beaverton, Oregon 97006
U.S.A.
Main: +1.503.718.4100
Fax: +1.503.718.4101
www.avnera.com

Avnera Corporation reserves the right to make changes without notice to the product to improve function, reliability, or performance.

Avnera Corporation does not assume any liability arising from the application or use of the products or circuits described herein.