MG245X
Datasheet

VER.2.01

REVISION HISTORY

Version	Date	Description
VER.1.0	2008.1.19	▪ First Official Version Release
VER.1.1	2008.1.24	▪ Section 5 -Delete the followings in the Table 1. P0[0]:SCKO of SPI master P0[5]:SSB of SPI slave P0[6]:SDO of SPI slave P0[2]:MISO of SPI master P0[3]:SPICSNI P0[7]:SDI of SPI slave P0[1]:MOSI of SPI master P0[4]:SCKI of SPI slave ▪ Section 7.6.7 -Modify SPER(SPI E REGISTER) -> SPER(SPI EXTENDED REGISTER) ▪Section 7.6.12 -Modify SADCREF of SADCCON register
VER.1.2	2008.2.28	▪Section 3 -Correct Typing Error(-99dBm -> -98dBm: High RF RX Sensitivity) ▪Section 6 - Add 'NOTE' ▪Section 7.2 - Add 'NOTE' ▪Section 7.5 -PM3: Change from 1μA to 0.3μA. ▪Section 10 -Add Blocking/Desensitization -PM3: Change from 1μA to 0.3μA.
VER.1.3	2008.4.10	▪Section 4 - Modify Power ▪[Figure 2] - AVDD_XOSC -> DVDD_XOSC ▪[Table 1] -PIN H4: Modify Pin Description -PIN B5/B6 (AVDD_XOSC -> DVDD_XOSC)

		▪Section 6 -Modify entire contents ▪Section 7.3 -Modify contents(Add CLKDIV0) ▪Section 7.6.14 / 7.6.15 -Modify [Figure 18] / [Figure 19] and contents ▪Section 7.8.2 -Entire contents of PLL0/1/2/3 (PLL CONTROL 0/1/2/3 REGISTER, 0x2286, 0x2287, 0x2288, 0x228B)
VER.1.31	2008.6.19	▪Section 7.6.3 -Modify WDTCON. WDTWE: Modify Description. WDTEN: Modify Reset Value(0->1) WDTPRE: Modify Reset Value(0->11) ▪Section 7.7.3 -Modify MTFCSTS. Full: Modify R/W part(R/W ->R/O) Empty: Modify R/W part(R/W ->R/O)
VER.1.4	2008.7.20	▪Section 7.1.1 -Add the address table of code banking including common area. ▪Section 7.5 -Modify entire contents. ▪Section 7.6.4 -Modify entire contents. - Add ‘Note’. ▪Section 7.6.8 -Add ‘Note’ for ADPCM. ▪Section 7.6.10 -Add ‘Note’ in the bit field 0(mode) of QCTL. ▪Section 7.6.14 -Add ‘Note’.

		▪Section 7.6.15 -Add 'Note'.
VER.1.41	2008.12.8	▪Section 9 - Change V_{DD} to V_{DDIO} on V_{IH} , V_{IL} , V_{OH} ▪Section 7.2 -Add NOTE ▪Section 8,9 - Change MAX value 2.0 to 1.65 on VDD - Change MAX value 3.6 to 3.3 on VDDIO ▪Section 7.6.4 - Modify NOTE
VER.1.42	2009.2.13	▪Section 7.1.4 - Change 'P3OEN, P0OEN' initial/reset value to 0xFF, 'P1OEN' initial/reset value to 0xEF. ▪Section 7.8.1 - RX End Interrupt (RXEND_INT) Correct 'TX FIFO' to 'RX FIFO' ▪Section 7.8.2 -PCMD0 (PHY COMMAND0 REGISTER, 0x2200) Name RXON : Contents corrected - PCMD1 (PHY COMMAND1 REGISTER,0x2201) Name RXOFF : Contents corrected -RXRFPU (RF RX PATH POWER-UP REGISTER, 0x2205) Name LNAPU : Contents corrected -TXRFPD (RF TX PATH POWER-DOWN REGISTER, 0x2206) Name TXUMBUFPD : Contents corrected -PHYSTS1 (PHY STATUS1 REGISTER, 0x2271) Name TXSTSF, MDSTSF : Contents corrected
VER.1.5	2009.2.27	▪Section 6 -Modify 'application circuit' ▪Section 7.2 -Delete Reset Errata.

		▪Section 7.5 -Add PDM Register, PDCON Register ▪Section 7.6.4 -Change RTEN to STEN bit in PDCON ▪Section 7.6.5 -Add RCOSC1 Register
VER.1.51	2009.6.22	▪Section 7.5 - Modify reset value of PDM, PDCON register. ▪Section 7.6.5 -Modify reset value of RCOSC1 register. ▪Section 7.8.2 -Change 'TDCNF0' to 'TDCNF3', 'TDCNF1' to 'TDCNF0'.
VER.2.0	2009.12.10	▪Section 7.1.4 - P1OEN/P0REN/P1REN/P3REN reset value modified. ▪Section 7.6.11 - Contents modified. ▪Section 7.6.12 - Modify '8KHz' to '16KHz'. - SADCCON - SADCDONE, SADCREF contents modified. - SADCVALH - contents modified. - SADCVALL - contents modified. - SADCBIASH, SADCBIASL delete. ▪Section 7.6.14 - contents and note modified. ▪Section 7.6.15 - contents and note modified. ▪Section 10. - Add PM1 max value. ▪All section - Datasheet of MG2450 and of MG2455 are combined.
VER.2.01	2010.4.1	▪Section 7.6.4. - RTDLY description and reset value are changed.

CONTENTS

FIGURES

TABLES

1. INTRODUCTION

This guide is a datasheet for MG2450 and MG2455(hereinafter “MG245X”) of RadioPulse. The specification applied only to one model is described with **MG2450** or **MG2455** mark. All characteristics are common unless the ‘**MG2450**’ or ‘**MG2455**’ are marked.

MG245X is a true single-chip solution, compliant to ZigBee specifications and IEEE802.15.4, a complete wireless solution for ZigBee applications such as home control and sensor network.

MG245X consists of an RF transceiver with baseband modem, a hardwired MAC and an embedded 8051 microcontroller with internal flash memory for application program. It also includes numerous general-purpose I/O pins and peripheral devices such as timer and UART and is one of the first devices to provide an embedded Voice CODEC. This chip is ideal for very low power applications.

RadioPulse provides its customer with ZigBee stack software in compiled library. User application software can be compiled using a popular C-language compiler such as Keil.

2. APPLICATIONS

- Home Automation and Security
- Automatic Meter Reading
- Factory Automation and Motor Control
- Replacement for legacy wired UART
- Voice Applications
- Energy Management
- Remote Keyless Entry with Acknowledgement
- Low Power Telemetry
- Health-care equipments
- PC peripherals
- Toys

3. ENHANCED FEATURES

- Scalable Data Rate; 250kbps for ZigBee, 500kbps and 1Mbps for custom applications.
- Voice Codec Support; μ-law/a-law/ADPCM
- High RF RX Sensitivity; -98dBm @1.5V
- High RF TX Power of +8dBm @1.5V
- Embedded 8051 Compatible Microprocessor with 96KB Embedded Flash Memory for Program Space
- 8KB of Data Memory
- Power Management Scheme with Deep Sleep Mode(under 1μA)
- Single Voltage operation; 1.9 to 3.3V using an internal regulator(1.5V core)

4. FEATURES

RF Transceiver

- Single-chip 2.4GHz RF Transceiver
- Low Power Consumption
- Low Operating Voltage of 1.5V
- High Sensitivity of –98dBm@1.5V
- No External T/R Switch and Filter needed
- On-chip VCO, LNA, and PA
- Programmable Output Power up to +8dBm@1.5V
- Direct Sequence Spread Spectrum
- O-QPSK Modulation
- Scalable Data Rate: 250Kbps for ZigBee, 500Kbps and 1Mbps for private application
- RSSI Measurement
- Compliant to IEEE802.15.4

Hardwired MAC

- Two 256-byte circular FIFOs
- FIFO management
- AES-128 Engine
- CRC-16 Computation and Check

8051-Compatible Microcontroller

- 8051 Compatible(single cycle execution)
- 96KB Embedded Flash Memory
- 8KB Data Memory

- 128-byte CPU dedicated Memory
- 1KB Boot ROM
- Dual DPTR Support
- Multi-Bank Support for 96KB Program Memory(3Banks)
- I2S/PCM Interface with two128-byte FIFOs
- μ-law/a-law/ADPCM Voice Codec
- Two High-Speed UARTs with Two 16-byte FIFOs (up to 1Mbps)
- 4 Timers/2 PWMs
- Watchdog Timer
- Sleep Timer
- Quadrature Signal Decoder
- 24 General Purpose I/Os**(MG2450)** / 22 General Purpose I/Os**(MG2455)**
- Internal RC oscillator for Sleep Timer
- On-chip Power-on-Reset
- 4-channel 8-bit ADC
- SPI Master/Slave Interface
- ISP (In System Programming)
- Internal Temperature Sensor

Clock Inputs

- 16MHz Crystal for System Clock(optional 19.2MHz)
- 32.768KHz Crystal for Sleep Timer(optional)

Power

- When using Internal Regulator of MG245X
  1.5V(Core)/1.9~3.3V(I/O) Operation
- When NOT using Internal Regulator of MG245X
  1.5V(Core)/1.5V(I/O) Operation
- Power Management Scheme with Deep Sleep Mode Support
- Separate On-chip Regulators for Analog and Digital Circuitry.
- Power Supply Range for Internal Regulator(1.9V(Min) ~ 3.6V(Max))
- Battery Monitoring Support

Package

- **MG2450**: Lead-Free 72-pin VFBGA Package (5mm × 5mm x 0.9mm)
- **MG2455**: Lead-Free 48-pin QFN Package (7mm x 7mm x 0.9mm)

5. PIN DESCRIPTION

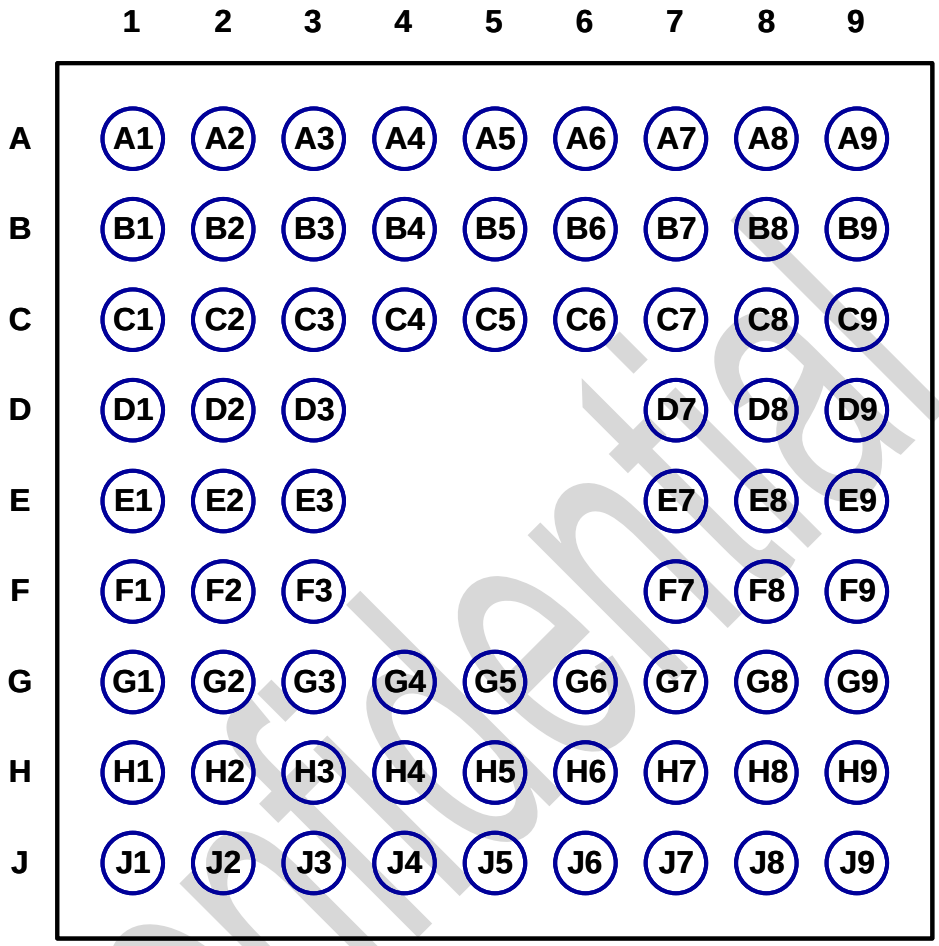


Figure 1. Pinout top view(1) of MG2450-B72(72-pin VFBGA Package)

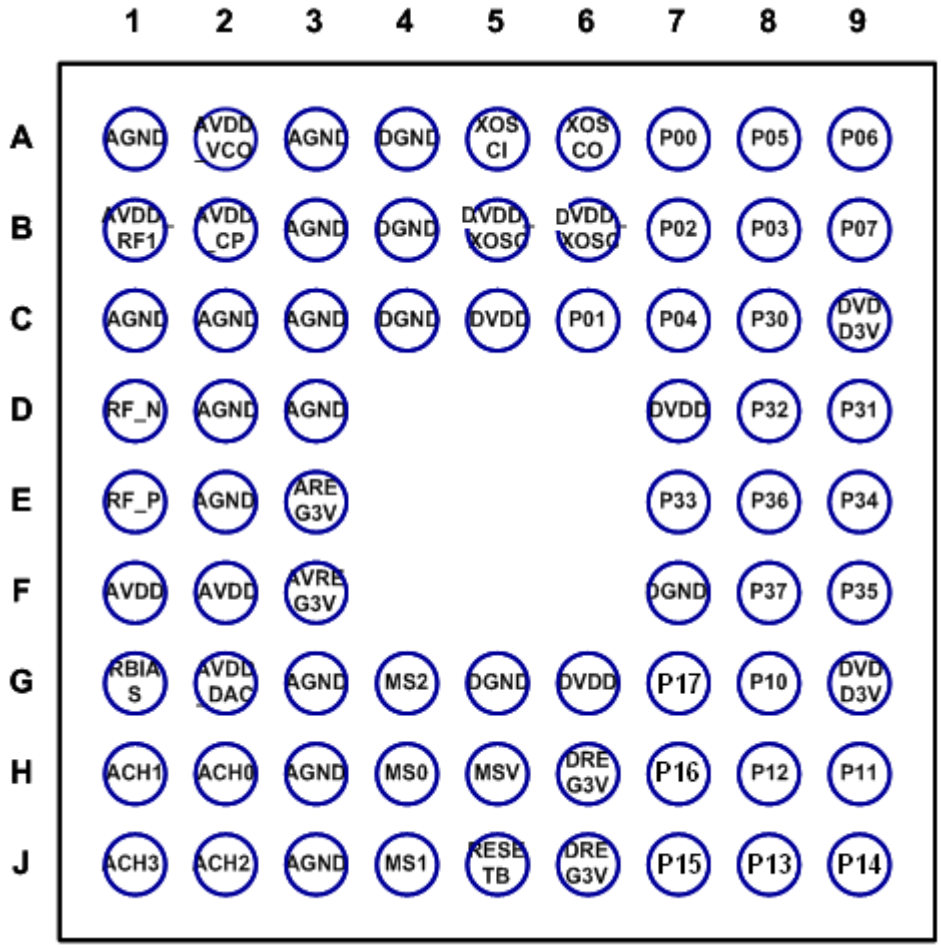


Figure 2. Pinout top view(2) of MG2450-B72(72-pin VFBGA Package)

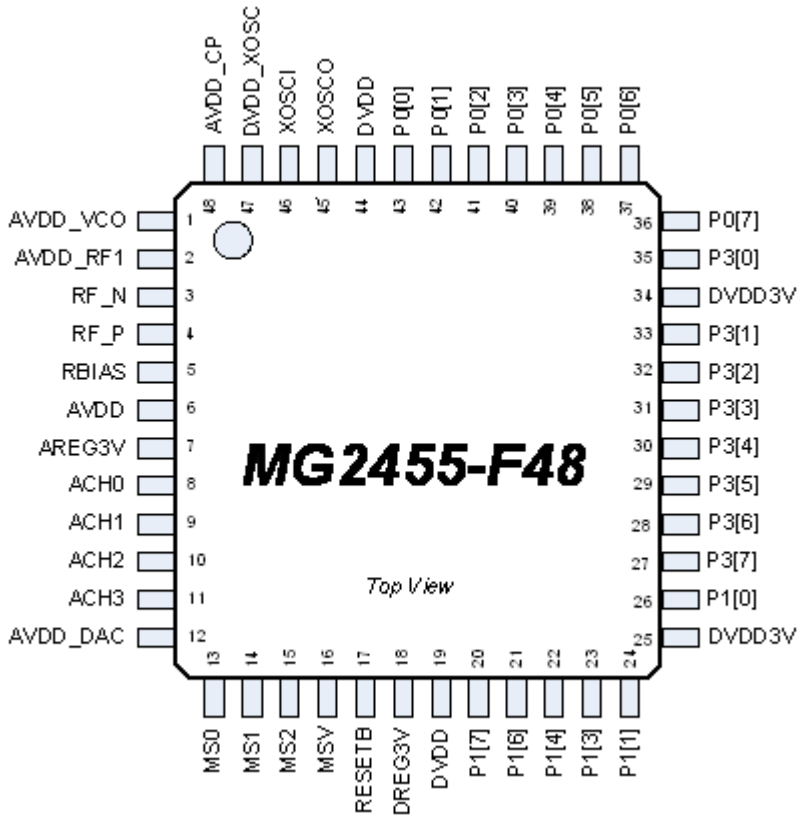


Figure 3. Pinout top view of MG2455-F48(Exposed Pad 48-pin QFN Package)

** Chip Ground(GND) is located at the bottom of a chip*

The **MG2450** Pinout overview is shown in [Table 1].

Table 1. Pinout overview of MG2450

Ball	Ball Name	Ball Type	Ball Description
A1	AGND	Ground	Ground for RF and Analog blocks.
A2	AVDD_VCO	Power	1.5V Power supply for VCO and Divider
A3	AGND	Ground	Ground for RF and Analog blocks.
A4	DGND	Ground	Ground for digital core and IO.
A5	XOSCI	Analog	Crystal Oscillator Input.
A6	XOSCO	Analog	Crystal Oscillator Output.
A7	P0[0]	B (digital)	Port P0.0 / I2SRX_DI.
A8	P0[5]	B (digital)	Port P0.5 / I2STX_LRCLK.
A9	P0[6]	B (digital)	Port P0.6 / I2STX_BCLK.
B1	AVDD_RF1	Power	1.5V Power supply for LNA and PA.
B2	AVDD_CP	Power	1.5V Power supply for Charge Pump and PFD.
B3	AGND	Ground	Ground for RF and Analog blocks.
B4	DGND	Ground	Ground for digital core and IO.
B5	DVDD_XOSC	Power	1.5V Power supply for Crystal oscillator.
B6			
B7	P0[2]	B (digital)	Port P0.2 / I2SRX_BCLK.
B8	P0[3]	B (digital)	Port P0.3 / I2SRX_MCLK.
B9	P0[7]	B (digital)	Port P0.7 / I2STX_MCLK.
C1	AGND	Ground	Ground for RF and Analog blocks.
C2	AGND	Ground	Ground for RF and Analog blocks.
C3	AGND	Ground	Ground for RF and Analog blocks.
C4	DGND	Ground	Ground for digital core and IO.
C5	DVDD	Power	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V

		(In/Out)	Power supply for Digital Core(input mode @ No REG).
C6	P0[1]	B (digital)	Port P0.1 / I2SRX_LRCK.
C7	P0[4]	B (digital)	Port P0.4 / I2STX_DO.
C8	P3[0]	B (digital)	Port P3.0 / RXD0 / QUADXA.
C9	DVDD3V	Power	3.0V Power supply for Digital IO.
D1	RF_N	RF	Negative RF input/output signal to LNA / from PA in receive / transmit mode.
D2	AGND	Ground	Ground for RF and Analog blocks.
D3	AGND	Ground	Ground for RF and Analog blocks.
D7	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core(input mode @ No REG).
D8	P3[2]	B (digital)	Port P3.2 / INT0 (active low).
D9	P3[1]	B (digital)	Port P3.1 / TXD0 / QUADXB.
E1	RF_P	RF	Positive RF input/output signal to LNA / from PA in receive / transmit mode.
E2	AGND	Ground	Ground for RF and Analog blocks.
E3	AVREG3V	Power	3.0V Power supply for Analog Internal Voltage Regulator.
E7	P3[3]	B (digital)	Port P3.3 / INT1 (active low).
E8	P3[6]	B (digital)	Port P3.6 / 12mA Drive capability /PWM2/RTS1/SPICLK.
E9	P3[4]	B (digital)	Port P3.4 /T0/RTS0/QUADYA/SPIDI.
F1	AVDD	Power (In/Out)	Output of Analog Internal Voltage Regulator (1.5V) / 1.5V Power supply for Mixer, VGA and LPF (input mode @ No REG).
F2	AVDD	Power (In/Out)	Output of Analog Internal Voltage Regulator (1.5V) / 1.5V Power supply for Mixer, VGA and LPF (input mode @ No REG).

F3	AVREG3V	Power	3.0V Power supply for Analog Internal Voltage Regulator.
F7	DGND	Ground	Ground for digital core and IO.
F8	P3[7]	B (digital)	Port P3.7 / 12mA Drive capability /PWM3 /CTS1/SPICSN(slave only).
F9	P3[5]	B (digital)	Port P3.5 /T1/CTS0/QUADYB/SPIDO.
G1	RBIAS	Analog	External bias resistor.
G2	AVDD_DAC	Power	1.5V Power supply for ADC and DAC.
G3	AGND	Ground	Ground for RF and Analog blocks.
G4	MS[2]	I (digital)	MS[2:0](Mode Select) 000:Normal Mode 001:ISP Mode
G5	DGND	Ground	Ground for digital core and IO.
G6	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core(input mode @ No REG).
G7	P1[7]	O (digital)	Port P1.7 GPO / P0AND/ TRSW / Fold / Clocks / BIST Fail Indicator.
G8	P1[0]	B (digital)	Port P1.0 / RXD1.
G9	DVDD3V	Power	3.0V Power supply for Digital IO.
H1	ACH1	Analog	Sensor ADC input / BBA Output.
H2	ACH0	Analog	Sensor ADC input / BBA Output.
H3	AGND	Ground	Ground for RF and Analog blocks.
H4	MS[0]	I (digital)	MS[2:0](Mode Select) 000:Normal Mode 001:ISP Mode
H5	MSV	I (digital)	Mode Select of Voltage.
H6	DVREG3V	Power	3.0V Power supply for Internal Voltage Regulator.
H7	P1[6]	B (digital)	Port P1.6 / TRSWB.

H8	P1[2]	B (digital)	Port P1.2.
H9	P1[1]	B (digital)	Port P1.1 / TXD1.
J1	ACH3	Analog	Sensor ADC input / BBA Output.
J2	ACH2	Analog	Sensor ADC input / BBA Output.
J3	AGND	Ground	Ground for RF and Analog blocks.
J4	MS[1]	I (digital)	MS[2:0](Mode Select) 000:Normal Mode 001:ISP Mode
J5	RESETB	I (digital)	Reset (Active Low).
J6	DVREG3V	Power	3.0V Power supply for Internal Voltage Regulator.
J7	P1[5]	B (digital)	Port P1.5.
J8	P1[3]	B (digital)	Port P1.3 / QUADZA / Sleep Timer OSC Buffer Output / RTCLKOUT.
J9	P1[4]	B (digital)	Port P1.4 / QUADZB / Sleep Timer OSC Buffer Input.

The **MG2455** Pinout overview is shown in [Table 2].

Table 2. Pinout overview of MG2455

Pin NO.	Pin Name	Pin Type	Pin Description
Exposed bottom	GND	Ground	Ground for RF, Analog, digital core, and IO
1	AVDD_VCO	Power	1.5V Power supply for VCO and Divider
2	AVDD_RF1	Power	1.5V Power supply for LNA and PA
3	RF_N	RF	Negative RF input/output signal to LNA / from PA in receive / transmit mode
4	RF_P	RF	Positive RF input/output signal to LNA / from PA in receive / transmit mode
5	RBIAS	Analog	External bias resistor
6	AVDD	Power	Output of Analog Internal Voltage Regulator (1.5V) / 1.5V

		(In/Out)	Power supply for Mixer, VGA, and LPF (input mode @ No REG)
7	AVREG3V	Power	3.0V Power supply for Analog Internal Voltage Regulator
8	ACH0	Analog	Sensor ADC input
9	ACH1	Analog	Sensor ADC input
10	ACH2	Analog	Sensor ADC input
11	ACH3	Analog	Sensor ADC input
12	AVDD_DAC	Power	1.5V Power supply for ADC and DAC
13	MS[0]	I (digital)	MS[2:0] (Mode Select) ▪ When using Internal Regulator of MG2455 000: Normal mode 001: ISP mode ▪ When NOT using Internal Regulator of MG2455 010: Normal mode 110: ISP mode
14	MS[1]	I (digital)	
15	MS[2]	I (digital)	
16	MSV	I (digital)	Mode Select of Voltage 0 – 1.5V
17	RESETB	I (digital)	Reset (Active Low)
18	DVREG3V	Power	3.0V Power supply for Internal Voltage Regulator
19	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core(input mode @ No REG)
20	P1[7]	O (digital)	Port P1.7 GPO / P0AND / TRSW
21	P1[6]	B (digital)	Port P1.6 / TRSWB
22	P1[4]	B (digital)	Port P1.4 / QUADZB / Sleep Timer OSC Buffer Input
23	P1[3]	B (digital)	Port P1.3 / QUADZA / Sleep Timer OSC Buffer Output / RTCLKOUT
24	P1[1]	B (digital)	Port P1.1 / TXD1
25	DVDD3V	Power	3.0V Power supply for Digital IO
26	P1[0]	B (digital)	Port P1.0 / RXD1

27	P3[7]	B (digital)	Port P3.7 / 12mA Drive capability / PWM3 / CTS1 / SPICSN
28	P3[6]	B (digital)	Port P3.6 / 12mA Drive capability /PWM2 / RTS1 / SPICLK
29	P3[5]	B (digital)	Port P3.5 / T1 / CTS0 / QUADYB / SPIDO
30	P3[4]	B (digital)	Port P3.4 / T0 / RTS0 / QUADYA / SPIDI
31	P3[3]	B (digital)	Port P3.3 / INT1 (active low)
32	P3[2]	B (digital)	Port P3.2 / INT0 (active low)
33	P3[1]	B (digital)	Port P3.1 / TXD0 / QUADXB
34	DVDD3V	Power	3.0V Power supply for Digital IO
35	P3[0]	B (digital)	Port P3.0 / RXD0 / QUADXA
36	P0[7]	B (digital)	Port P0.7 / I2STX_MCLK
37	P0[6]	B (digital)	Port P0.6 / I2STX_BCLK
38	P0[5]	B (digital)	Port P0.5 / I2STX_LRCLK
39	P0[4]	B (digital)	Port P0.4 / I2STX_DO
40	P0[3]	B (digital)	Port P0.3 / I2SRX_MCLK
41	P0[2]	B (digital)	Port P0.2 / I2SRX_BCLK
42	P0[1]	B (digital)	Port P0.1 / I2SRX_LRCK
43	P0[0]	B (digital)	Port P0.0 / I2SRX_DI
44	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core(input mode @ No REG)

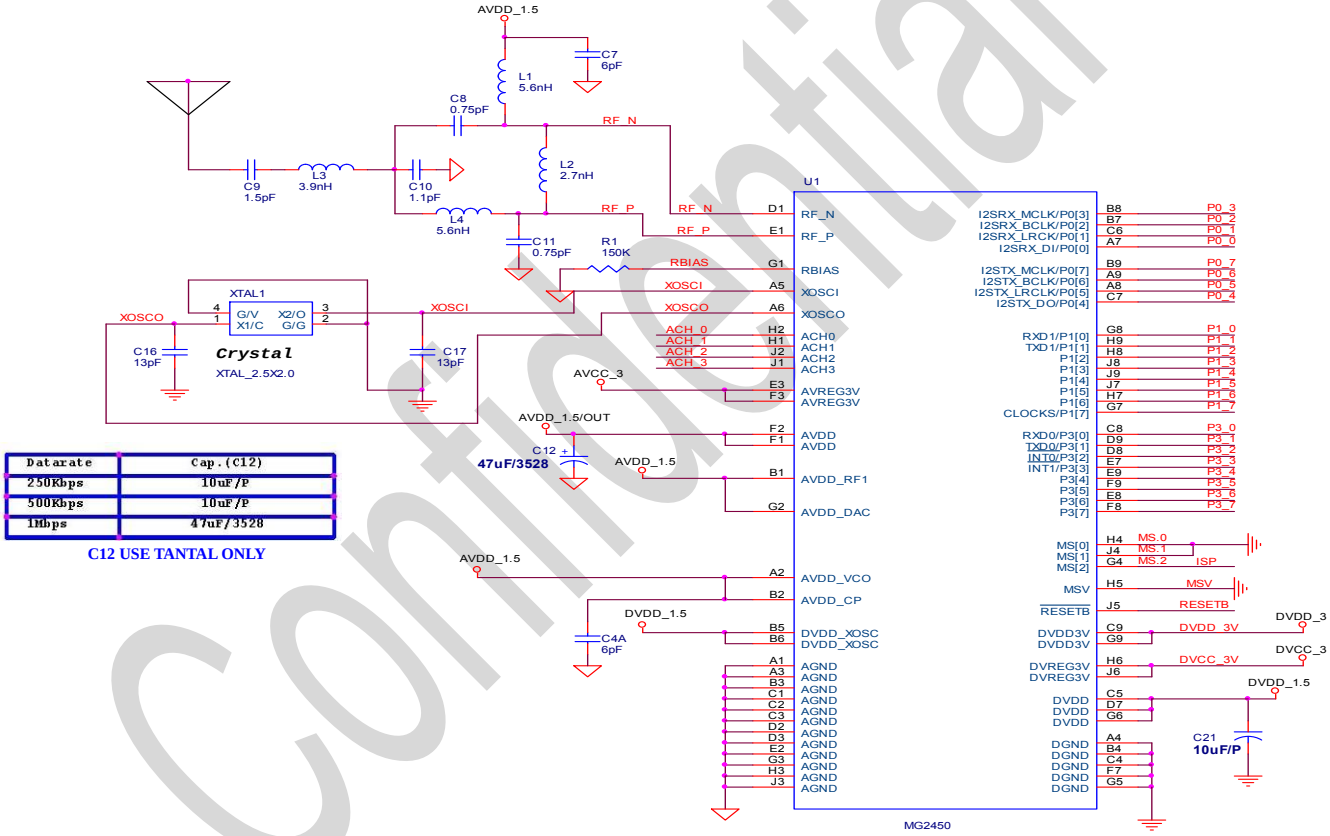
45	XOSCO	Analog	Crystal Oscillator Output
46	XOSCI	Analog	Crystal Oscillator Input
47	DVDD_XOSC	Power	1.5V Power supply for Crystal oscillator.
48	AVDD_CP	Power	1.5V Power supply for Charge Pump and PFD

6. APPLICATION CIRCUITS

The MG245X operates from a single supply voltage. The core must run at 1.5V, so, if 1.5V is available, both the core and the I/O can run from 1.5V. If a higher voltage I/O is required (or higher voltage is available on the board) the MG245X contains an on-chip voltage regulator that can step down a 1.9V~3.3V supply to 1.5V for the core. In this case the I/O can be run from a 1.9V to 3.3V supply.

A typical application circuit for the MG245X using 1.9V~3.3V as the I/O power through the internal regulator is shown in [Figure 4, 5].

Typical value and description of external components are shown in [Table 3, 4] below.



Datarate	Cap.(C12)
250Kbps	10uF/P
500Kbps	10uF/P
1Mbps	47uF/3528

Figure 4. MG2450 Application Circuit (I/O Power: 1.9V~3.3V , MS[1]=0)

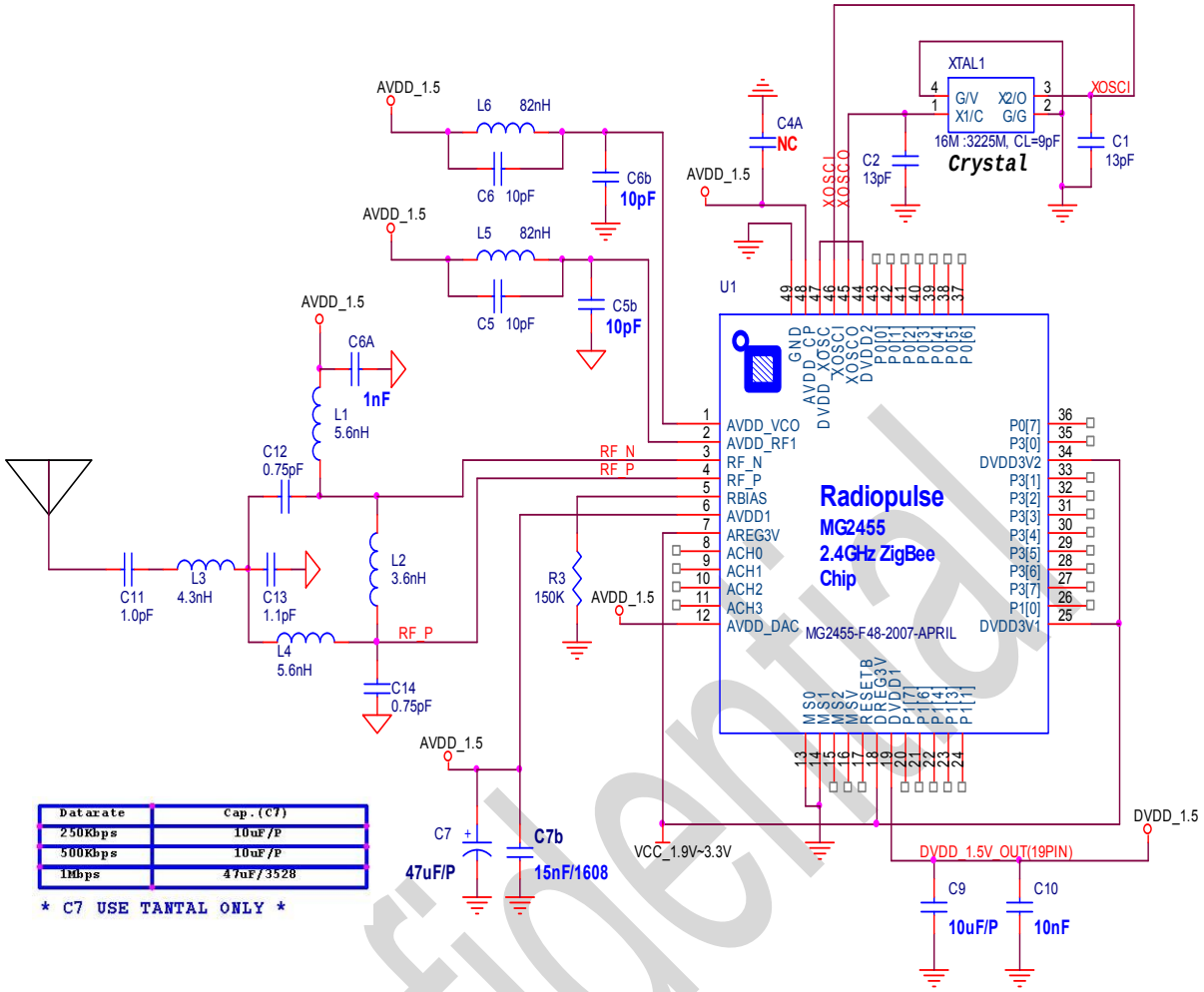
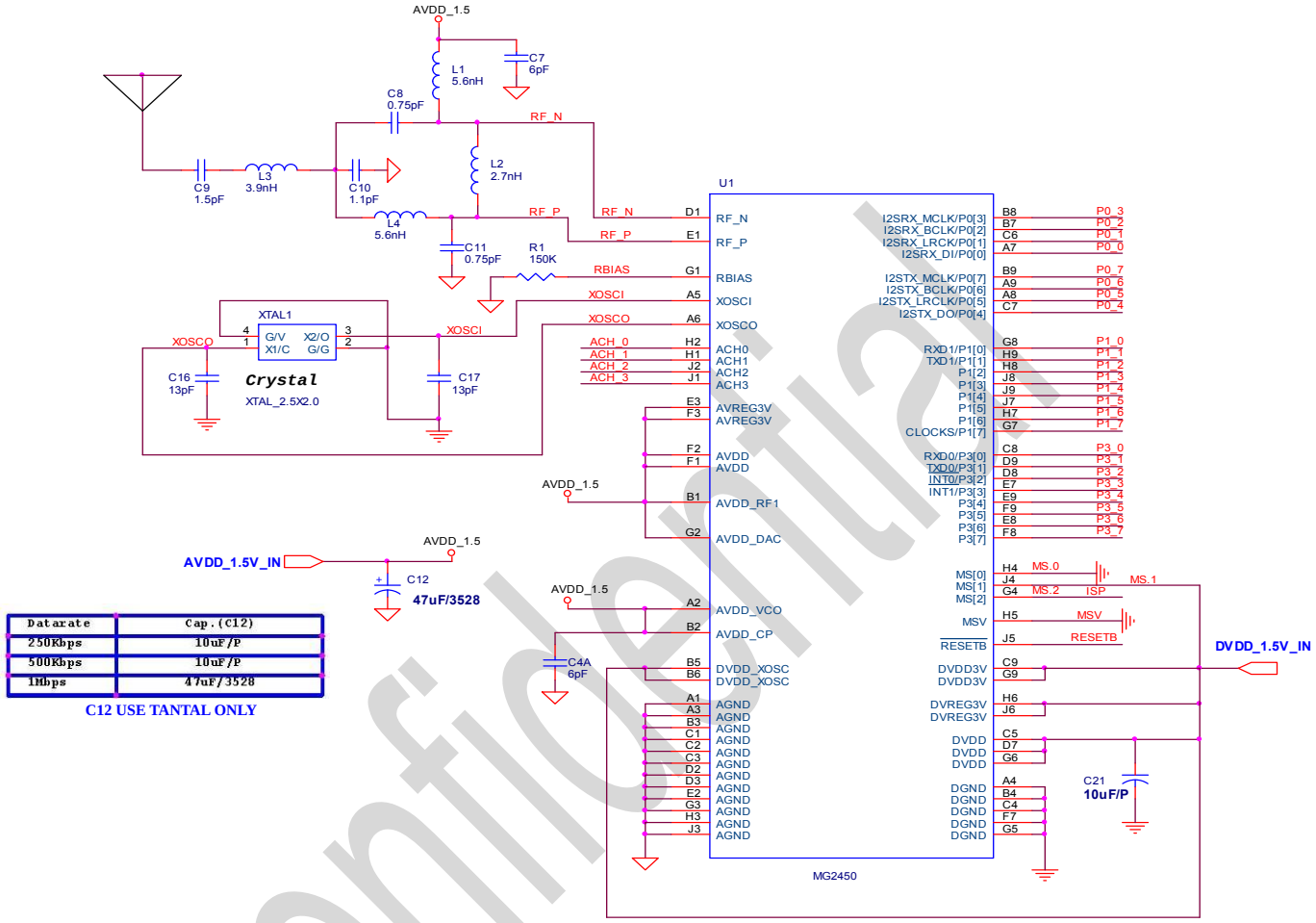


Figure 5. MG2455 Application Circuit(I/O Power: 1.9V~3.3V , MS[1]=0)

**** GND is bottom pad (down-bonding pad) in the above schematic.*

[Figure 6, 7] shows the application circuit of MG245X when using 1.5V as the I/O power and not using internal regulator. In this case, a software setting is needed to turn off the internal regulator of the devices as **CAUTION 1.**



Datarate	Cap.(C12)
250Kbps	10uF/P
500Kbps	10uF/P
1Mbps	47uF/3528

C12 USE TANTAL ONLY

Figure 6. MG2450 Application Circuit (I/O Power: 1.5V , MS[1]=1)

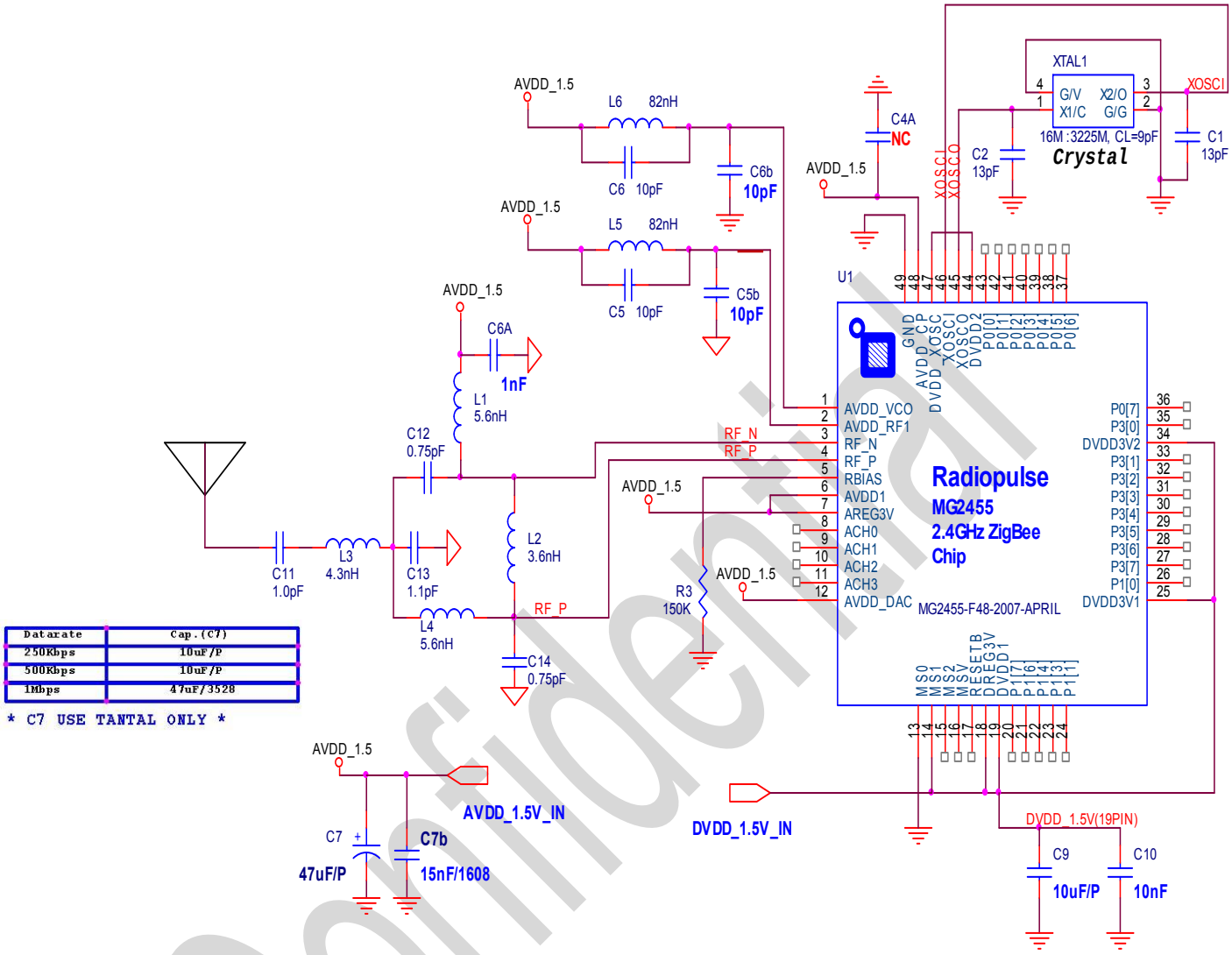


Figure 7. MG2455 Application Circuit (I/O Power: 1.5V , MS[1]=1)

**** GND is bottom pad (down-bonding pad) in the above schematic.*

CAUTION 1: Software Setting

In order to turn off internal regulator of MG245X, please call ZHAL_3V_LOGIC_INIT() first and then write XBYTE[0x22F1] & = 0x7F in the source of DK(Development Kit)

```
ZHAL_3V_LOGIC_INIT();
XBYTE[0x22F1] & = 0x7F;    //Turn off AVREG(Analog Regulator)
```

NOTE: When MG245X is operating below minimum operating voltage, reset will be in error because of unstable voltage. When you apply reset circuit of MG245X, reset function will be more stable when Power ON/OFF. For more detailed information, refer to the Note of '**Section 7.2 RESET**'.

[Table 3] shows the external components of [Figure 4, 5] above.

Table 3. Overview of external components (excluding supply decoupling capacitors)

NO.	Part Name	Specification	Amount	Position
1	Chip-Cap	13pF	2pc	C16, C17
2	Chip-Cap	0.75pF	2pc	C8, C11
3	Chip-Cap	1.5pF	1pc	C9
4	Chip-Cap	1.1pF	1pc	C10
5	Chip-Cap	10μF/P	1pc	C21
6	Chip-Ind	5.6nH	2pc	L1, L4
7	Chip-Ind	2.7nH	1pc	L2
8	Chip-Ind	3.9nH	1pc	L3
9	Chip-Res	150K	1pc	R1
10	ZigBee Chip	MG2450-B72	1pc	U1
11	X-TAL-SMD	XTAL_2.5X2.0/10ppm	1pc	XTAL1

[Table 4] shows the external components of [Figure 6, 7] above.

Table 4. Overview of external components (excluding supply decoupling capacitors)

NO.	Part Name	Specification	Amount	Position
1	Chip-Cap	13pF	2pc	C2, C1
2	Chip-Cap	10μF	1pc	C9
3	Chip-Cap	0.75pF	2pc	C12, C14
4	Chip-Cap	1pF	1pc	C11
5	Chip-Cap	1.1pF	1pc	C13
6	Chip-Ind	5.6nH	2pc	L1, L4
7	Chip-Ind	3.6nH	1pc	L2
8	Chip-Ind	4.3nH	1pc	L3
9	Chip-Res	150K	1pc	R3
10	ZigBee Chip	MG2455-F48	1pc	U1

11	X-TAL-SMD	16M:3225M/10ppm, CL=9pF	1pc	XTAL1

[Figure 8, 9] below shows the PCB artwork pattern of the recommended RF matching circuit.

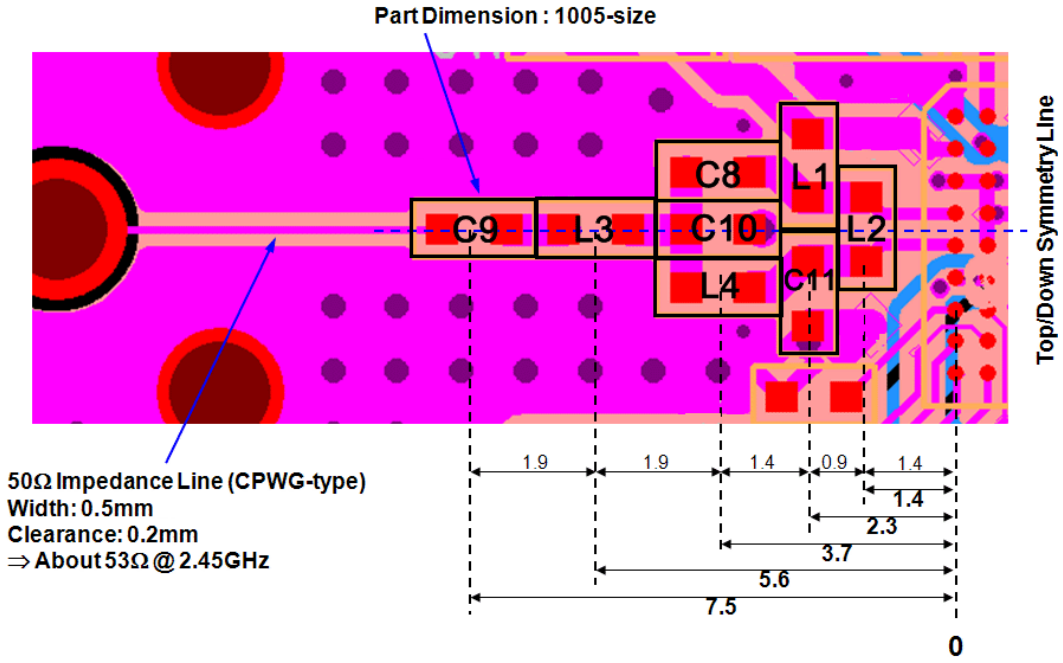


Figure 8. PCB artwork of MG2450

***CAUTION*: Please use ONLY Murata C,L.**

RF Matching Procedure

① The values of L1/C8/L4/C11 are adjusted to 2.4GHz band.

② L3 and C9 organize narrow band-pass.

③ Adjust L2 and C10 value to maximize output level.

④ Adjust L3 and C9 to minimize 2nd and 3rd harmonic.

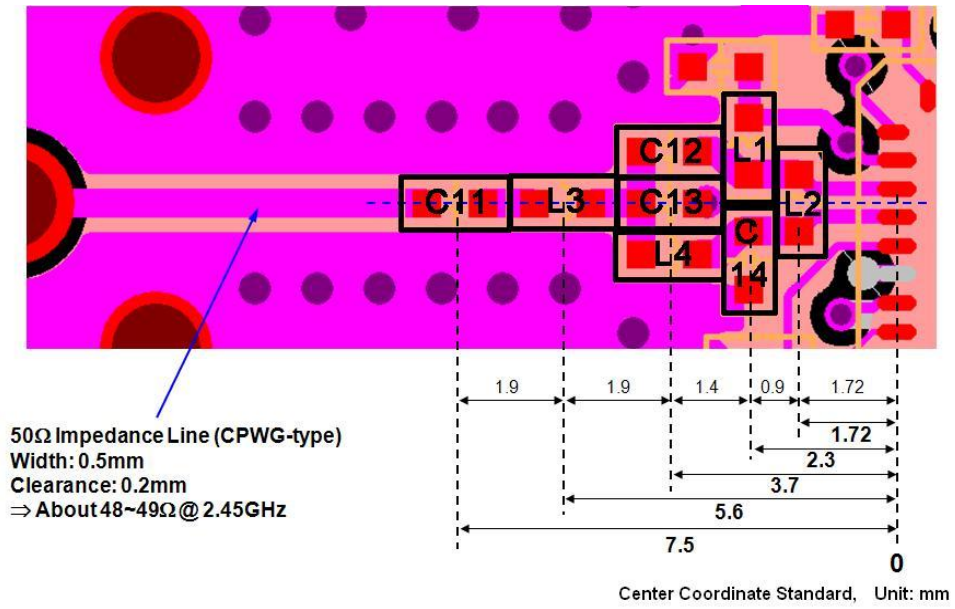


Figure 9. PCB artwork of MG2455

***CAUTION*: Please use ONLY Murata C,L.**

RF Matching Procedure

① The values of L1/C12/L4/C14 is adjusted to 2.4GHz band.

② L3 and C11 organize narrow band-pass.

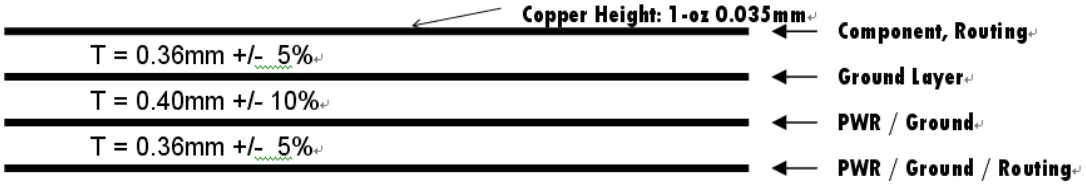
③ Adjust L2 and C13 value to maximize output level.

④ Adjust L3 and C11 to minimize 2nd and 3rd harmonic.

For best performance, a four layer PCB is highly recommended. As the picture above, the first layer(top layer) is used for signal routing and the empty area needs to be used as ground.
It is not good for signal routing with middle layers. Second layer is used for connecting ground routing and third layer is used for connecting power-line. Finally, fourth layer is used for ground and signal routing.

The middle of the bottom of **MG2455** package should be connected to the ground of a board. The ground is located in the middle of the bottom of **MG2455**. The figure below shows the PCB layer structure of **MG2455**.

PCB Layer Structure



PCB : 1.2mm, FR-4 , Er = 4.5

7. FUNCTIONAL DESCRIPTION

[Figure 10, 11] shows the block diagram of MG245X. The MG245X consists of 2.4GHz RF, Modem, a MAC hardware engine, a Voice CODEC block, Clocks, Peripherals, a Flash memory and Microcontroller (MCU) block.

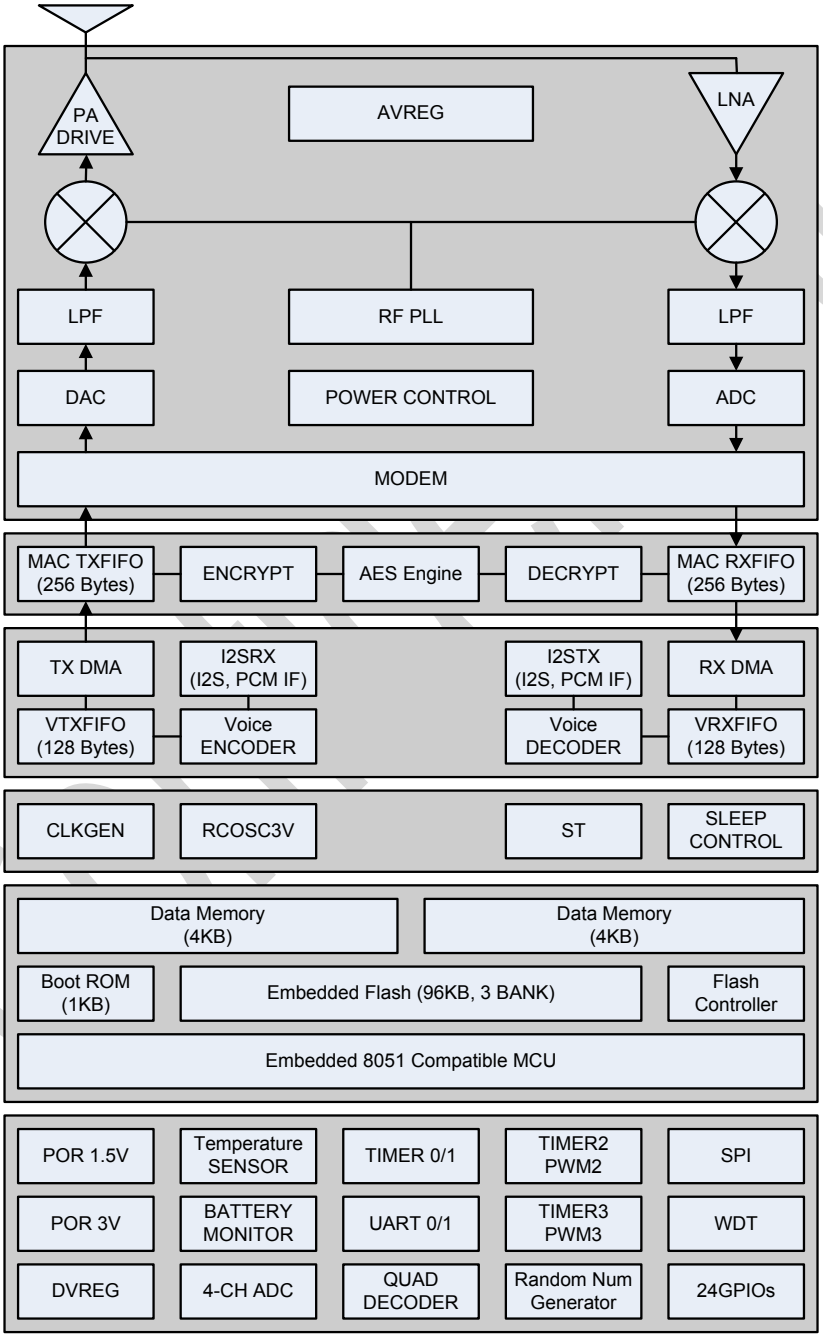


Figure 10. Functional Block Diagram of MG2450

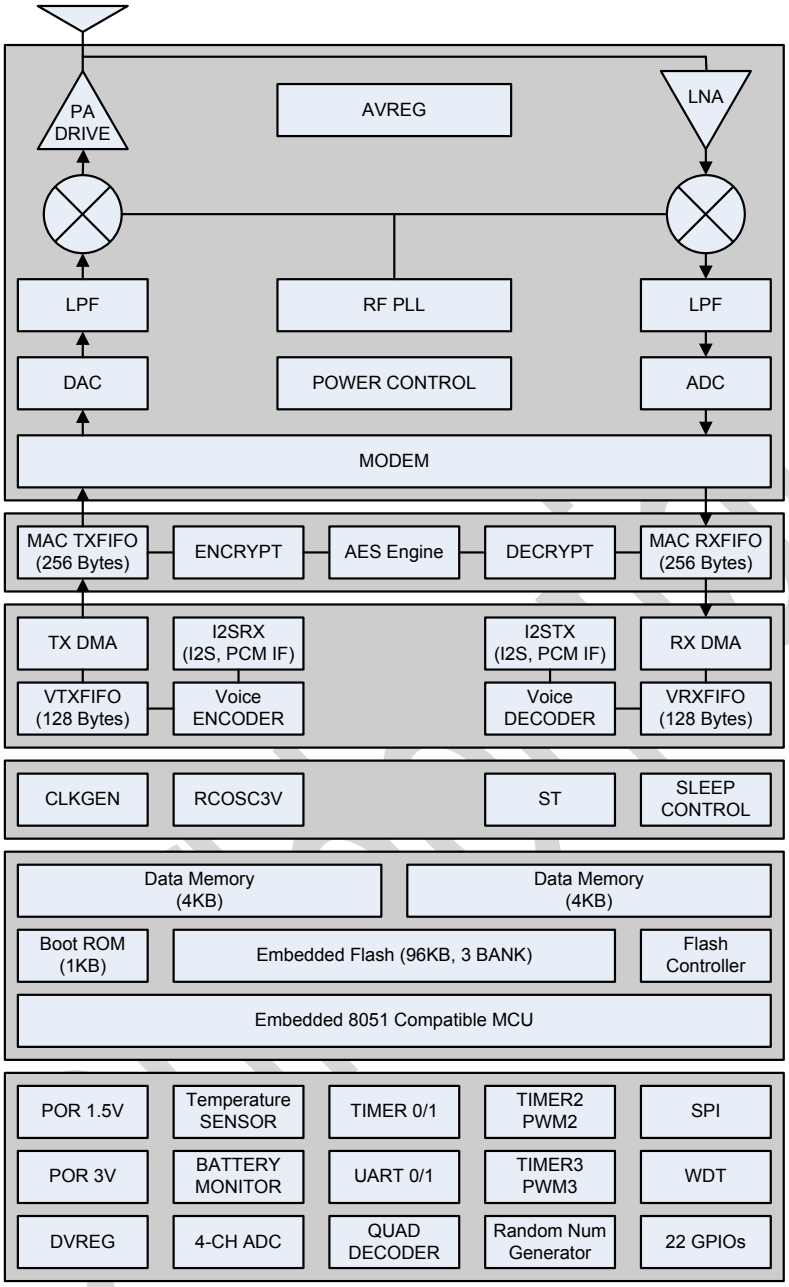


Figure 11. Functional Block Diagram of MG2455

In the receive mode, the received RF signal is amplified by the LNA(Low Noise Amplifier), down-converted to quadrature signal and then to baseband signal. The baseband signal is filtered, amplified, converted to a digital signal by ADC and transferred to a modem. The data, which is the result of signal processing such as dispreading, is transferred to the MAC block.

In the transmit mode, the buffered data at the MAC is transferred to a baseband modem which, After signal processing such as spreading and pulse shaping, outputs a signal through the DAC. The analog baseband signal is filtered by the low-pass filter, converted to RF signal by up-

conversion mixer, is amplified by PA and finally applied to an antenna.

The MAC block provides IEEE802.15.4 compliant hardware and it is located between microprocessor and a baseband modem. MAC block includes FIFOs for transmitting/receiving packet, AES engine for security operation, CRC and related control circuit. In addition, it supports automatic CRC check and address decoding.

MG245X integrates a high performance embedded microcontroller, compatible to an intel i8051 microcontroller in an instruction level. This embedded microcontroller has 8-bit operation architecture sufficient for controller applications. The embedded microcontroller has 4-stage pipeline architecture to improve the performance over previous compatible chips making it capable of executing simple instructions during a single cycle.

The memory organization of the embedded microcontroller consists of program memory and data memory. The data memory has 2 memory areas. For more detail explanation, refer to the data memory section.(7.1.2)

MG2450 includes 24 GPIO and MG2455 has 22. MG245X also includes various peripheral circuits to aid in the development of an application circuit with an interrupt handler to control the peripherals. MG245X uses 16MHz crystal oscillator for RF PLL and 8MHz clock generated from 16MHz in clock generator is used for microcontroller, MAC, and the clock of a baseband modem.

MG245X supports a voice function as follows. The data generated by an external ADC is input to the voice block via I2S interface. After the data is received via I2S it is compressed by the voice codec, and stored in Voice TXFIFO. The data in Voice TXFIFO is transferred to the MAC TXFIFO and then transmitted via PHY. In contrast, the received data in MAC RXFIFO is transferred to voice RXFIFO via DMA operation. The data in voice RXFIFO is decompressed by the internal voice codec. The decompressed data is transferred to the external DAC via I2S interface.

7.1. MEMORY ORGANIZATION

7.1.1. PROGRAM MEMORY

The address space of program memory is 64KB(0x0000~0XFFFF). Basically, the lower 63KB of program memory is implemented by Non-volatile memory. The upper 1KB from 0XFC00 to

0XFFFF is implemented by both Non-volatile memory and ROM. As shown in [Figure 12] below, there are two types of memory in the same address space. The address space, which is implemented by Non-volatile memory, is used as general program memory and the address space, which is implemented by ROM, is used for ISP (In-System Programming).

As shown in (a) of [Figure 12] below, when Power is turned on, the upper 1KB of program memory is mapped to ROM. As shown in (b) of [Figure 12], if this program area (1KB) is used as non-volatile program memory, ENROM should be set to '0'. See the SFR section(7.1.4) for ENROM.

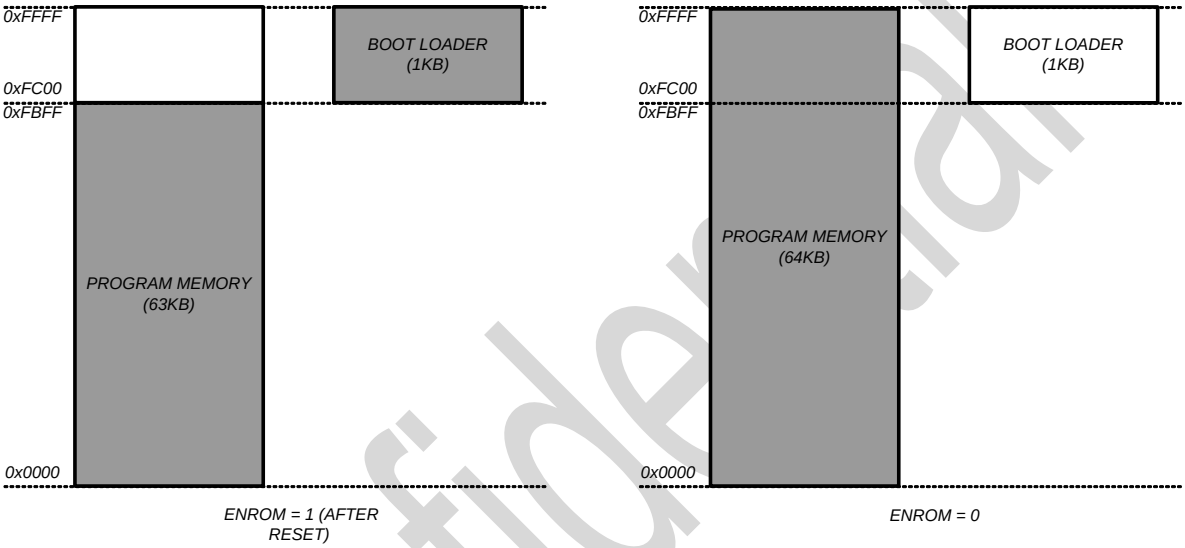


Figure 12. Address Map of Program Memory

MG245X includes non-volatile memory of 96KB. However, as described already, program memory area is 64KB. Therefore, if necessary, the upper 64KB of physical 96KB non-volatile memory is separated into two 32KB memory bank. Each bank is logically mapped to the program memory. When FBANK value is '0', lower 64KB of non-volatile memory is used as shown in (a) of [Figure 13]. When FBANK value is '1', lower 32 KB and upper 32KB of non-volatile memory are used as shown in (b) of [Figure 13]. See the SFR section(7.1.4) for FBANK.

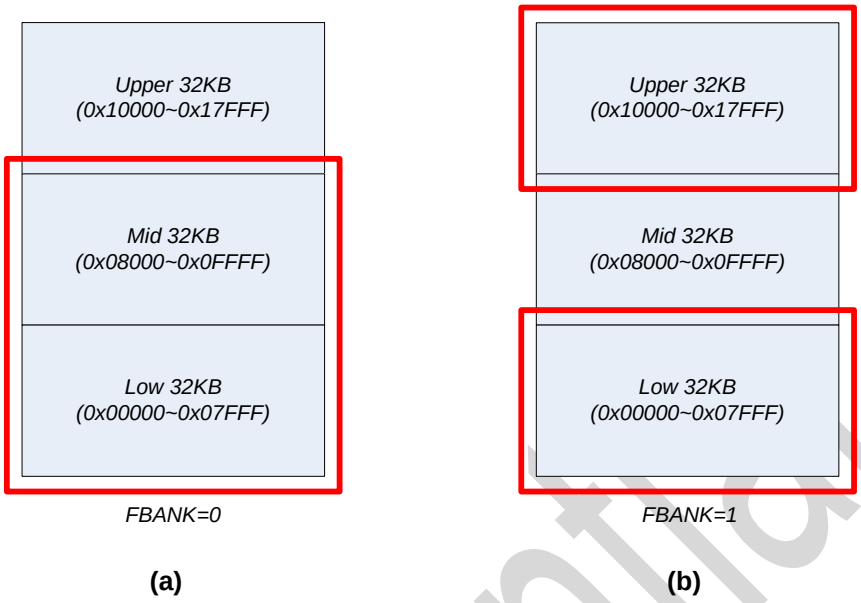


Figure 13. Bank Selection of Program Memory

The following table shows the address of code banking including Common area.

	MG245X		
Code Area	Start Addr	End Addr	Size
Common	0x00000	0x07FFF	32KB
BANK0	0x08000	0x0FFFF	32KB
BANK1	0x10000	0x17FFF	32KB
BANK2	-	-	-
BANK3	0x18000	0x18400	1KB
			97KB

7.1.2. DATA MEMORY

MG245X reserves 64 KB data memory address space. This address space can be accessed by MOVX command. [Figure 14] shows the address map of this data memory.

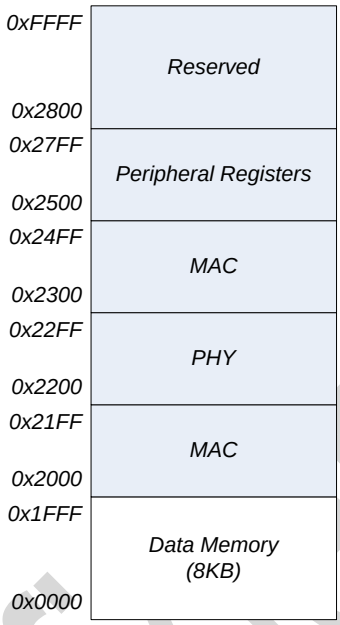


Figure 14. Address Map of Data Memory

The data memory used in the application programs resides in the address range of 0x0000-0x1FFF.

The registers and memory used in MAC block reside in the address range of 0x2000-0x21FF and 0x2300-0x24FF respectively. The registers to control or report the status of PHY block reside in the address range of 0x2200-0x22FF.

Registers related to the numerous peripheral functions of the embedded microprocessor reside in the address range of 0x2500-0x27FF.

7.1.3. GENERAL PURPOSE REGISTERS (GPR)

[Figure 15] describes the address map of the GPRs. GPRs can be addressed either directly or indirectly. As shown in the lower address space of [Figure 15], a bank consists of 8 registers.
The address space above the bank area is the bit addressable area, which is used as a flag by software or by a bit operation. The address space above the bit addressable area includes registers used as a general purpose of a byte unit. For the detailed information, refer to the below.

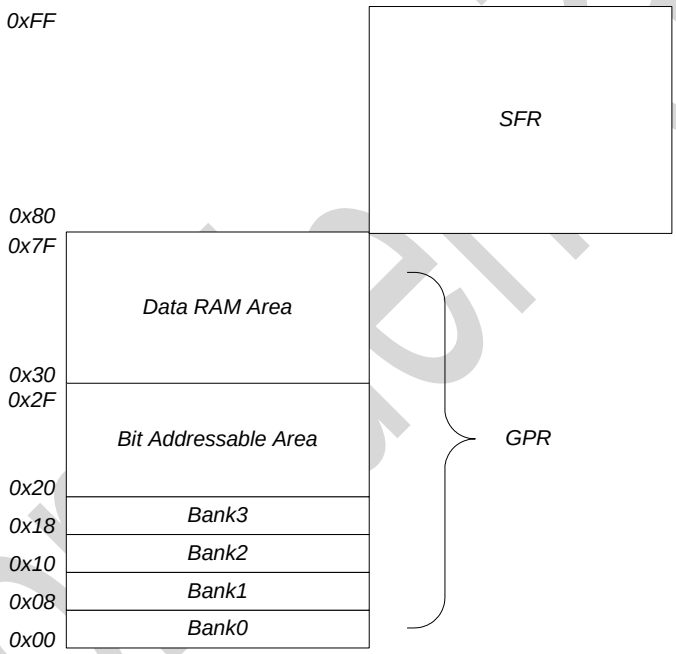


Figure 15. GPRs Address Map

Register Bank 0-3: It is located from 0x00 to 0x1F(32 bytes). One bank consists of each 8 registers out of 32 registers. Therefore, there are total 4 banks. Each bank should be selected by software as referring the RS field in PSW register. The bank(8 registers) selected by RS value can be accessed by a name(R0-R7) by software. After reset, the default value is set to bank0.

Bit Addressable Area: The address is assigned to each bit of 16 bytes(0x20~0x2F) and registers, which is the multiple of 8, in SFR. Each bit can be accessed by the address which is assigned to these bits. 128 bits(16 bytes,0x20~0x2F) can be accessed by direct addressing for each bit(0~127) and by a byte unit as using the address from 0x20~0x2F.

Data RAM Area: A user can use registers(0x30~0x7F) as a general purpose.

7.1.4. SPECIAL FUNCTION REGISTERS (SFR)

Generally, a register is used to store the data. MCU needs the memory to control the embedded hardware or the memory to show the hardware status. SFRs(Special Function Registers) process these functions described above. SFR includes the status or control of the I/O ports, the timer registers, the stack pointers and so on. [Table 5] shows the address to all SFRs in MG245X.

All SFRs are accessed by a byte unit. However, when SFR address is multiple of 8, it can be accessed by a bit unit.

Table 5. SFR (Special Function Register) Map

Register Name	SFR Address	B7	B6	B5	B4	B3	B2	B1	B0	Initial Value
EIP	0xF8		VCEIP	SPIIP	RTCIP	T3IP	AESIP	T2IP	RFIP	0x00
B	0xF0									0x00
EIE	0xE8		VCEIE	SPIIE	RTCIE	T3IE	AESIE	T2IE	RFIE	0x00
ACC	0xE0									0x00
EICON	0xD8					RTCIF				0x00
WDT	0xD2				WDTWE	WDTEN	WDTCLR	WDTPRE		0x0B
PSW	0xD0	CY	AC	F0	RS		OV	F1	P	0x00
WCON	0xC0						ISPMODE	ENROM		0x00
P3REN	0xBC									0x00
P1REN	0xBA									0x00
P0REN	0xB9									0x00

IP	0xB8		PS1		PS0	PT1	PX1	PT0	PX0	0x00
P3OEN	0xB4									0xFF
P1OEN	0xB2									0x7F
P0OEN	0xB1									0xFF
P3	0xB0									0x3F
TL3	0xAD									0x00
TL2	0xAC									0x00
TH3	0xAB									0x00
TH2	0xAA									0x00
T23CON	0xA9					TR3	M3	TR2	M2	0x00
IE	0xA8	EA	ES1		ES0	ET1	EX1	ET0	EX0	0x00
AUXR1	0xA2								DPS	0x00
FBANK	0xA1	RAM1	RAM0					FBANK		0x00
EXIF	0x91	T3IF	AESIF	T2IF	RFIF					0x00
P1	0x90									0xFF
TH1	0x8D									0x00
TH0	0x8C									0x00
TL1	0x8B									0x00
TL0	0x8A									0x00
TMOD	0x89	GATE1	CT1	M1		GATE0	CT0	M0		0x00
TCON	0x88	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0x00
PCON	0x87							PD	IDLE	0x00
P0SEL	0x85							ExNoEdge	P0AndSEL	0x00
P0MSK	0x84									0xFF
DPH	0x83									0x00
DPL	0x82									0x00
SP	0x81									0x07
P0	0x80									0xFF

The following section describes each SFR related to microprocessor.

Note 1: This table shows register bit conventions.

Symbol	Access Mode
RW	Read/write
RO	Read Only

WCON (WRITE CONTROL REGISTER, 0xC0)

This register can control the upper 1KB of program memory.

Bit	Name	Descriptions	R/W	Reset Value
7:3		Reserved		0
2	ISPMODE	ISP Mode Indication. When MS[1:0], an external pin, is '3', this field is set to 1 by hardware. It notifies the MCU whether ISPMODE or not.	RO	-
1	ENROM	When this field is '1', the upper 1KB (0xFC00~0xFFFF) is mapped to ROM. When this field is '0', the upper 1KB (0xFC00~0xFFFF) is mapped to non-volatile memory.	R/W	1
0		Reserved		0

FBANK (PROGRAM MEMORY BANK SELECTION REGISTER, 0xA1)

Bit	Name	Descriptions	R/W	Reset Value
7:1		Reserved		0x00
0	FBANK	Program Memory Bank Select. 0: Bank0 (Default) 1: Bank1 2: Not Used 3: Not Used	R/W	0

ACCUMULATOR(0xE0)

This register is marked as A or ACC and it is related to all the operations.

Bit	Name	Descriptions	R/W	Reset Value

7:0	A	Accumulator	R/W	0x00

B REGISTER(0xF0)

This register is used for a special purpose when multiplication and division are processed. For other instructions, it can be used as a general-purpose register. After multiplication is processed, this register contains the MSB data and 'A register' contains LSB data for multiplication result. In division operation, this register stores the value before division(dividend) and the remainder after division. At this time, before division, the divisor should be stored in 'A register' and result value(quotient) is stored in it after division.

Bit	Name	Descriptions	R/W	Reset Value
7:0	B	B register. Used in MUL/DIV instructions.	R/W	0x00

PROGRAM STATUS WORD (PSW, 0xD0)

This register stores the status of the program. The explanation of each bit is as follows.

Bit Field	Name	Descriptions	RW	Reset Value
7	CY	Carry flag	R/W	0
6	AC	Auxiliary carry flag	R/W	0
5	F0	Flag0. User-defined	R/W	0
4:3	RS	Register bank select. 0: Bank0 1: Bank1 2: Bank2 3: Bank3	R/W	0
2	OV	Overflow flag	R/W	0
1	F1	Flag1. User-defined	R/W	0
0	P	Parity flag. Set to 1 when the value in accumulator has odd number of '1' bits.	R/W	0

STACK POINTER(0x81)

When PUSH and CALL command is executed, some data (like the parameters by function call) are stored in stack to inform the values. In embedded MCU, the data memory area which can

be used for a general purpose(0x08~0x7F) is used as a stack area.

This register value is increased before the data is stored and the register value is decreased after the data is read when the data of stack is disappeared by POP and RET command. The default value is 0x07.

Bit Field	Name	Descriptions	RW	Reset Value
7:0	SP	Stack Pointer	R/W	0x07

DATA POINTER(DPH: 0x83, DPL: 0x82)

Data pointer consists of a high byte(DPH) and a low byte(DPL) to support 16-bit address. It can be accessed by 16-bit register or by two 8-bit registers respectively.

Bit Field	Name	Descriptions	RW	Reset Value
7:0	DPH	Data pointer, high byte	R/W	0x00

Bit Field	Name	Descriptions	RW	Reset Value
7:0	DPL	Data pointer, low byte	R/W	0x00

AUXR1 (AUXILIARY CONTROL REGISTER, 0xA2)

This register is used to implement Dual DPTR functions. Physically, DPTR consists of DPTR0 and DPTR1. However, DPTR0 and DPTR1 can be accessed depending on the DPS value of AUXR1 respectively. In other words, they cannot be accessed at the same time.

Bit Field	Name	Descriptions	RW	Reset Value
7:1		Reserved		0x00
0	DPS	Dual DPTR Select. This field is used to select either DPTR0 or DPTR1. When DPS is ‘0’, DPTR0 is selected. When DPS is ‘1’, DPTR1 is selected.	R/W	0

P3(0xB0)

This port register can be used by other functions besides general purpose I/O.

Bit Field	Name	Descriptions	R/W	Reset Value
7	P3.7 /PWM3 /CTS1 /SPICSN	This port register is used as general purpose I/O port.(12mA Drive) When Timer3 is operated as a PWM mode, it outputs PWM wave (PWM3) of Timer3. When port register is used as UART1, it is used as a CTS signal (CTS1) of UART1. When used as a Master mode, SPI Slave Select signal is outputted. When used as a Slave mode, this port register receives SPI Slave Select signal. This signal activate in low.	R/W	0
6	P3.6 /PWM2 /RTS1 /SPICLK	This port register is used as general purpose I/O port.(12mA Drive) When Timer2 is operated as a PWM mode, it outputs PWM wave (PWM2) of Timer2. When port register is used as UART1, it is used as a RTS signal (RTS1) of UART1. When used as a Master mode, SPI clock is outputted. When used as a Slave mode, this port register receives SPI clock.	R/W	0
5	P3.5 /T1 /CTS0 /SPIDO /QUADYB	This port register is used as general purpose I/O port. When Timer1 is operated as a COUNTER mode, it is operated as a counter input signal(T1) of Timer1. When port register is used as UART0, it is used as a CTS signal (CTS0) of UART0. In a Master mode or a Slave mode, this port register is used for outputting SPI data. When port register is used as QUAD function, it is used as the input signal of YB value.	R/W	1
4	P3.4 /T0	This port register is used as general purpose I/O port. When Timer0 is operated as a COUNTER mode, it is operated as a counter input signal(T0) of Timer0.	R/W	1

	/RTS0 /SPIDI /QUADYA	When port register is used as UART0, it is used as a RTS signal (RTS0) of UART0. In a Master mode or a Slave mode, this port register is used for receiving SPI data. When port register is used as QUAD function, it is used as the input signal of YA value.		
3	P3.3 /INT1	This port register is used as general purpose I/O port. When port register is used as an input signal, it can receive an external interrupt(INT1).	R/W	1
2	P3.2 /INT0	This port register is used as general purpose I/O port. When port register is used as a input signal, it can receive an external interrupt(INT0).	R/W	1
1	P3.1 /TXD0 /QUADXB	This port register is used as general purpose I/O port. When port register is used as UART0, it is used as a UART0 data output(TXD0). When port register is used as QUAD function, it is used as the input signal of XB value.	R/W	1
0	P3.0 /RXD0 /QUADXA	This port register is used as general purpose I/O port. When port register is used as UART0, it is used as a UART0 data input(RXD0). When port register is used as QUAD function, it is used as the input signal of XA value.	R/W	1

P1(0x90)

This port register can be used by other functions except general purpose I/O.

Bit Field	Name	Descriptions	R/W	Reset Value

7	P1.7 /P0AND /TRSW	This port register is used as a general purpose I/O port. When P0AndSel value in P0SEL register is set to '1', P1.7 outputs the result of bit-wise AND operation of (P0 OR P0MSK). It can be used as TRSW(RF TX/RX Indication signal) signal by setting PHY register.	R/W	1
6	P1.6 /TRSWB	This port register is used as general purpose I/O port. It can be used as TRSWB(TRSW Inversion signal) signal by setting the PHY register.	R/W	1
5	P1.5	This port register is used as general purpose I/O port.	R/W	1
4	P1.4 /QUADZB /STXTALI	This port register is used as a general purpose I/O port. When this port register is used as QUAD function, it is used as the input signal of ZB value. This port register is used as connecting to the external crystal(32.768KHz), which is used in the Sleep Timer, by setting the PHY register.	R/W	1
3	P1.3 /QUADZA /STXTALO /RTCLKO	This port register is used as a general purpose I/O port. When this port register is used as QUAD function, it is used as the input signal of ZA value. This port register is used for connecting to the external crystal(32.768KHz), which is used in the Sleep Timer, by setting the PHY register. This port register is used to output the internal RCOSC by setting the PHY register.	R/W	1
2	P1.2	This port register is used as a general purpose I/O port.	R/W	1
1	P1.1 /TXD1	This port register is used as a general purpose I/O port. When this port register is used as UART1, it is used as UART1 data output(TXD1).	R/W	1
0	P1.0 /RXD1	This port register is used as a general purpose I/O port. When this port register is used as UART1, it is	R/W	1

		used as UART1 data input(RXD1).		

P0(0x80)

This port register can be used as other functions besides general purpose I/O.

Bit Field	Name	Descriptions	R/W	Reset Value
7	P0.7 /I2STXMCLK	This port register is used as a general purpose I/O port. When this port register is used as I2S, it is operated as TX Master clock of I2S interface.	R/W	1
6	P0.6 /I2STXBCLK	This port register is used as a general purpose I/O port. When this port register is used as I2S, it is operated as TX Bit clock of I2S interface.	R/W	1
5	P0.5 /I2STXLRCK	This port register is used as a general purpose I/O port. When this port register is used as I2S, it is operated as TX LR clock of I2S interface.	R/W	1
4	P0.4 /I2STXDO	This port register is used as a general purpose I/O port. When this port register is used as I2S, it is operated as TX data output of I2S interface.	R/W	1
3	P0.3 /I2SRXMCLK	This port register is used as a general purpose I/O port. When this port register is used as I2S, it is operated as RX Master clock of I2S interface.	R/W	1
2	P0.2 /I2SRXBCLK	This port register is used as general purpose I/O port. When this port register is used as I2S, it is operated as RX Bit clock of I2S interface.	R/W	1
1	P0.1 /I2SRXLRCK	This port register is used as a general purpose I/O port. When this port register is used as I2S, it is operated as RX LR clock of I2S interface.	R/W	1
0	P0.0 /I2SRXDI	This port register is used as general purpose I/O port. When this port register is used as I2S, it is operated as RX data input of I2S interface.	R/W	1

P0OEN/P1OEN/P3OEN(0xB1, 0xB2, 0xB4)

P0OEN, P1OEN and P3OEN enable the output of port0,1 and 3. When each bit is cleared to '0', the output of the corresponding port is enabled. For example, when 4th bit of P1OEN is set to low, the output of port1.3 is enabled.

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	P3OEN	It controls the TX buffer function for each pin in Port3. When each bit field is set to '0', the TX buffer of the corresponding pin outputs the value.	R/W	0xFF

Bit Field	Name	Descriptions	R/W	Reset Value
7		Reserved		0
6:0	P1OEN	It controls the TX buffer function for each pin in Port1. When each bit field is set to '0', the TX buffer of the corresponding pin outputs the value.	R/W	0x7F

P1.7 only acts as output.

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	P0OEN	It controls the TX buffer function for each pin in Port0. When each bit field is set to '0', the TX buffer of the corresponding pin outputs the value.	R/W	0xFF

P0REN/P1REN/P3REN(0xB9, 0xBA, 0xBC)

P0REN, P1REN, P3REN enable Pull-up of port 0, 1 and 3. When each bit area is cleared to '0', the Pull-up of the corresponding port is enabled.

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	P3REN	It controls the Pull-up function for each pin in Port3. When each bit field is set to '0', the Pull-up function of the corresponding pin is operated.	R/W	0x00

Bit Field	Name	Descriptions	R/W	Reset Value
7		Reserved		0
6:0	P1REN	It controls the Pull-up function for each pin in Port1. When each bit field is set to '0', the Pull-up function of the corresponding pin is operated. **P1.7 doesn't have a control field because it is operated as an output.*	R/W	0x00

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	P0REN	It controls the Pull-up function for each pin in Port0. When each bit field is set to '0', the Pull-up function of the corresponding pin is operated.	R/W	0x00

P0MSK (P0 INPUT MASK REGISTER, 0x84)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	P0MSK	This register is used for masking the input of P0 pin(Refer to P0AndSel in P0SEL register).	R/W	0xFF

P0SEL (P0 INPUT SELECTION REGISTER, 0x85)

Bit Field	Name	Descriptions	R/W	Reset Value
7:2		Reserved		0
1	ExNoEdge	This field controls the wake up of the MCU by an external interrupt when in power-down mode. When this field is '0', the MCU wakes up when INT0 or INT1 signal is high(This is the normal case in the MCU.) When this field is '1', the MCU is woken up by wakeup signal of Sleep Timer. Remote control function can be implemented by the interrupt service routine of the MCU when the WAKEUP signal occurs by adjusting RTDLY value in the Sleep Timer while either INT0 or INT1 is low.	R/W	0
0	P0AndSel	When this field is set to '1', P0 and P0MSK are ORed per bit. The bits of the result value are to be ANDed and then output to P1.7. This	R/W	0

		function is used to implement remote control function.		

7.2. RESET

MG245X shall be reset to be operated. There are three kinds of reset sources. The first one is to use an external reset pin(RESET#). When applying a low signal to this pin more than 1ms, MG245X is reset. Second, MG245X can be reset by an internal POR when it is powered up as using the internal Power-On-Reset(POR) block. Third, as a reset by the watchdog timer, a reset signal is generated when the internal counter of watchdog timer reaches a pre-set value.

Parameter	MIN	TYP	MAX	UNIT
POR Specifications				
1.5V POR Release		1.18		V
1.5V POR Hysteresis		0.11		V

For more detailed information, refer to **[MG245X ERRATA NOTES-002] RESET ERRATA** document.

7.3. CLOCK SOURCE

MG245X can use 16MHz or 19.2MHz crystal as system clock source. An external 32.768KHz crystal or internal clock generated from internal RCOSC is used for the Sleep Timer clock.

For the internal 8051 MCU Clock in MG245X, either 8MHz or 16MHz can be used. When selecting 8051 MCU Clock(8MHz, 16MHz), CLKDIV0 register should be set as follows.

CLKDIV0 (OPERATING FREQUENCY CONTROL REGISTER, 0x22C3)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CLKDIV0	This register is used to control the clock of the internal 8051 MCU. When this register is set to 0xFF, the clock is set to 8MHz; when set to 0x00, the clock is set to 16MHz. All other values except 0xFF and 0x00 are reserved.	R/W	0xFF

7.4. INTERRUPT SCHEME

The program interrupt functions of the embedded MCU are similar to other microprocessors. When the interrupt occurs, the interrupt service routine at the corresponding vector address is executed. When the interrupt service routine process is completed, the program is resumed from the point of time at which interrupt occurred. Interrupts can be initiated from the internal operation of the embedded microprocessor (e.g. the overflow of timer count) or from an external signal.

MG245X has 13 interrupt sources. The following [Table 6] describes the detailed information for the interrupt sources. The 'Interrupt Address' indicates the address where the interrupt service routine is located. The 'Interrupt Flag' is the bit that notifies the MCU that the corresponding interrupt has occurred. 'Interrupt Enable' is the bit which decides whether each interrupt has been enabled. 'Interrupt Priority' is the bit which decides the priority of the interrupt. 'Interrupt Number' is the interrupt priority fixed by the hardware. That is, when two or more interrupts having the same 'Interrupt Priority' value, occur simultaneously, the lower 'Interrupt Number' is processed first.

Table 6. Interrupt Descriptions

Interrupt Number	Interrupt Type	Interrupt Address	Interrupt Flag	Interrupt Enable	Interrupt Priority
0	External Interrupt0	0003H	TCON.IE0	IE.EX0	IP.PX0
1	Timer0 Interrupt	000BH	TCON.TF0	IE.ET0	IP.PT0
2	External Interrupt1	0013H	TCON.IE1	IE.EX1	IP.PX1
3	Timer1 Interrupt	001BH	TCON.TF1	IE.ET1	IP.PT1
4	UART0 Interrupt (TX) UART0 Interrupt (RX)	0023H	Refer to Note1	IE.ES0	IP.PS0
7	UART1Interrupt (TX) UART1 Interrupt (RX)	003BH	Refer to Note1	IE.ES1	IP.PS1
8	PHY Interrupt	0043H	EXIF.PHYIF	EIE.RFIE	EIP.RFIP
9	Timer2 Interrupt	004BH	EXIF.T2IF	EIE.T2IE	EIP.T2IP
10	AES Interrupt	0053H	EXIF.AESIF	EIE.AESIE	EIP.AESIP
11	Timer3 Interrupt	005BH	EXIF.T3IF	EIE.T3IE	EIP.T3IP
12	Sleep Timer Interrupt	0063H	EICON.RTCIF	EIE.RTCIE	EIP.RTCIP

13	SPI Interrupt	0068H	Refer to Note2	EIE.SPIIE	EIP.SPIIP
14	Voice Interrupt	0073H	Refer to Note3	EIE.VCEIE	EIP.VCEIP

Note 1: *In case of a UART Interrupt, bit[0] of IIR register(0x2502,0x2512) in the UART block is used as a flag. Also, the Tx, Rx, Timeout, Line Status and Modem Status interrupts can be distinguished by bit[3:1] value. For more detailed information, refer to the UART0/1description in Section 7.6.6t.*

Note 2: *In case of an SPI interrupt, there is another interrupt enable bit in the SPI register besides EIE.SPIIE. In order to enable SPI interrupt, both SPIE in SPCR(0x2540) register and EIE.SPIIE should be set to '1'. And SPIF in SPSR(0x2541) register acts as an interrupt flag.*

Note 3: *In case of Voice interrupt, there are interrupt enable register and interrupt flag register in voice block. The interrupt enable register are VTFINTENA(0x2770), VRFINTENA(0x2771) and VDMINTENA(0x2772). There are 24 interrupt sources. When both an interrupt enable signal and an interrupt flag signal are set to '1,' voice interrupt is enabled.*

IE (INTERRUPT ENABLE REGISTER, 0xA8)

The EA bit in IE register is the global interrupt enable signal for all interrupts. In addition, each interrupt is masked by each interrupt enable bit. Therefore, in order to use an interrupt, both EA and the specific interrupt enable bit should be set to '1'. When the bit for each interrupt is '0', that interrupt is disabled. When the bit for each interrupt is '1', that interrupt is enabled.

Bit Field	Name	Descriptions	R/W	Reset Value
7	EA	Global interrupt enable 0: No interrupt will be acknowledged. 1: Each interrupt source is individually enabled or disabled by setting its corresponding enable bit.	R/W	0
6	ES1	UART1 interrupt enable 1: interrupt enabled. (EA bit should be set to '1')	R/W	0
5		Reserved		0
4	ES0	UART0 interrupt enable 1: interrupt enabled. (EA bit should be set to '1')	R/W	0
3	ET1	Timer1 interrupt enable 1: interrupt enabled. (EA bit should be set to '1')	R/W	0
2	EX1	External interrupt1 enable 1: interrupt enabled. (EA bit should be set to '1')	R/W	0
1	ET0	Timer0 interrupt enable 1: interrupt enabled. (EA bit should be set to '1')	R/W	0
0	EX0	External interrupt0 enable 1: interrupt enabled. (EA bit should be set to '1')	R/W	0

IP (INTERRUPT PRIORITY REGISTER, 0xB8)

If a bit corresponding to each interrupt is '0', the corresponding interrupt has lower priority and if a bit is '1', the corresponding interrupt has higher priority.

Bit Field	Name	Descriptions	R/W	Reset Value
7		Reserved		0
6	PS1	UART1 interrupt priority 1: UART1 interrupt has higher priority.	R/W	0
5		Reserved		0
4	PS0	UART 0 interrupt priority 1: UART0 interrupt has higher priority.	R/W	0
3	PT1	Timer1 interrupt priority 1: Timer1 interrupt has higher priority.	R/W	0
2	PX1	External interrupt1 interrupt priority 1: Interrupt of external interrupt1 has a higher priority.	R/W	0
1	PT0	Timer0 interrupt priority 1: Timer0 interrupt has higher priority.	R/W	0
0	PX0	External interrupt0 interrupt priority 1: Interrupt of external interrupt0 has a higher priority.	R/W	0

EIE (EXTENDED INTERRUPT ENABLE REGISTER, 0xE8)

If a bit is '0', corresponding interrupt is disabled and if a bit is '1', corresponding interrupt is enabled. Refer to the following table.

Bit Field	Name	Descriptions	R/W	Reset Value
7		Reserved	R/W	0
6	VCEIE	Voice Interrupt Enable. 0: interrupt disabled 1: interrupt enabled	R/W	0
5	SPIIE	SPI Interrupt Enable 0: interrupt disabled 1: interrupt enabled	R/W	0
4	RTCIE	Sleep Timer Interrupt Enable	R/W	0

		0: interrupt disabled 1: interrupt enabled		
3	T3IE	Timer3 Interrupt Enable 0: interrupt disabled 1: interrupt enabled	R/W	0
2	AESIE	AES Interrupt Enable 0: interrupt disabled 1: interrupt enabled	R/W	0
1	T2IE	Timer2 Interrupt Enable 0: interrupt disabled 1: interrupt enabled	R/W	0
0	RFIE	RF Interrupt Enable 0: interrupt disabled 1: interrupt enabled	R/W	0

EIP (EXTENDED INTERRUPT PRIORITY REGISTER, 0xF8)

If a bit is '0', the corresponding interrupt has lower priority. If a bit is '1', the corresponding interrupt has higher priority.

Bit Field	Name	Descriptions	R/W	Reset Value
7		Reserved		0
6	VCEIP	Voice Interrupt Priority 1: voice interrupt has higher priority. 0: voice interrupt has lower priority.	R/W	0
5	SPIIP	SPI Interrupt Priority 1:SPI interrupt has higher priority. 0:SPI interrupt has lower priority.	R/W	0
4	RTCIP	Sleep Timer Interrupt Priority 1: Sleep Timer interrupt has higher priority. 0: Sleep Timer interrupt has lower priority.	R/W	0
3	T3IP	Timer3 Interrupt Priority 1: Timer3 interrupt has higher priority. 0: Timer3 interrupt has lower priority.	R/W	0
2	AESIP	AES Interrupt Priority 1: AES interrupt has higher priority. 0: AES interrupt has lower priority.	R/W	0

1	T2IP	Timer2 Interrupt Priority 1: Timer2 interrupt has higher priority. 0: Timer2 interrupt has lower priority.	R/W	0
0	RFIP	RF Interrupt Priority 1: RF interrupt has higher priority. 0: RF interrupt has lower priority.	R/W	0

EXIF (EXTENDED INTERRUPT FLAG REGISTER, 0x91)

This register stores the interrupt state corresponding to each bit. When the interrupt corresponding to a bit is triggered, the flag is set to '1'.

Bit Field	Name	Descriptions	R/W	Reset Value
7	T3IF	Timer3 Interrupt Flag. 1: Interrupt pending	R/W	0
6	AESIF	AES Interrupt Flag. 1: Interrupt pending	R/W	0
5	T2IF	Timer2 Interrupt Flag. 1: Interrupt pending	R/W	0
4	RFIF	RF Interrupt Flag. 1: Interrupt pending	R/W	0
3:0		Reserved		0

EICON (EXTENDED INTERRUPT CONTROL REGISTER, 0xD8)

Bit Field	Name	Descriptions	R/W	Reset Value
7		Reserved		0
6:4		Reserved		0
3	RTCIF	Sleep Timer Interrupt Flag. 1: Interrupt pending	R/W	0
2:0		Reserved		0

7.5. POWER MANAGEMENT

MG245X has four operation modes as shown in the following table. PM0 is the normal operating mode. The other 3 modes, PM1/PM2/PM3, are called power modes. The power modes can be set by PDMODE[1:0] bits in PDCON(0x22F1) register. After setting PDMODE, each power mode can be started by making PDSTART bit to 1. Each mode has different current consumption and different wake-up sources. Following table describes the normal mode and three power modes.

PDMODE[1:0]	Description	Wake-up Sources	Regulator for Digital Block	Current Consumption (Typ.)
0	PM0 mode (Normal mode)	-	-	-
1	PM1 mode (Power mode)	Hardware Reset, Sleep Timer interrupt, External interrupt	ON	25μA
2	PM2 mode (Power mode)	Hardware Reset, Sleep Timer interrupt, External interrupt	OFF (After wake-up, register configuration is required)	<2μA
3	PM3 mode (Power mode)	Hardware Reset, External interrupt	OFF (After wake-up, register configuration is required)	0.3μA

The following describes the time it takes from power mode to system operation for each of the wake-up sources.

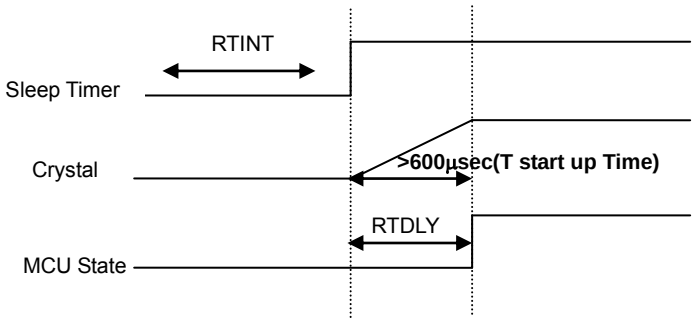
① Wake-up by Hardware

The wake-up time in PM1, PM2 and PM3 is around 1001μsec. For more detailed information, refer to the [Figure 33] below.

② Wake-up by Sleep Timer Interrupt

The following shows the time of Sleep Timer Interrupt Wake Up. As shown in below, the wake-up time is decided by the register value of RTINT and RTDLY. RTDLY should

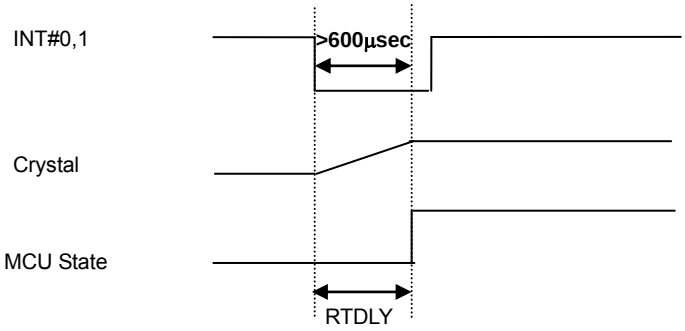
be set over '0x11' at least to stabilize crystal. In case of PM1 and PM2, the minimum wake-up time is around 534μsec (RTINT:0x01, RTDLY:0x11).



Based on the Radio Pulse's reference circuit.

③ Wake-up by External Interrupt

The following shows the time of External Interrupt Wake Up. The wake-up time can be different based on the releasing time of external interrupt (that is, rising edge of external interrupt signal in the below figure). Thus, it is recommended to set RTDLY to over 600μsec at least to make the crystal be stabilized.



Based on the Radio Pulse's reference circuit.

The following table describes the status of voltage regulator, oscillator, and sleep timer in each power mode.

Power Mode	AVREG	DVREG	Main OSC	Sleep Timer
PM0	ON	ON	ON	ON
PM1	OFF	ON	OFF	ON
PM2	OFF	OFF	OFF	ON
PM3	OFF	OFF	OFF	OFF

Table 7. Power Mode

When exiting from a power mode, RTDLY(0x22F4) register specifies the delay time for oscillator stabilization. If the delay time is too short, the oscillator can be unstable and it can cause a problem to fetch a wrong instruction command in the MCU.

In addition, there are two power-saving modes that can be only used in the MCU. One is PD(Power-Down) mode and the other is IDLE mode. PD(Power-Down) mode of MCU is enabled by setting PD in PCON register to '1'. In PD(Power-Down) mode, all the clocks of MCU are stopped and current consumption is minimized. When interrupts, which is allowed for wake-up, occurs, it exits from PD mode. After exiting, the corresponding interrupt service routine is executed. And then, the next instruction after the instruction for setting PD to '1' is executed. In IDLE mode, clocks of all the blocks in the MCU except peripherals are stopped. The current consumption of MCU in IDLE mode is about 2.7mA. When an interrupt occurs (except a timer interrupt and external interrupt) the IDLE bit is cleared and the device exits from IDLE mode. The required interrupt service routine is then executed and the next instruction (after the instruction for setting IDLE to '1') is executed.

PCON (POWER CONTROL REGISTER, 0x87)

Bit Field	Name	Descriptions	R/W	Reset Value
7:2		Reserved		0
1	PD	MCU Power-down Mode. When this field is set to '1', all the clocks in MCU are stopped.	R/W	0
0	IDLE	MCU Idle Mode. When this field is set to '1', all the clocks in MCU except peripherals are stopped. Only peripheral operates normally.	R/W	0

When MG245X goes into a power mode by setting PDSTART field of PDM register, the PD bit of PCON register should also be set. The procedure is shown in the [Figure 16].

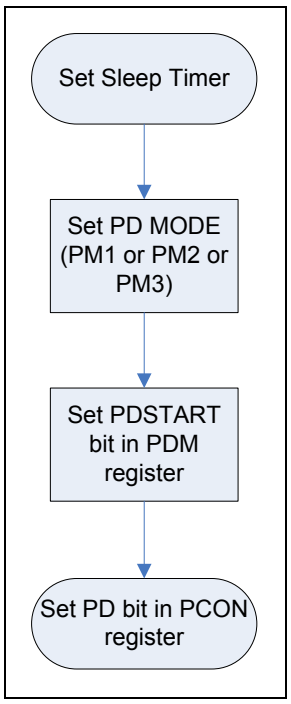


Figure 16. Power mode setting procedure

PDM (POWER DOWN REGISTER, 0x22F0)

It controls Register which is used for operation of 1.5V/1.8V Voltage Regulator, Polarity controlling of external Interrupt, and power down of MG245X.

Bit Field	Name	Descriptions	R/W	Reset Value
7:6	RSVD	Reserved		0x00
5	INT0_POLH	It decides polarity of external interrupt. 0: Recognizes low level as interrupt signal. 1: Recognizes high level as interrupt signal.	R/W	0
4	INT1_POLH	It decides polarity of external interrupt. 0: Recognizes low level as interrupt signal. 1: Recognizes high level as interrupt signal.	R/W	0
3:1	RSVD	Reserved		0x00
0	PDSTART	Power Down Start signal. When '1' is written, it is automatically cleared after 2 cycles, goes into Power Down.	R/W	0

PDCON (POWER DOWN CONTROL REGISTER, 0x22F1)

It controls AVREG, operation of AVREG_OK, and block regarding Power down mode.

Bit Field	Name	Descriptions	R/W	Reset Value
7	AVREGEN	It controls Voltage regulator in Analog part. 0: Disables VREG in Analog part. 1: Enables VREG in Analog part.	R/W	1
6	AVREGOKEN	It decides on/off for monitoring voltage level of voltage regulator in Analog part. When voltage level of VREG_OUT exceeds 1.26V, it's flagged to high. 0: AVREGOK block off. 1: AVREGOK block on.	R/W	1
5	AVREG_OK	When AVREGOKEN is '1', if voltage level of VREG_OUT exceeds 1.26V, it's flagged to high.	R/O	0
4	STEN	Register for controlling Sleep timer. When STEN is high, internal Sleep timer operates by RCOSC or external XTAL. 0: Disables Sleep timer. 1: Enables Sleep timer.	R/W	0
3	RCOSCEN	It decides oscillation of internal RCOSC. 0: Disables RCOSC. (RCOSC output is maintained as '0'.) 1: Enables RCOSC.	R/W	1
2	DBODEN	It enables brown out detector, when DVDD falls under certain voltage(900mV approximately), resets Digital core. DBODEN='0': Disables Brown out detector. DBODEN='1': Enables Brown out detector.	R/W	0
1:0	PDMODE[1:0]	Register for power down mode of MG245X. When "00", it's PM0, and when "01", "10", "11", it's PM1, PM2, PM3 in order.(Refer to Table 5.)	R/W	0xC8

7.6. ON-CHIP PERIPHERALS

On-chips peripherals in MG245X are as follows.

- TIMER 0/1
- TIMER 2/3, PWM 2/3
- Watch-dog timer
- Sleep Timer
- Internal RC Oscillator for Sleep Timer
- Two High-Speed UARTs with Two 16-byte FIFOs (up to 1Mbps)
- SPI Master/Slave Interface
- I2S/PCM Interface with two 128-byte FIFOs
- μ-law / a-law / ADPCM Voice Codec
- Random Number Generator
- Quad Decoder
- Internal Voltage Regulator
- 4-channel 8-bit sensor ADC
- On-chip Power-on-Reset
- Temperature Sensor
- Battery Monitoring

7.6.1. TIMER 0/1

The Embedded MCU has two 16-bit timers which are compatible with Intel 8051 MCU(Timer0, Timer1). These timers have 2 modes; one is operated as a timer and the other is operated as a counter. When it is operated as a timer, there are 4 operating modes.
Each timer is 16-bit timer and consists of two 8-bit register. Therefore, the counter can be either 8-bit or 16-bit set by the operating mode.

In counter mode, the input signal T0(P3.4) and T1(P3.5) are sampled once every 12 cycles of the system clock. If the sampled value is changed from ‘1’ to ‘0’, the internal counter is incremented. In this time, the duty cycle of T0 and T1 doesn’t affect the increment. Timer0 and Timer1 are accessed by using 6 SFR’s.

The following table describes timer register and mode.

TCON (TIMER CONTROL REGISTER, 0x88)

This register is used to control a timer function and monitor a timer status.

Bit Field	Name	Descriptions	R/W	Reset Value
7	TF1	Timer1 Overflow Flag. When this field is '1', a Timer1 interrupt occurs. After the Timer1 interrupt service routine is executed, this field value is cleared by hardware.	R/W	0
6	TR1	Timer1 Run Control. When this bit is set to '1', Timer1 is enabled.	R/W	0
5	TF0	Timer0 Interrupt Flag. 1: Interrupt is pending After Timer0 interrupt service routine is executed, this field is cleared by hardware.	R/W	0
4	TR0	Timer0 Run When this bit is set to '1', Timer0 is enabled.	R/W	0
3	IE1	External Interrupt1 Edge Flag. When this field is '1', External interrupt1 is pending. After the interrupt service routine is executed, this field is cleared by hardware.	R/W	0
2	IT1	External Interrupt1 Type Control. This field specifies the type of External interrupt1. 1=Edge type. When the falling edge of INT1 is detected, the interrupt occurs. 0=Level type. When INT1 is low level, the interrupt occurs.	R/W	0
1	IE0	External Interrupt0 Edge Flag. When this field is '1', External interrupt0 is pending. After the interrupt service routine is executed, this field is cleared by hardware.	R/W	0
0	IT0	External Interrupt0 Type Control. This field specifies the type of External interrupt1. 1=Edge type. When the falling edge of INT1 is detected, the interrupt occurs. 0=Level type. When INT0 is low level, the interrupt occurs.	R/W	0

TMOD (TIMER MODE CONTROL REGISTER, 0x89)

Bit Field	Name	Descriptions	R/W	Reset Value
7	GATE1	Timer Gate Control When TR1 is set to '1' and GATE1 is '1', Timer1 is enabled while INT1 pin is in high. When GATE1 is set to '0' and TR1 is set to '1', Timer1 is enabled.	R/W	0
6	CT1	Timer1 Counter Mode Select When this field is set to '1', Timer1 is enabled as counter mode.	R/W	0
5:4	M1	Timer1 mode select 0: Mode0, 12-bit Timer 1: Mode1, 16-bit Timer 2: Mode2, 8-bit Timer with auto-load 3: Mode3, two 8-bit Timers	R/W	0
3	GATE0	Timer0 Gate Control When TR0 is set to '1' and GATE0 is '1', Timer0 is enabled while INT0 pin is in high. When GATE1 is set to '0' and TR1 is set to '1', Timer0 is enabled.	R/W	0
2	CT0	When this field is set to '1', Timer0 is enabled as counter mode.	R/W	0
1:0	M0	Timer0 mode select 0: Mode0, 12-bit Timer 1: Mode1, 16-bit Timer 2: Mode2, 8-bit Timer with auto-load 3: Mode3, two 8-bit Timers	R/W	0

TL0/TL1/TH0/TH1 (TIMER REGISTERS,0x8A, 0x8B, ,0x8C, 0x8D)

A pair of register, which are (TH0, TL0) and (TH1, TL1), can be used as 16-bit timer register for Timer0 and Timer1 and it can be used as 8-bit register respectively.

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	TH1	Timer1 High Byte Data	R/W	0x00

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	TH0	Timer0 High Byte Data	R/W	0x00

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	TL1	Timer1 Low Byte Data	R/W	0x00

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	TL0	Timer0 Low Byte Data	R/W	0x00

In mode0, 12-bit register of timer0 consists of 7-bit of TH0 and lower 5-bit of TL0. The higher 1-bit of TH0 and higher 3-bit of TL0 are disregarded. When this 12-bit register is overflowed, set TF0 to ‘1’. The operation of timer1 is same as that of timer0.

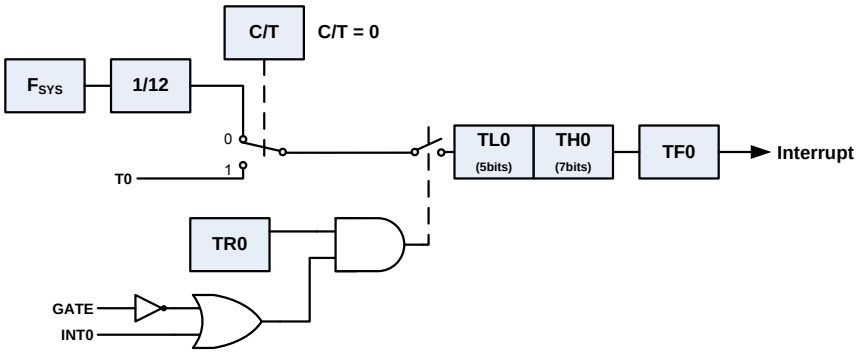


Figure 17. Timer0 Mode0

In Mode1, the operation is same as it of Mode0 except all timer registers are enabled as a 16-bit counter.

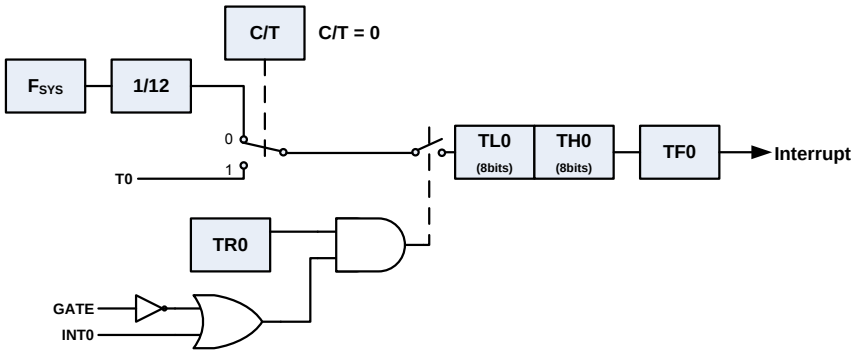


Figure 18. Timer0 Mode1

In mode2, TL0 of Timer0 is enabled as an 8-bit counter and TH0 automatically reloads TL0. TF0 is set to '1' by overflowing of TL0. TH0 value retains the previous value regardless of the reloading. The operation of Timer1 is same as that of Timer0.

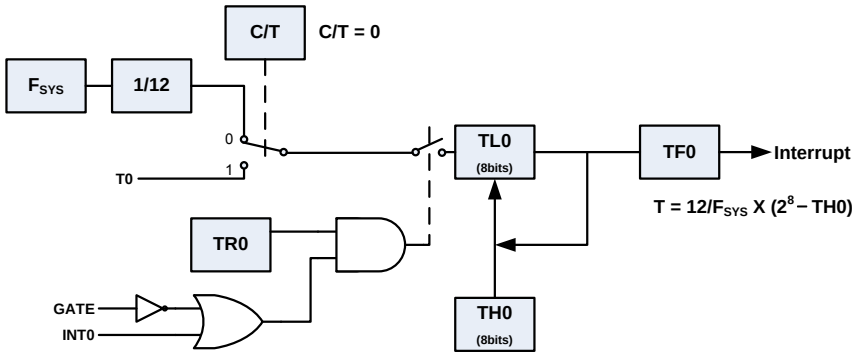


Figure 19. Timer0 Mode2

In Mode3, Timer0 uses TL0 and TH0 as an 8-bit timer respectively. In other words, it uses two counters. TL0 controls as the control signals of Timer0. TH0 is always used as a timer function and it controls as TR1 of Timer1. The overflow is stored in TF1. At this time, Timer1 is disabled and it retains the previous value.

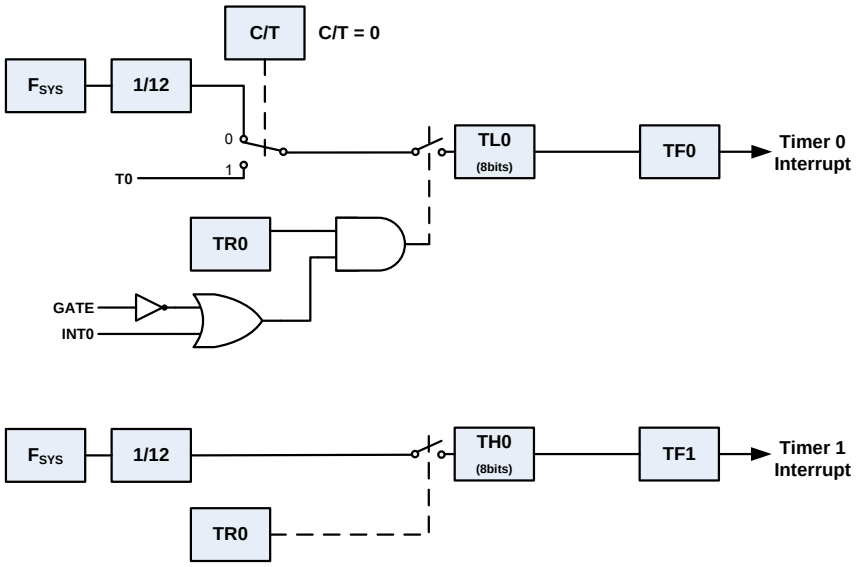


Figure 20. Timer0 Mode3

7.6.2. TIMER 2/3, PWM 2/3

TIMER 2/3

The embedded MCU includes two 16-bit timers(Timer2 and Timer3).

T23CON (TIMER2/3 CONTROL REGISTER, 0xA9)

This register is used to control Timer2 and Time3.

Bit Field	Name	Descriptions	R/W	Reset Value
7:4		Reserved	R/W	0
3	TR3	Timer3 Run. When this field is set to '1', Timer3 is operated.	R/W	0
2	M3	Timer3 PWM Mode. When this field is set to '1', Timer3 acts as PWM mode.	R/W	0
1	TR2	Timer2 Run. When this field is set to '1', Timer2 is operated.	R/W	0
0	M2	Timer3 PWM Mode. When this field is set to '1', Timer3 acts as PWM mode.	R/W	0

TL2/TL3/TH2/TH3 (TIMER2/3 TIMER REGISTER, 0xAC, 0xAD, 0xAA, 0xAB)

Register (TH2, TL2) and (TH3, TL3) are 16-bit timer counter register for Timer2 and Timer3.

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	TL3	Timer3 Low Byte Data	R/W	0x00

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	TL2	Timer2 Low Byte Data	R/W	0x00

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	TH3	Timer3 High Byte Data	R/W	0x00

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	TH2	Timer2 High Byte Data	R/W	0x00

Timer2 acts as a general 16-bit timer. Time-out period is calculated by the following equation.

$$T_2 = \frac{8 \times (256 \times TH2 + TL2 + 1)}{fsystem}$$

If the time-out period is set too short, excessive interrupt occur causing abnormal operation of the system. It is recommended to set sufficient time-out period for Timer2(over 100μs).

Timer3 acts as a general 16-bit timer. Time-out period of Timer3 is calculated by the following equation.

$$T_3 = \frac{3 \times (256 \times TH3 + TL3 + 1)}{fsystem}$$

If the time-out period is set too short, excessive interrupt occur causing abnormal operation of the system. It is recommended to set a sufficient time-out period of Timer3.

PWM 2/3

TIMER 2/3 can be used as Pulse Width Modulators, PWM2 and PWM3 respectively based on setting the M2, M3 bits in T23CON register. P 3.6 outputs PWM2 signal and P3.7 outputs PWM3 signal.

The following table describes the frequency and High Level Duty Rate in PWM mode.

Channel	Frequency (Hz)	High Level Duty Rate (%)
PWM2	$\frac{fsystem}{256\times(TH2+1)}$	$\frac{TL2}{256}\times 100$
PWM3	$\frac{fsystem}{256\times(TH3+1)}$	$\frac{TL3}{256}\times 100$

Note 4: *The following is not applied for the frequency of equation described above.*

-TH=0: Acts as 15.625 KHz.

-TH=1: Acts as 7.812 KHz.

7.6.3. WATCHDOG TIMER

The Watchdog Timer (WDT) monitors whether the MCU is or is not operating normally. If a problem occurs, the WDT will immediately reset the MCU.

In fact, when the system does not clear the WDT counter value, WDT considers that a problem has occurred, and therefore, resets the MCU automatically. The WDT is used when a program is not completed normally because a software error has been caused by the environment such as electrical noise, unstable power or static electricity.

When Powered-up, the internal counter value of WDT is set to '0' and watchdog timer is operated. If overflow is caused in the internal counter, a system reset is initiated with a timeout period is about 0.5 second. A user may reset the WDT by clearing WDTEN bit of WDTCON. When WDT operates, an application program must clear the WDT periodically to prevent the system from being reset accidentally.

WDTCON (WATCHDOG TIMER CONTROL REGISTER, 0xD2)

Bit Field	Name	Descriptions	R/W	Reset Value
7:5		Reserved	R/W	0
4	WDTWE	WDT Write Enable. To set WDTEN to '0' or '1', this field should be set to '1'. If this field is '0', it is impossible to change WDTEN to '0'.	R/W	0

3	WDTEN	WDT Enable. To use WDT, this bit should be set to '1'.	R/W	1
2	WDTCLR	WDT Clear. Watchdog Timer resets a system when the internal counter value is reached to the defined value by WDTPRE value. This field does not allow system to be reset by clearing the internal counter. When this field is set to '1', this field value is cleared automatically.	R/W	0
1:0	WDTPRE	Watchdog Timer Prescaler. Sets the prescale value of WDT.	R/W	11

Reset interval of WDT is calculated by the following equation. For example, when WDTPRE value is '0' and system clock of MCU is 8MHz, reset interval of WDT is 65.536ms.

$$\text{Watchdog Reset Interval} = \frac{256 \times 2^{(11+WDTPRE)}}{f_{system}}$$

7.6.4. SLEEP TIMER

Sleep Timer can generate time interval such as 1 or 2 seconds with internal or external real-time clocks sources. Sleep Timer(ST) is used to exit from the Power-Down mode.

The clock source desired can be generated from an external crystal or the internal RC oscillator. ST is activated as setting STEN bit in PDCON to '1' and the interrupt interval can be programmed by setting RTCON[6:0], RTINT1 and RTINT0 register.

RTCON (SLEEP TIMER CONTROL REGISTER, 0x22F5)

Bit Field	Name	Descriptions	R/W	Reset Value
7	RTCSEL	Sleep Timer Select. When this field is set to '1', internal RCOSC is used as a clock source. When this field is set to '0', external 32.768KHz crystal is used as a clock source. When this field is set to '0' and external crystal is not turned on, ST does not act.	R/W	1
6:0	RTINT[22:16]	This field determines the ST interrupt interval with RTINT0 and RTINT1	R/W	0x00

RTINT1 (SLEEP TIMER INTERRUPT INTERVAL 1, 0x22F6)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	RTINT[15:8]	This field determines ST interrupt interval with RTINT0 and RTCON[6:0]	R/W	0x00

RTINT0 (SLEEP TIMER INTERRUPT INTERVAL 0, 0x22F7)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	RTINT[7:0]	This field determines ST interrupt interval with RTINT1 and RTCON[6:0]	R/W	0x08

Sleep Timer Interrupt Interval

RTCON[6:0], RTINT1 and RTINT0 register represent RTINT[22:0](23-bit) and the timer interval is determined by this value. If ST clock source acts as 32.786KHz, one ST cycle is 1/32768 second and the timer interval is RTINT * (1/32768) second. Therefore, ST interrupt occurs per (RTINT * 30.5)μs and maximum is 256 second.

RTDLY (SLEEP TIMER DELAY REGISTER, 0x22F4)

This register is used when MG245X exits from a power mode.

RTDLY specifies the delay time for oscillator stabilization. When MG245X exits from a power mode, MCU executes the instruction after the delay time.

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	RTDLY	Delay Time = RTDLY / 32.768KHz when ST clock source is 32.768KHz. The value of RTDLY should be greater than 11.	R/W	0x02

Note : When using ST(Sleep Timer), system cannot have regular cycle because there are much errors of time to be woken up. Therefore, it is recommended to use external RTC for the application which needs accurate timing.(When using external RTC, electricity consumption is increasing according to external RTC and circuits.)

7.6.5. INTERNAL RC OSCILLATOR

Internal RC oscillator generates the internal clock and provides the clock to Sleep Timer block in the embedded MCU. The Internal RC oscillator can be controlled by 3rd bit in the PDCON(0x22F1) register. When this bit is set to '1', internal RC Oscillator is enabled. The default value is '1'.

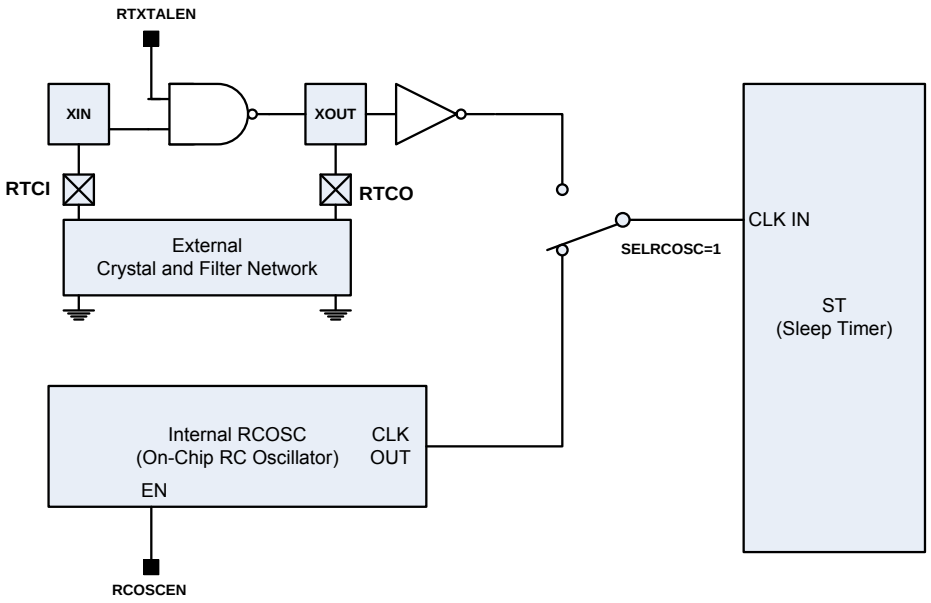


Figure 21. Internal RCOSC

RCOSC1 (RCOSC1 REGISTER, 0x22F2)

It sets Register regarding OSCBUFFER and RCC of RCOSC.

Bit Field	Name	Descriptions	R/W	Reset Value
7	RCCEN	It enables or disables RC calculation(RCC) block in RCOSC block. 0: Disables RCC block. 1: Enables RCC block.	R/W	0
6	SELRTXTAL	It selects XTAL32kHz and internal RCOSC. 0: Disables External XTAL32k. 1: Enables External XTAL32k.	R/W	0
5:4	RSVD	Reserved		0x37
3	OSC_OK	Stabilization monitoring Register. When OSCLK is stabilized, OSC_OK signal is set	R/O	0

		as high.		
2:0	RSVD	Reserved		0x37

.

7.6.6. UART0/1

Serial communication is categorized as synchronous mode and asynchronous mode in terms of its data transmission method. Synchronous mode is to transmit the data based on the standard clock pulse. Asynchronous mode is to transmit the data bit by arranging the baud rate of data bit each other without standard clock. That is, when a transmitter transmits the data as arranged frequency, a receiver read the data according to the arranged method previously.

Embedded MCU has UART0 and UART1 to enable two-way communication.
These devices support asynchronous mode. The following registers are used to control UART.

RBR (UART0 RECEIVE BUFFER REGISTER, 0x2500)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	RBR	Read the received data	R/O	0x00

THR (UART0 TRANSMITTER HOLDING REGISTER, 0x2500)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	THR	This register stores the data to be transmitted. The address is the same as RBR register. When accessing this address, received data(RBR) is read and the data to be transmitted is stored.	W/O	0x00

DLL (UART0 DIVISOR LSB REGISTER, 0x2500)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	DLL	This register can be accessed only when DLAB bit in the LCR register is set to '1'. This register shares a 16-bit register with DLM register occupying the lower 8 bits. This full	R/W	0x00

		16-bit register is used to divide clock.		

***Note 5:**: After the data is written to DLM register, it should be written in this register. When the data is written to DLL register, the clock divisor begins. Baud rate is calculated by the following equation.*

Baud rate = clock_speed / (7 × divisor_latch_value)

IER (UART0 INTERRUPT ENABLE REGISTER, 0x2501)

Bit Field	Name	Descriptions	R/W	Reset Value
7:4		Reserved		0
3	EDSSI	Enable MODEM Status Interrupt. When this field is set to '1', Modem status interrupt is enabled.	R/W	0
2	ELSI	Enable Receiver Line Status Interrupt.	R/W	0
1	ETBEI	Enable Transmitter Holding Register Empty Interrupt	R/W	0
0	ERBEI	Enable Received Data Available Interrupt	R/W	0

DLM (UART0 DIVISOR LATCH MSB REGISTER, 0x2501)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	DLM	This register can be accessed only when DLAB bit in the LCR register is set to '1'. This register shares a 16-bit register with DLL register occupying the higher 8 bits. This full 16-bit register is used to divide clock.	R/W	0x00

IIR (UART0 INTERRUPT IDENTIFICATION REGISTER, 0x2502)

Bit Field	Name	Descriptions	R/W	Reset Value
7:4		Reserved	R/O	0
3:1	INTID	Interrupt Identification. Refer to the [Table 5].	R/O	0
0	PENDING	Shows whether the interrupt is pending or not. When this field is '0', the interrupt is pending.	R/O	1

Note 6: *IIR register uses the same address as FCR register below. IIR register is read only and FCR register is write only.*

Table 8. UART0 Interrupt Lists

INTID	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
011	1st	Receiver Line Status	Parity, Overrun or Framing errors or Break Interrupt	Reading the LSR (Line Status Register).
010	2nd	Receiver Data available	FIFO trigger level reached	FIFO drops below trigger level
110	2nd	Timeout Indication	There is at least 1 character in the FIFO but no character has been input to the FIFO or read from it for the last 4 character times.	Reading from the FIFO (Receiver Buffer Register)
001	3rd	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Writing to the Transmitter Holding Register or reading IIR
000	4th	Modem Status	CTS, DSR, RI or DCD	Reading the Modem status register

FCR (UART0 FIFO CONTROL REGISTER, 0x2502)

Bit Field	Name	Descriptions	R/W	Reset Value
7:6	URXFTRIG	Adjust the trigger level of Receiver FIFO. Interrupt occurs when FIFO receives the data byte based on this field value below. For example, when URXFTRIG field is set to '3', interrupt does not occur until FIFO receives 14 byte. When FIFO receives 14 byte, interrupt occurs. 0: 1 byte 1: 4 byte 2: 8 byte 3: 14 byte	W/O	3
5:3		Reserved	W/O	0
2	UTXFRST	When this field is set to '1', Transmitter FIFO is cleared and the circuits related to it are reset.	W/O	0

1	URXFRST	When this field is set to ‘1’, Receiver FIFO is cleared and the circuits related to it are reset.	W/O	0
0		Reserved	W/O	0

LCR (UART0 LINE CONTROL REGISTER, 0x2503)

Bit Field	Name	Descriptions	R/W	Reset Value
7	DLAB	Divisor Latch Access Enable. When this field is set to ‘1’, Divisor register (DLM, DLL) can be accessed. When this field is set to ‘0’, general register can be accessed.	R/W	0
6	SB	Set Break. When this field is set to ‘1’, serial output is to be ‘0’ by force(break state)	R/W	0
5	SP	Stick Parity. When PEN and EPS is ‘1’ while this field is set to ‘1’, parity, which is generated as ‘0’, is transmitted. In reception mode, it checks whether parity value is ‘0’ or not. When PEN is ‘1’ and EPS is ‘0’ while this field is set to ‘1’, parity, which is generated as ‘1’, is transmitted. In reception mode, it checks whether parity value is ‘1’ or not.	R/W	0
4	EPS	Even Parity Enable. When this field is set to ‘1’, parity value is determined to transfer ‘1’ which is in even number. When this field is set to ‘0’, parity value is determined to transfer ‘1’ which is in odd number.	R/W	0
3	PEN	Parity Enable. When this field is set to ‘1’, parity is calculated for the byte to be transmitted and transferred with it. In reception mode, checks parity. When this field is ‘0’, parity is not generated.	R/W	0
2	STB	Number of Stop Bits. When this field is set to ‘1’, 2 stop bit is used. When transmitting a word (character) of 5 bit length, 1.5 stop bit is used. When this field is ‘0’, 1 stop bit is used.	R/W	0
1:0	WLS	Word Length Select. 0: 5-bit Word	R/W	3

		1: 6-bit Word 2: 7-bit Word 3: 8-bit Word		

There are more registers such as Modem Control Register, Line Status Register, Modem Status Register and Port Enable Register in a UART0 block. This document doesn't include these registers because they are not commonly used. For more detail information, please contact RadioPulse Inc.

The following registers are to control UART1.

RBR (UART1 RECEIVE BUFFER REGISTER, 0x2510)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	RBR	Read the received data	R/O	0x00

THR (UART1 TRANSMITTER HOLDING REGISTER, 0x2510)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	THR	This register stores the data to be transmitted. The address is same as RBR register. By accessing this address, received data(RBR) can be read and the data to be transmitted can be stored.	W/O	0x00

DLL (UART1 DIVISOR LSB REGISTER, 0x2510)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	DLL	This register can be accessed only when DLAB bit in LCR register is set to '1'. This register consists of 16-bit register with DLM register and it is a lower 8 bit of 16-bit. This 16-bit register is used to divide clock.	R/W	0x00

Note 7: *After the data is written to DLM register, it should be written in this register. When the data is written to DLL register, the clock divisor begins. Baud rate is calculated by the following equation.*

Baud rate = clock_speed / (7 × divisor_latch_value)

IER (UART1 INTERRUPT ENABLE REGISTER, 0x2511)

Bit Field	Name	Descriptions	R/W	Reset Value
7:4		Reserved		0
3	EDSSI	Enable MODEM Status Interrupt. When this field is set to '1', Modem status interrupt is enabled.	R/W	0
2	ELSI	Enable Receiver Line Status Interrupt.	R/W	0
1	ETBEI	Enable Transmitter Holding Register Empty Interrupt	R/W	0
0	ERBEI	Enable Received Data Available Interrupt	R/W	0

DLM (UART1 DIVISOR LATCH MSB REGISTER, 0x2511)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	DLM	This register can be accessed only when DLAB bit in LCR register is set to '1'. This register consists of 16-bit register with DLL register and it is a higher 8 bit of 16-bit. This 16-bit register is used to divide clock.	R/W	0x00

IIR (UART1 INTERRUPT IDENTIFICATION REGISTER, 0x2512)

Bit Field	Name	Descriptions	R/W	Reset Value
7:4		Reserved	R/O	0
3:1	INTID	Interrupt Identification. Refer to the [Table 9].	R/O	0
0	PENDING	Shows whether the interrupt is pending or not. When this field is '0', the interrupt is pending.	R/O	1

Note 8: *IIR register uses the same address as FCR register below. IIR register is read only and FCR register is write only.*

Table 9.UART1 Interrupt Lists

INTID	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
011	1st	Receiver Line Status	Parity, Overrun or Framing errors or Break Interrupt	Reading the LSR (Line Status Register).
010	2nd	Receiver Data available	FIFO trigger level reached	FIFO drops below trigger level
110	2nd	Timeout Indication	There is at least 1 character in the FIFO but no character has been input to the FIFO or read from it for the last 4 character times.	Reading from the FIFO (Receiver Buffer Register)
001	3rd	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Writing to the Transmitter Holding Register or reading IIR
000	4th	Modem Status	CTS, DSR, RI or DCD	Reading the Modem status register

FCR (UART1 FIFO CONTROL REGISTER, 0x2512)

Bit Field	Name	Descriptions	R/W	Reset Value
7:6	URXFTRIG	Adjust the trigger level of Receiver FIFO. Interrupt occurs when FIFO receives the data byte based on this field's value below. For example, when URXFTRIG field is set to '3', interrupt does not occur until FIFO receives 14 bytes until FIFO receives 14 bytes. 0: 1 byte 1: 4 byte 2: 8 byte 3: 14 byte	W/O	3
5:3		Reserved	W/O	0
2	UTXFRST	When this field is set to '1', Transmitter FIFO is cleared and the circuits related to it are reset.	W/O	0
1	URXFRST	When this field is set to '1', Receiver FIFO is cleared and the circuits related to it are reset.	W/O	0
0		Reserved	W/O	0

LCR (UART1 LINE CONTROL REGISTER, 0x2513)

Bit Field	Name	Descriptions	R/W	Reset Value
7	DLAB	Divisor Latch Access Enable. When this field is set to '1', Divisor register (DLM, DLL) can be accessed. When this field is set to '0', general register can be accessed.	R/W	0
6	SB	Set Break. When this field is set to '1', serial output is to be '0' by force(break state)	R/W	0
5	SP	Stick Parity. When PEN and EPS are '1' while this field set to '1', a parity of '0' is transmitted. In reception mode, it checks whether parity value is '0' or not. When PEN is '1' and EPS is '0' while this field is set to '1', parity of '1' is transmitted. In reception mode, it checks whether parity value is '1' or not.	R/W	0
4	EPS	Even Parity Enable. When this field is set to '1', parity value is even. When set to '0', parity value is odd.	R/W	0
3	PEN	Parity Enable. When this field is set to '1', parity is calculated for the byte to be transmitted and transferred with it. In reception mode, checks parity. When this field is '0', parity is not generated.	R/W	0
2	STB	Number of Stop Bits. When this field is set to '1', 2 stop bit is used. When transmitting a word (character) of 5 bit length, 1.5 stop bit is used. When this field is '0', 1 stop bit is used.	R/W	0
1:0	WLS	Word Length Select. 0: 5-bit Word 1: 6-bit Word 2: 7-bit Word 3: 8-bit Word	R/W	3

There are more registers such as Modem Control Register, Line Status Register, Modem Status Register and Port Enable Register in a UART1 block. This document doesn't include these registers because they are not commonly used. For more detailed information, please contact RadioPulse Inc.

7.6.7. SPI MASTER/SLAVE

During an SPI transmission, data is simultaneously transmitted(shifted out serially) and received(shifted in serially). The operation is different in either Master mode or Slave mode

In the Master mode, the data transmission is done by writing to the SPDR(SPI Data Register, 0x2542).
After transmission, data reception is initiated by a byte transmitted to the Slave device from the Master SPI clock. When the SPI interrupt occurs, the value of the SPDR register becomes the received data from the SPI slave device. Even though the SPDR TX and RX have the same address, no data collision occurs because the processes of writing and reading data happen sequentially.

In the Slave mode, the data must be ready in the SPDR when the Master calls for it. Data transmission is accomplished by writing to the SPDR before the SPI clock is generated by the Master. When the Master generates the SPI clock, the data in the SPDR of the Slave is transferred to the Master. If the SPDR in the Slave is empty, no data exchange occurs. Data reception is done by reading the SPDR when the next SPI interrupt occurs.

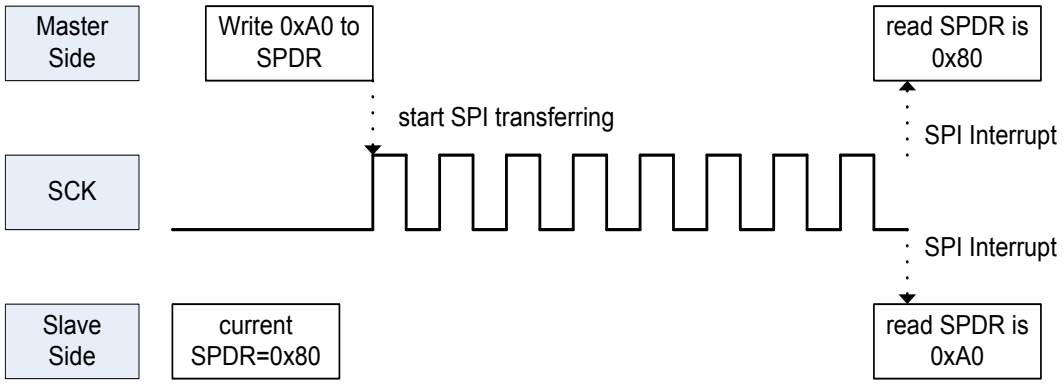


Figure 22. SPI Data Transfer

SPCR (SPI CONTROL REGISTER, 0x2540)

Bit Field	Name	Descriptions	R/W	Reset Value
7	SPIE	SPI Interrupt Enable. When this field is set to '1', SPI interrupt is enabled.	R/W	0
6	SPE	SPI Enable. When this field is set to '1', SPI is enabled.	R/W	0
5		Reserved		0
4	MSTR	Master Mode Select. When this field is set to '1', a Master mode is selected.	R/W	1
3	CPOL	Clock Polarity. If there is no data transmission while this field is set to '0', SCK pin retains '0'. If there is no data transmission while this field is set to '1', SCK pin retains '1'. This field is used to set the clock and data between a Master and Slave with CPHA field. Refer to the below for the more detail explanation.	R/W	0
2	CPHA	Clock Phase. This field is used to set the clock and data between a Master and Slave with CPOL field.	R/W	0
1:0	SPR	SPI Clock Rate Select. With ESPR field in SPER register(0x2543), this field selects SPI clock(SCK) rate when a device is configured as a Master. Refer to the ESPR field.	R/W	0

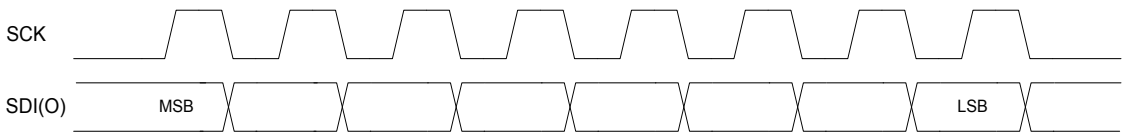
There are four methods of data transfer based on the settings of CPOL and CPHA. Polarity of SPI serial clock(SCK) is determined by CPOL value and it determines whether SCK activates high or low.

If CPOL value is '0', SCK pin retains '0' during no data transmission. If CPOL value is '1', SCK pin retains '1' during no data transmission. CPHA field determines the format of data to be transmitted.

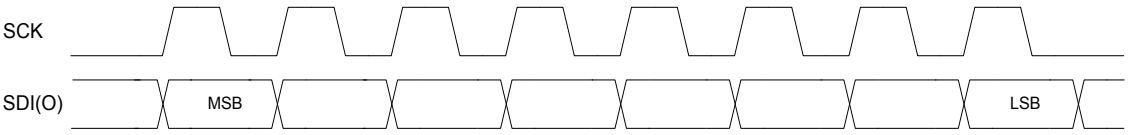
The table below describes the clock polarity and the data transition timing.

CPOL	CPHA	SCK when idle	Data Transition Timing
0	0	Low	Falling Edge of SCK
0	1	Low	Rising Edge of SCK
1	0	High	Rising Edge of SCK
1	1	High	Falling Edge of SCK

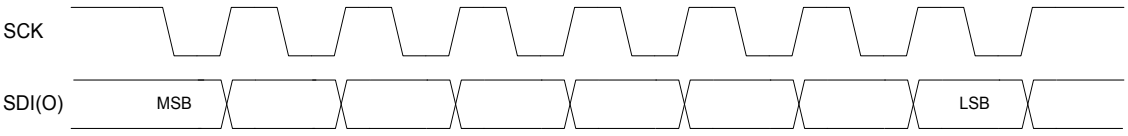
The following describes this block when slave mode is selected. When the values of CPOL and CPHA are the same, (a) and (b) below, output data is changed at the falling edge of SCK. Input data is captured at the rising edge of SCK. When the CPOL and CPHA values are different, (b) and (c) below, output data is changed at the rising edge of received SCK. Input data is captured at the falling edge of SCK.



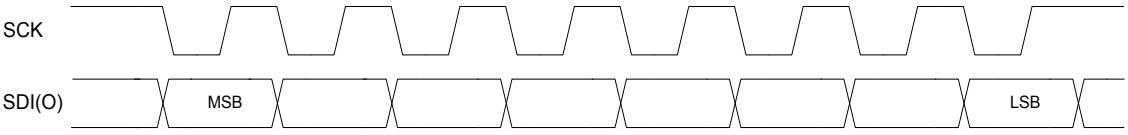
(a) CPOL=0, CPHA=0



(b) CPOL=0, CPHA=1



(c) CPOL=1, CPHA=0



(d) CPOL=1, CPHA=1

SPSR (SPI STATUS REGISTER, 0x2541)

Bit Field	Name	Descriptions	R/W	Reset Value
7	SPIF	SPI Interrupt Flag. When SPI interrupt occurs, this field is set to '1'. This field is set whenever data transmission is finished and it can be cleared by software.	R/W	0
6	WCOL	Write Collision This field is set to '1' when writing data to the SPDR register while SPITX FIFO is full. It can be cleared by software.	R/W	0
5:4		Reserved		0
3	WFFUL	Write FIFO Full. This field is set to '1' when Write FIFO is full. This field is read only.	R/O	0
2	WFEMPTY	Write FIFO Empty. This field is set to '1' when Write FIFO is cleared. This field is read only.	R/O	1
1	RFFUL	Read FIFO Full. This field is set to '1' when Read FIFO is full. This field is read only.	R/O	0
0	RFEMPTY	Read FIFO Empty. This field is set to '1' when Read FIFO is cleared. This field is read only.	R/O	1

SPDR(SPI DATA REGISTER, 0x2542)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	SPDR	This register is read/write buffer.	R/W	-

SPER(SPI EXTENDED REGISTER, 0x2541)

Bit Field	Name	Descriptions	R/W	Reset Value
7:6	ICNT	Interrupt Count. This field indicates the number of byte to transmit. SPIF bit is set to '1' whenever each byte is transmitted.	R/W	0

<table>
<tr><td>5:2</td><td></td><td>Reserved</td><td></td><td>0</td></tr>
<tr><td>1:0</td><td>ESPR</td><td>Extended SPI Clock Rate Select.
With SPR field in SPCR Register(0x2540), this field selects SPI clock(SCK) rate when a device is configured as a Master.

<table><tr><th>{ESPR, SPR}</th><th>(System Clock Divider)</th></tr><tr><td>0000</td><td>Reserved</td></tr><tr><td>0001</td><td>Reserved</td></tr><tr><td>0010</td><td>8</td></tr><tr><td>0011</td><td>32</td></tr><tr><td>0100</td><td>64</td></tr><tr><td>0101</td><td>16</td></tr><tr><td>0110</td><td>128</td></tr><tr><td>0111</td><td>256</td></tr><tr><td>1000</td><td>512</td></tr><tr><td>1001</td><td>1024</td></tr><tr><td>1010</td><td>2048</td></tr><tr><td>1011</td><td>4096</td></tr></table>* ESPR field : high bit
SPR field: low bit</td><td>R/W</td><td>2</td></tr>
</table>

The value of ESPR and SPR is used to divide system clock to generate SPI clock(SCK).

For example, if the value of ESPR and SPR is ‘0010’ and system clock is 8MHz, SPI clock(SCK) is 1MHz.

7.6.8. VOICE

A voice function includes the followings;

- I2S Interface
- Voice CODEC (u-law / a-law /ADPCM)
- Voice FIFO
- DMA

The data generated through an external ADC is input to the voice block in MG245X via an IS2 interface. Data received via I2S is compressed at the voice codec, and stored in the Voice TXFIFO. The data is then transferred to the MAC TX FIFO through DMA operation and finally transmitted through the PHY layer.

By contrast, received data in the MAC RX FIFO is transferred to the Voice RXFIFO and decompressed in the voice codec. It is finally transferred to an external DAC via I2S interface.

I2S is commonly used for transferring/receiving voice data. As well, voice data can be transferred or received via SPI or UART interface as well.

Voice codec supports u-law, a-law and ADPCM methods.
If the voice codec function is not needed, it can be bypassed.

Note: When the transmission error is caused while sending audio data using DVI ADPCM codec embedded in MG245X, sound might be changed in a sudden.
For the detail information, refer to '[MG245X ERRATA NOTES-005] ADPCM ERRATA' note.

7.6.8.1. I2S

In I2S interface, data is transferred MSB first from the left channel, and then from the right channel. There are two ways to send data via I2S TX: writing data to the register by software, or by hardware. This is enabled by using POP field in STXMODE(0x252d). Similarly, there are two ways to receive data via I2S RX: the first is reading the register by software, and the other is by the PUSH field in SRXMODE(0x253d).
There are four methods in I2S interface as follows;

- I2S mode
- Left Justified mode
- Right Justified mode
- DSP mode

In I2S mode, left channel data is transferred in order. When left channel data is transferred, LRCK value is '0' and when right channel data is transferred, LRCK value is 0. Transferred data and LECK is changed at the falling edge. Refer to the (a) below.

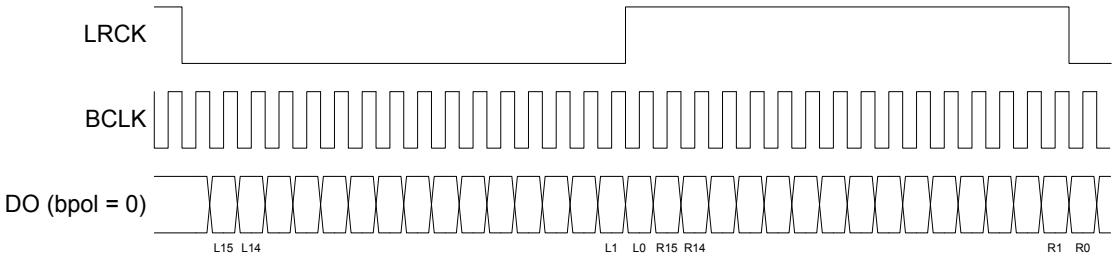
In Left Justified mode, left channel data is transferred whenever LRCK=1 and right channel data is transferred, whenever LRCK=0. LRCK is changed at the falling edge of BLCK. Transferred data is changed at the rising edge of BCLK. Refer to the (b) below.

In Right Justified mode, left channel data allows last LSB to be output before LRCK value goes to '0' and right channel data allows last LSB to be output before LRCK value goes to '1'.
LRCK value is changed at the falling edge of BCLK. Output data is changed at the rising edge of BCLK. Refer to the (c) below.

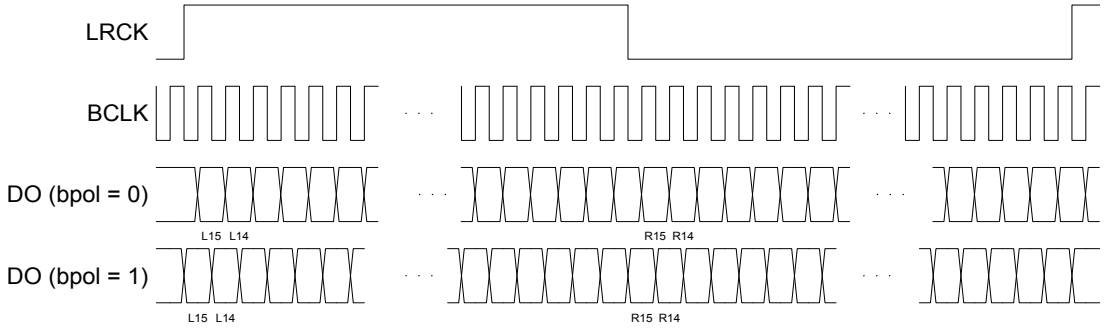
In DSP mode, after LRCK outputs to '1' for one period of BCLK, it goes to '0'. After that, left channel data is outputted and then right channel data is outputted. LRCK value is changed at the falling edge of BCLK. Output data is changed at the rising edge of BCLK. Refer to the (d) below.

The following shows the interface method for each mode and I2S TX block is selected as Master. The setting of register is as follows. MS field in STXAIC(0x2528) register is set to '1'. WL field is set to '0'(The data of left and right channel represents 16-bit). Other fields are set to

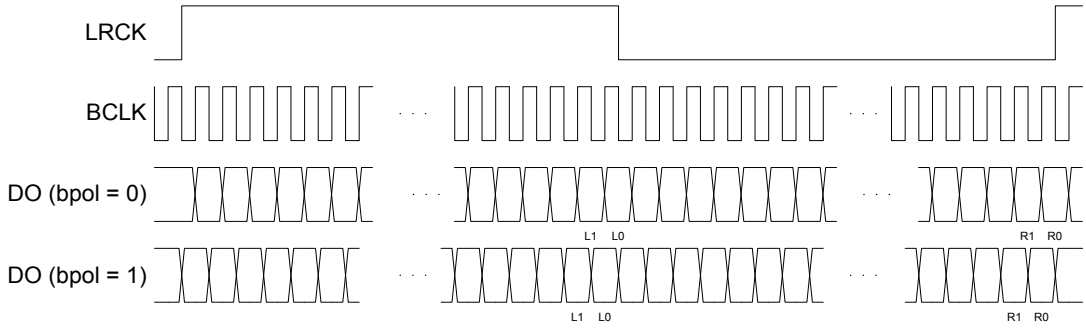
‘0’. In ISP mode, BPOL field in STXMODE(0x252D) register is set to ‘0’. In other modes, BPOL field in STXMODE(0x252D) register is set to ‘0’ or ‘1’ respectively.



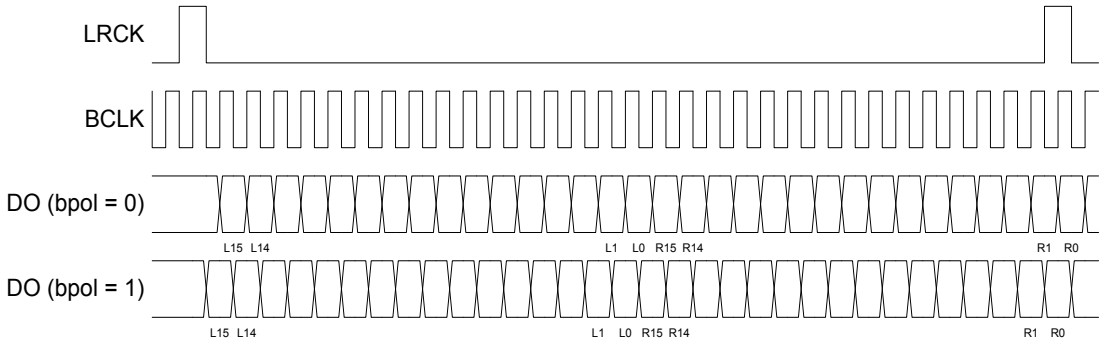
(a) I2S Mode



(b) Left Justified Mode



(c) Right Justified Mode



(d) DSP Mode

STXAIC (I2S TX INTERFACE CONTROL REGISTER, 0x2528)

Bit Field	Name	Descriptions	R/W	Reset Value
7	MS	When this field is set to '1', Master mode is configured. When this field is set to '0', Slave mode is configured. Any device can act as the system master by providing the necessary clock signals. A slave will usually derive its internal clock signal from an external clock input.	R/W	1
6:5	FMT	Four modes of operation determined by the value of this field below. 0: I2S mode 1: Left Justified mode 2: Right Justified mode 3: DSP mode	R/W	2
4:3	WL	Word Length. This field indicates the number of bit per channel. 0: 16 bit 1: 20 bit 2: 24 bit 3: 32 bit	R/W	0
2	LRSWAP	Left/Right Swap. When this field is set to '1', the order of the channel for transmitting data is changed. In other words, the data in a right channel is transmitted first.	R/W	0
1	FRAMEP	When this field is set to '1', the polarity of LRCK is changed. For example, in Left Justified mode, the left channel data is outputted when LRCK=1 and the right	R/W	0

		channel data is outputted when LRCK=0. However, when this field is set to '1', the right channel data is outputted when LRCK=1 and the left channel data is outputted when LRCK=0.		
0	BCP	When this field is set to '1', the polarity of BCLK(Bit Clock) is changed. Clock edge, which allows the data change, is changed.	R/W	0

STXSDIV (I2S TX SYSTEM CLOCK DIVISOR REGISTER, 0x252A)

Bit Field	Name	Descriptions	R/O	Reset Value
7:0	STXSDIV	This register set the value for dividing a system clock to generate MCLK. The equation is as follows: MCLK = System Clock/(2×STXSDIV) When this field is '0', MCLK is not generated.	R/O	0x00

STXMDIV (I2S TX MCLK DIVISOR REGISTER, 0x252B)

Bit Field	Name	Descriptions	R/O	Reset Value
7:0	STXMDIV	This register sets the value for dividing MCLK to generate BCLK. When STXSDIV register value is '1', BCLK = MCLK/STXMDIV. When STXSDIV register value is greater than 2, BCLK = MCLK/(2×STXMDIV). When this register value is '0', BCLK is not generated.	R/O	0x00

STXBDIV (I2S TX BCLK DIVISOR REGISTER, 0x252C)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	STXBDIV	This register set the value for dividing BCLK to generate LRCK. When FMT field in STXAIC(0x2528) register is '0','1','2', LRCK = BCLK/(2×STXBDIV). When FMT field in STXAIC(0x2528) register	R/W	0x00

		is ‘3’, LRCK = BCLK/STXBDIV. When this register value is ‘0’, LRCK is not generated.		

STXMODE (I2S TX MODE REGISTER, 0x252D)

Bit Field	Name	Descriptions	R/W	Reset Value
7	CSHR	This field is meaningful when I2STX block acts as Slave mode. When this field is set to ‘1’, I2S TX block shares the clock of I2S RX block. In other words, the MCLK of the I2S RX block is input to the MCLK of I2S TX block and BCLK of I2S RX block is input to the BCLK of I2S TX block. As well, LRCK of I2S RX block is input to the LRCK of I2S TX block.	R/W	1
6	MPOL	This field determines the polarity of MCLK. When this field is ‘0’, MCLK signal retains ‘1’. When this field is ‘1’, MCLK signal retains ‘0’.	R/W	1
5	BPOL	This field indicates the relationship between BCLK and LRCK. When this field is set to ‘0’, LRCK value is changed at the falling edge of BCLK. When this field is set to ‘1’, LRCK value is changed at the rising edge of BCLK.	R/W	1
4	B16	This field determines bit width to transfer data in voice block to I2S block. When this field is set to ‘1’, data is transferred by 16-bit data format to I2S block. When this field is set to ‘0’, data is transferred by 8-bit data format to I2S block.	R/W	1
3	POP	When this field is set to ‘1’, data is transferred to I2S block. When this field is set to ‘0’, data is not transferred to I2S block.	R/W	1
2:1	MODE	This field sets the mode of transferred data. 0: BLK Mode. Transfer a ‘0’. 1: MRT Mode. Only the data in Right channel is transferred.(‘0’ is transferred in Left channel) 2: MLT Mode. Only the data in Left channel is transferred.(‘0’ is transferred in Right	R/W	3

		channel) 3: STR Mode. All data in Left or Right channel are transferred.		
0	CLKENA	Clock Enable. When this field is set to '1', I2S TX is enabled.	R/W	0

SRXAIC (I2S RX INTERFACE CONTROL REGISTER, 0x2538)

Bit Field	Name	Descriptions	R/W	Reset Value
7	MS	When this field is set to '1', Master mode is configured. When this field is set to '0', Slave mode is configured. Any device can act as the system master by providing the necessary clock signals. A slave will usually derive its internal clock signal from an external clock input.	R/W	1
6:5	FMT	Four modes determined by the value of this field below. 0: I2S mode 1: Left Justified mode 2: Right Justified mode 3: DSP mode	R/W	2
4:3	WL	Word Length. This field indicates the number of bit per each channel. 0: 16 bit 1: 20 bit 2: 24 bit 3: 32 bit	R/W	0
2	LRSWAP	Left/Right Swap. When this field is set to '1', the order of the channel for transmitting data is changed. In other words, the data in a right channel is transmitted first.	R/W	0
1	FRAMEP	When this field is set to '1', the polarity of LRCK is changed, in Left Justified mode(FMT=1), data is stored in the left channel when LRCK=1 and data is stored in the right channel when LRCK=0. However, when this field is set to '1', data is stored in the right channel when LRCK=1 and the data is stored in the left channel when LRCK=0.	R/W	0
0	BCP	When this field is set to '1', the polarity of BCLK(Bit Clock) is changed.	R/W	0

		Clock edge, which allows the data change, is changed.		

SRXSDIV (I2S RX SYSTEM CLOCK DIVISOR REGISTER, 0x253A)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	SRXSDIV	This register sets the value for dividing a system clock to generate MCLK. The equation is as follows: MCLK = System Clock/(2× SRXSDIV) When this field is '0', MCLK is not generated.	R/W	0x00

SRXMDIV (I2S RX MCLK DIVISOR REGISTER, 0x253B)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	SRXMDIV	This register sets the value for dividing MCLK to generate BCLK. When SRXSDIV register value is '1', BCLK = MCLK/SRXMDIV. When SRXSDIV register value is greater than 2, BCLK = MCLK/(2×SRXMDIV). When this register value is '0', BCLK is not generated.	R/W	0x00

SRXBDIV (I2S RX BCLK DIVISOR REGISTER, 0x253C)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	SRXBDIV	This register sets the value for dividing BCLK to generate LRCK. When FMT field in SRXAIC(0x2528) register is '0','1','2', LRCK = BCLK/(2(SRXBDIV). When FMT field in SRXAIC(0x2528) register is '3', LRCK = BCLK/SRXBDIV. When this register value is '0', LRCK is not generated.	R/W	0x00

SRXMODE (I2S RX MODE REGISTER, 0x253D)

Bit Field	Name	Descriptions	R/W	Reset Value
7	CSHR	This field is meaningful when I2SRX block acts in a Slave mode. When this field is set to '1', I2S RX block shares the clock of I2S TX block. In other words, MCLK of I2S TX block is input to the MCLK of I2S RX block and BCLK of I2S TX block is input to the BCLK of I2S RX block. As well, LRCK of I2S TX block is input to the LRCK of I2S RX block.	R/W	0
6	MPOL	This field determines the polarity of MCLK. When this field is '0', MCLK signal retains '1'. When this field is '1', MCLK signal retains '0'.	R/W	1
5	BPOL	This field indicates the relationship between BCLK and LRCK. When this field is set to '0', LRCK value is changed at the falling edge of BCLK. When this field is set to '1', LRCK value is changed at the rising edge of BCLK.	R/W	1
4	B16	This field determines bit width to transfer data received from external ADC via I2S interface to voice block. When this field is set to '1', data is transferred by 16-bit data format to voice block. When this field is set to '0', data is transferred by 8-bit data format to voice block.	R/W	1
3	PUSH	When this field is set to '1', data received from external ADC via I2S interface is transferred to voice block. When this field is set to '0', data received from external ADC via I2S interface is not transferred to voice block.	R/W	1
2:1	MODE	This field sets the mode of transferred data. 0: BLK Mode. Transfer a '0'. 1: MRT Mode. Only the data in Right channel is transferred.('0' is transferred in Left channel) 2: MLT Mode. Only the data in Left channel is transferred.('0' is transferred in Right channel)	R/W	3

		3: STR Mode. All data in Left or Right channel are transferred.		
0	CLKENA	Clock Enable. When this field is set to '1', I2S RX is enabled.	R/W	0

7.6.8.2. VOICE CODEC

MG245X includes three voice codec algorithms.

- μ-law
- a-law
- ADPCM

The μ-law algorithm is a companding algorithm primarily used in the digital telecommunication systems of North America and Japan. As with other companding algorithms, its purpose is to reduce the dynamic range of an audio signal. In the analog domain this can increase the signal-to-noise ratio (SNR) achieved during transmission and in the digital domain, it can reduce the quantization error (hence increasing signal to quantization noise ratio). These SNR improvements can be traded for reduced bandwidth and equivalent SNR instead.

The a-law algorithm is a standard companding algorithm used in European digital communications systems to optimize/modify the dynamic range of an analog signal for digitizing.

The a-law algorithm provides a slightly larger dynamic range than the μ-law at the cost of worse proportional distortion for small signals.

Adaptive DPCM (ADPCM) is a variant of DPCM (Differential (or Delta) pulse-code modulation) that varies the size of the quantization step, to allow further reduction of the required bandwidth for a given signal-to-noise ratio. DPCM encodes the PCM values as differences between the current and the previous value. For audio this type of encoding reduces the number of bits required per sample by about 25% compared to PCM.

In order to control voice codec, there are several registers. This section describes the major commonly used registers. For more detailed information, please contact RadioPulse Inc.

ENCCTL (VOICE ENCODER CONTROL REGISTER, 0x2745)

Bit Field	Name	Descriptions	R/W	Reset Value
7:6		Reserved	R/W	0
5	B16	When the bit width of data received to voice encoder is 16-bit, set this field to '1'. When the bit width of data received to voice encoder is 8-bit, set this field to '0'.	R/W	0
4	MUT	Mute Enable. When this field is set to '1', the Mute function is enabled. ENCMUT1 and ENCMUT0 values are input to the voice encoder block.	R/W	0
3:2	SEL	Encoder Select. Selects voice encoder algorithm. 0: No Encoding 1: μ-law 2: a-law 3: ADPCM	R/W	0
1	INI	Encoder Initialize. When this field is set to '1', the pointer in voice encoder is initialized. This field cannot be read.	W	0
0	ENA	Encoder Enable. When this field is set to '1', voice encoder acts.	R/W	0

DECCTL (VOICE DECODER CONTROL REGISTER, 0x274D)

Bit Field	Name	Descriptions	R/W	Reset Value
7	LPB	Loopback Test. When this field is set to '1', Loopback test mode is selected. In this case, the output of voice encoder is connected to the input of voice decoder.	R/W	0
6		Reserved	R/W	0
5	B16	The bit width of data which is output from voice decoder is 16-bit, set this field to '1'. When this field is set to '0', the bit width of data which is output from voice decoder is 8-bit.	R/W	0

4	MUT	Mute Enable. When this field is set to '1', Mute function is enabled. DECMUT1 and DECMUT0 value is transferred from voice decoder.	R/W	0
3:2	SEL	Decoder Select. Select voice decoder. 0: No Decoding 1: μ-law 2: a-law 3: ADPCM	R/W	0
1	INI	When this field is set to '1', the pointer in voice decoder is initialized. This field cannot be read.	W	0
0	ENA	Decoder Enable. When this field is set to '1', voice decoder acts.	R/W	0

7.6.8.3. VOICE FIFO

Data received via I2S interface is compressed by voice codec; compressed data is stored in Voice TXFIFO(0x2600~0x267F). The size of Voice TXFIFO is 128 byte.

Data in MAC RXFIFO is processed by DMA operation, and stored in Voice RX FIFO(0x2680~0x26FF). Data in Voice RXFIFO is decompressed by the voice codec and transmitted to an external component via I2S. The size of Voice RXFIFO is 128 byte.

7.6.8.4. VOICE TX FIFO CONTROL

VTFDAT (VOICE TX FIFO DATA REGISTER, 0x2750)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	VTFDAT	When writing data to this register, data is stored in Voice TX FIFO in order. When reading this register, data stored in Voice TX FIFO can be read.	R/W	0x00

VTFMUT (VOICE TX FIFO MUTE DATA REGISTER, 0x2751)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	VTFMUT	When MUT field in VTFCTL register is set to '1', data in this register is transferred instead of data in Voice TX FIFO. When INI field in VTFCTL register is set to '1', data in Voice TX FIFO is initialized by data in VTFMUT.	R/W	0x00

VTFCTL (VOICE TX FIFO CONTROL REGISTER, 0x2752)

Bit Field	Name	Descriptions	R/W	Reset Value
7:4		Reserved		0
3	VTDENA	Voice TX DMA Enable. When this field is set to '1', Voice TX DMA is enabled. This field value is cleared automatically.	W/O	0
2	MUT	When this field is set to '1', data in VTFMUT register is transferred instead of data in Voice TX FIFO. This field can be read.	R/W	0
1	CLR	When this field is set to '1', Write pointer and Read pointer of Voice TX FIFO are initialized. The status value of underflow and overflow is initialized.	W/O	0
0	INI	When this field is set to '1', all data in Voice TXFIFO are replaced by the value in VTFMUT register.	W/O	0

VTFRP (VOICE TX FIFO READ POINTER REGISTER, 0x2753)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	VTFRP	This register indicates the address of Voice TXFIFO to be read next. Since the size of FIFO is 128 byte, LSB is used to test wrap-around.	R/W	0x00

VTFWP (VOICE TX FIFO WRITE POINTER REGISTER, 0x2754)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	VTFWP	This register indicates the address of Voice TXFIFO to be written next. Since the size of FIFO is 128 byte, LSB is used to test wrap-around.	R/W	0x00

VTFSTS (VOICE TX FIFO STATUS REGISTER, 0x275A)

Bit Field	Name	Descriptions	R/W	Reset Value
7:5		Reserved		0
4	ZERO	When INI field in VTFCTL register is set to '1', data in Voice TX FIFO is initialized by data in VTFMUT register. During this initialization is processed, this field is set to '1'. After initialization is finished, this field is set to '0'.	R/O	0
3	PSH	This field is set to '1' while pushing data into Voice TX FIFO.	R/O	0
2	POP	This field is set to '1' while popping data on Voice TX FIFO.	R/O	0
1:0		Reserved		0

VTDSIZE (VOICE TX DMA SIZE REGISTER(VOICE TX FIFO->MAC TX FIFO), 0x275B)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	VTDSIZE	Set the data size for DMA operation.	R/W	0x00

7.6.8.5. VOICE RX FIFO CONTROL

VRFDAT (VOICE RX FIFO DATA REGISTER, 0x2760)

Bit Field	Name	Descriptions	R/W	Reset Value

7:0	VRFDAT	When writing data to this register, data is stored in Voice RX FIFO in order. When reading this register, data stored in Voice RX FIFO can be read.	R/W	0x00

VRFMUT (VOICE RX FIFO MUTE DATA REGISTER, 0x2761)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	VRFMUT	When MUT field in VRFCTL register is set to '1', data in this register is transferred instead of data in Voice RX FIFO. When INI field in VRFCTL register is set to '1', data in Voice RX FIFO is initialized by data in VTFMUT.	R/W	0x00

VRFCTL (VOICE RX FIFO CONTROL REGISTER, 0x2762)

Bit Field	Name	Descriptions	R/W	Reset Value
7:4		Reserved		0
3	VRDENA	Voice RX DMA Enable. When this field is set to '1', Voice RX DMA is enabled. This field value is cleared automatically.	W/O	0
2	MUT	When this field is set to '1', data in VRFMUT register is transferred instead of data in Voice RX FIFO. This field can be read.	R/W	0
1	CLR	When this field is set to '1', Write pointer and Read pointer of Voice RX FIFO are initialized. The status value of underflow and overflow is initialized.	W/O	0
0	INI	When this field is set to '1', all data in Voice RXFIFO are replaced by the value in VRFMUT register.	W/O	0

VRFRP (VOICE RX FIFO READ POINTER REGISTER, 0x2763)

Bit Field	Name	Descriptions	R/W	Reset Value

7:0	VRFRP	This register indicates the address of Voice RXFIFO to be read next. Since the size of FIFO is 128 byte, LSB is used to test wrap-around.	R/W	0x00

VRFWP (VOICE RX FIFO WRITE POINTER REGISTER, 0x2764)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	VRFWP	This register indicates the address of Voice RXFIFO to be written next. Since the size of FIFO is 128 byte, the LSB is used to test wrap-around.	R/W	0x00

VRFSTS (VOICE RX FIFO STATUS REGISTER, 0x276A)

Bit Field	Name	Descriptions	R/W	Reset Value
7:5		Reserved		0
4	ZERO	When INI field in VRFCTL register is set to ‘1’, data in the Voice TX FIFO is initialized by data in VRFMUT register. During the processing of this initialization, this field is set to ‘1’, and set to ‘0’ when initialization is finished.	R/O	0
3	PSH	This field is set to ‘1’ while pushing data into the Voice RX FIFO.	R/O	0
2	POP	This field is set to ‘1’ while popping data on the Voice RX FIFO.	R/O	0
1:0		Reserved		0

VRDSIZE (VOICE RX DMA SIZE REGISTER(MAC RX FIFO->VOICE RX FIFO), 0x276B)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	VRDSIZE	Sets the data size for DMA.	R/W	0x00

7.6.8.6. VOICE INTERFACE CONTROL

VTFINTENA (VOICE TX FIFO INTERRUPT ENABLE REGISTER, 0x2770)

Bit Field	Name	Descriptions	R/W	Reset Value
7	EMPTY	Voice TX FIFO Empty Interrupt Enable	R/W	0
6	FULL	Voice TX FIFO Full Interrupt Enable	R/W	0
5:0		Should be set as ‘0’.		0

VRFINTENA (VOICE RX FIFO INTERRUPT ENABLE REGISTER, 0x2771)

Bit Field	Name	Descriptions	R/W	Reset Value
7	EMPTY	Voice RX FIFO Empty Interrupt Enable	R/W	0
6	FULL	Voice RX FIFO Full Interrupt Enable	R/W	0
5:0		Should be set as ‘0’.		0

VDMINTENA (VOICE DMA CONTROLLER INTERRUPT ENABLE REGISTER, 0x2772)

Bit Field	Name	Descriptions	R/W	Reset Value
7:5		Should be set as ‘0’.		0
4	VTDDONE	Voice TX DMA Done Interrupt Enable	R/W	0
3:1		Should be set as ‘0’.		0
0	VRDDONE	Voice RX DMA Done Interrupt Enable	R/W	0

VTFINTSRC (VOICE TX FIFO INTERRUPT SOURCE REGISTER, 0x2773)

Bit Field	Name	Descriptions	R/W	Reset Value
7	EMPTY	Voice TX FIFO Empty Interrupt Source. When EMPTY field in VTFINTENA register is set to ‘1’ and EMPTY field in VTFINTVAL register is set to ‘1’, this field is set to ‘1’. Cleared by software.	R/W	0

6	FULL	Voice TX FIFO Full Interrupt Source	R/W	0
5:0		Reserved		0

VRFINTSRC (VOICE RX FIFO INTERRUPT SOURCE REGISTER, 0x2774)

Bit Field	Name	Descriptions	R/W	Reset Value
7	EMPTY	Voice RX FIFO Empty Interrupt Source	R/W	0
6	FULL	Voice RX FIFO Full Interrupt Source	R/W	0
5:0		Reserved		0

VDMINTSRC (VOICE DMA CONTROLLER INTERRUPT SOURCE REGISTER, 0x2775)

Bit Field	Name	Descriptions	R/W	Reset Value
7:5		Should be set as ‘0’.		0
4	VTDDONE	Voice TX DMA Done Interrupt Source	R/W	0
3:1		Should be set as ‘0’.		0
0	VRDDONE	Voice RX DMA Done Interrupt Source	R/W	0

SRCCTL (VOICE SOURCE CONTROL REGISTER, 0x277A)

Bit Field	Name	Descriptions	R/W	Reset Value
7		Should be set as ‘0’.		0
6:5	MUX	Selects the specific interface to communicate between voice codec and an external data. 0: I2S 1: SPI 2: UART0 3: UART1	R/W	0
4:0		Should be set as ‘0’.		0

VSPCTL (VOICE SOURCE PATH CONTROL REGISTER, 0x277E)

Bit Field	Name	Descriptions	R/W	Reset Value
7		Reserved		0
6	DECMUT	This register is used to send mute data from voice decoder to external interface. When this field is set to '1', VSPMUT1 and VSPMUT0 value are transferred to the external interface.	R/W	0
5	DECINI	When using 8-bit external interface, 16-bit data transferred from voice decoder needs to be changed to 8-bit. When this field is set to '1', corresponding control circuit is initialized.	R/W	0
4	DECB16	When using 8-bit external interface such as UART and so on, 16-bit data transferred from voice decoder needs to be changed to 8-bit. When this field is set to '1', high 8-bit data of 16-bit data is transferred first and then low 8-bit data is transferred.	R/W	0
3		Reserved		0
2	ENCMUT	This register is used to send mute data from external interface to voice encoder. When this field is set to '1', VSPMUT1 and VSPMUT0 values are transferred to voice encoder.	R/W	0
1	ENCINI	When using 8-bit external interface, 16-bit data transferred to voice encoder needs to be changed to 16-bit. When this field is set to '1', corresponding control circuit is initialized.	R/W	0
0	ENCB16	When using 8-bit external interface, 8-bit input data needs to be changed to 16-bit, which is compatible with the voice encoder. When this field is set to '1', it is changed to 16-bit.(8-bit received first: high bit 8-bit received later: low bit)	R/W	0

7.6.9. RANDOM NUMBER GENERATOR (RNG)

Random Number Generator generates 32-bit random number with seed. Whenever ENA bit in RNGC register is set to '1', generated number is stored in RNGD3 ~ RNGD0 register.

RNGD3 (RNG DATA3 REGISTER, 0x2550)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	RNGD3	This register stores MSB(RNG[31:24]) of 32-bit random number.	R/O	0xB7

RNGD2 (RNG DATA2 REGISTER, 0x2551)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	RNGD2	This register stores 2nd MSB(RNG[23:16]) of 32-bit random number.	R/O	0x91

RNGD1 (RNG DATA1 REGISTER, 0x2552)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	RNGD1	This register stores 3rd MSB(RNG[15:8]) of 32-bit random number.	R/O	0x91

RNGD0 (RNG DATA0 REGISTER, 0x2553)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	RNGD0	This register stores LSB(RNG[7:0]) of 32-bit random number.	R/O	0xC9

SEED3 (RNG SEED3 REGISTER, 0x2554)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	SEED3	This register stores MSB(SEED[31:24]) of required seed to generate random number.	W/O	-

SEED2 (RNG SEED2 REGISTER, 0x2555)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	SEED2	This register stores 2nd MSB(SEED[23:16]) of required seed to generate random number.	W/O	0x00

SEED1 (RNG SEED1 REGISTER, 0x2556)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	SEED1	This register stores 3rd MSB(SEED[15:8]) of required seed to generate random number.	W/O	0x00

SEED0 (RNG SEED0 REGISTER, 0x2557)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	SEED0	This register stores LSB(SEED[7:0]) of required seed to generate random number.	W/O	0x00

RNGC (RNG DATA3 REGISTER, 0x2558)

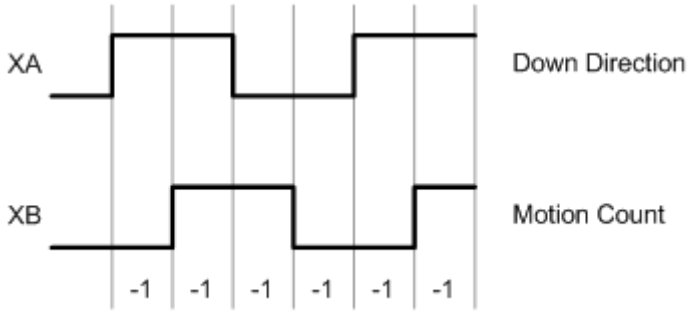
Bit Field	Name	Descriptions	R/W	Reset Value
7:1		Reserved		0
0	ENA	RNG Enable. When this field is set to ‘1’, RNG acts. This field value is changed to ‘0’ automatically.	R/W	0

7.6.10. QUAD DECODER

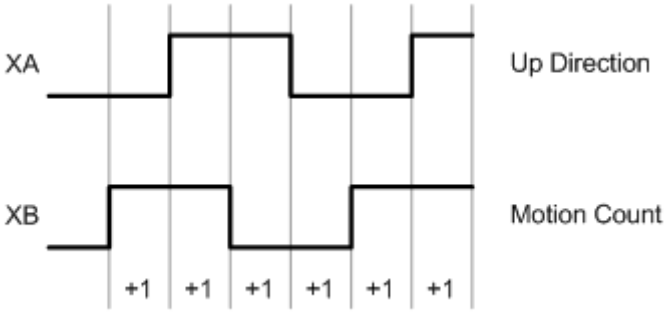
Quad Decoder block notifies the MCU of the counter value based on the direction and movement of a pointing device, such as a mouse, after receiving Quadrature signal from the pointing device.

Quadrature signal is changed with 90° phase difference(1/4 period) between two signals as shown in [Figure 23] In addition, counter value means 1/4 of one period. Since this block can receive three Quadrature signals, it can support not only the two-dimensional movement such as mouse but also the pointing device which is in three dimensions.

(a) in [Figure 23] shows that XA signal is changing before the XB signal. In this case, the pointing device is moving in the down direction. Drawing (b) shows that XB signal is changing before XA signal. In this case, the pointing device is moving in the up direction. The rules for YA, YB, ZA and ZB are the same as described above for XA and XB.



(a)



(b)

Figure 23. Quadrature signal between XA and XB signal.

UDX (UpDown X Register, 0x2560)

Bit Field	Name	Descriptions	R/W	Reset Value
7:1		Reserved		0
0	UPDN_X	This field notifies the MCU of movement in the X-axis direction. 1: Up 0: Down	R/O	0

CNTX (Count X Register, 0x2561)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	CNTX	This field notifies the MCU of the count value for movement in the X-axis direction.	R/O	0x00

UDY (UpDown Y Register, 0x2562)

Bit Field	Name	Descriptions	R/W	Reset Value
7:1		Reserved		
0	UPDN_Y	This field notifies the MCU of movement in the Y-axis direction. 1: Up 0: Down	R/O	0

CNTY (Count Y Register, 0x2563)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	CNTY	This field notifies the MCU of the count value for movement in the Y-axis direction.	R/O	0x00

UDZ (UpDown Z Register, 0x2564)

Bit Field	Name	Descriptions	R/W	Reset Value
7:1		Reserved		0x00
0	UPDN_Z	This field notifies the MCU of movement in the Z-axis. 1: Up 0: Down	R/O	0

CNTZ (Count Z Register, 0x2565)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	CNTZ	This field notifies the MCU of the count value for movement in the Z-axis.	R/O	0x00

QCTL (Quad Control Register, 0x2566)

Bit Field	Name	Descriptions	R/W	Reset Value
7:3		Reserved		x
2	ENA	Quad Enable. When this field is set to ‘1’, Quad Decoder is enabled.	R/W	
1	INI	Quad Initialize. When this field is set to ‘1’, internal register values of Quad Decoder are initialized.	R/W	
0	MODE	Mode Select. When this field is set to ‘1’, counter value is increased to the point of being changing movement direction. When this field is set to ‘0’, current counter value is decreased to the point of changing movement direction. **Note**: Mode 0 cannot be used due to operation error. For more detail information, refer to ‘[MG245X ERRATA NOTES-004]QUAD DECODER ERRATA’ note.	R/W	0

7.6.11. INTERNAL VOLTAGE REGULATORS

These blocks deliver power to internal blocks from external power source. There are two regulators; one supplies power to RF and analog circuit and the other to digital circuit. To generate 1.5V internal voltage, MSV pin shall be connected to ground. AVREG3V and DVREG3V, the external pins, shall be connected to the 3V power line for the operation of the internal regulators.

7.6.12. 4-CHANNEL 8-BIT SENSOR ADC

This block monitors external sensor output and converts the external analog signal into the corresponding digital value. The output of the sensor ADC is 8-bit wide and sampling frequency is 16KHz at maximum. The controlling registers of ADC are SADCCON(0x22AB), SADCVALH(0x22AC), and SADCVALL(0x22AD).

SADCCON (SENSOR ADC CONTROL REGISTER, 0x22AB)

This register controls sensor ADC operation.

Bit	Name	Descriptions	RW	Reset Value
7	SADCEN	Sensor ADC Enable	RW	0
6	SADCDONE	When conversion is completed, it is set to ‘1’. It shall be cleared for the next conversion.(sampling rate: 8kHz)	RO	0
5:4	SADCREF	Select the reference voltage for the sensor ADC.	RW	0

<table>
<tr><td></td><td></td><td>
<table>
<tr><td>SADCREF</td><td>Reference</td><td>Description</td></tr>
<tr><td>00</td><td>Internal</td><td>REFP = 1.2V
REFM = 0.3V
VMID = 0.75V</td></tr>
<tr><td>01</td><td></td><td>Reserved</td></tr>
<tr><td>10</td><td>External</td><td>REFP = ACH2(0V~1.5V)
REFM = ACH3(ACH3<ACH2)
VMID = (ACH2+ACH3)/2</td></tr>
<tr><td>11</td><td>Internal</td><td>REFP = VDD(1.5V)
REFM = GND
VMID = (VDD+GND)/2</td></tr>
</table>
</td><td></td><td></td></tr>
<tr><td>3:0</td><td>SADCCH</td><td>
Select the input channel of sensor ADC.
<table>
<tr><td>SSADCCH</td><td>Input</td><td>Description</td></tr>
<tr><td>0000</td><td>ACH0</td><td>Single input</td></tr>
<tr><td>0001</td><td>ACH1</td><td>Single input</td></tr>
<tr><td>0010</td><td>ACH2</td><td>Single input</td></tr>
<tr><td>0011</td><td>ACH3</td><td>Single input</td></tr>
<tr><td>0100</td><td>ACH0, ACH1</td><td>Differential input</td></tr>
<tr><td>0101</td><td>ACH2, ACH3</td><td>Differential input</td></tr>
<tr><td>0110</td><td>Temperature Sensor</td><td>Embedded temperature sensor</td></tr>
<tr><td>0111</td><td>Battery Monitor</td><td>Embedded battery monitor</td></tr>
<tr><td>1000</td><td>GND</td><td>Just for calibration</td></tr>
<tr><td>1001</td><td>VDD</td><td>Just for calibration</td></tr>
<tr><td>others</td><td></td><td>Reserved</td></tr>
</table>
</td><td>RW</td><td>0</td></tr>
</table>

SADCVALH (SENSOR ADC OUTPUT VALUE HIGH DATA REGISTER, 0x22AC)

SADCVAL is the output value of sensor ADC and represented by unsigned 16-bit integer. This register represents upper 8-bit data of 16-bit value of SADCVAL. (SADCVAL[15:8])

Bit	Name	Descriptions	RW	Reset Value
7:0	SADCVALH	SADCVAL[15:8]	RO	0x00

SADCVALL (SENSOR ADC OUTPUT VALUE LOW DATA REGISTER, 0x22AD)

This register represents lower 8-bit data of 16-bit value of SADCVAL. (SADCVAL[7:0])

Bit	Name	Descriptions	RW	Reset Value
7:0	SADCVALL	SADCVAL[7:0]	RO	0x00

When the input signals of ACH0~3 vary from 0 to 1.5V, the output value of SADC can be obtained through SADCVAL[15:0]. To obtain valid 8-bit data from SADC, 2-point calibration shall be used with the value of SADCVAL[15:0].

For temperature or battery monitor, 1-point calibration shall be used. For more detailed information, please refer to the application note ‘MG245X Offset Cancellation of Temperature Sensor Programming Guide’ and ‘MG245X Offset Cancellation of BATT Monitor Programming Guide’.

7.6.13. ON-CHIP POWER-ON RESET

This block generates the reset signal to initialize the digital block during power-up. When On-chip regulator output or external battery is used as the power of digital core block and power is provided, it outputs the internal reset signal.

7.6.14. TEMPERATURE SENSOR

To control the functionality of this block, refer to the section 7.6.12. Whenever temperature is increased by 1°C, the output of this block is decreased by -1.65mV/°C. Since the operating range of temperature sensor is about 200mV, and the valid resolution becomes 5 bits.

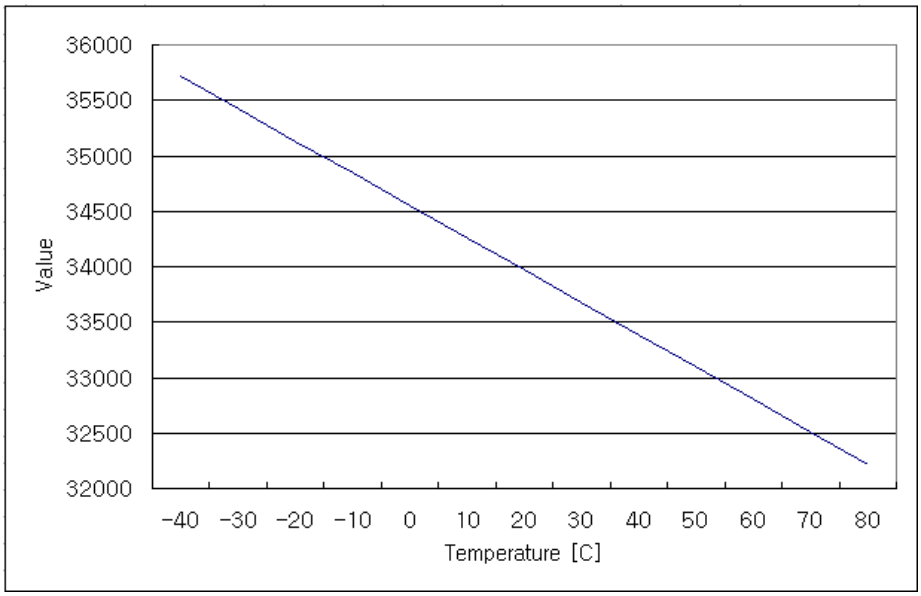


Figure 24. Temperature Sensor Characteristics

Note: Y axis of [Figure 24] represents 16-bit value. The valid output of the temperature sensor lies in the small portion of 16-bit range. To get the valid data, it is recommended to use ADC calibration. To reduce offset between MG245X chips, please refer to 'MG245X Offset Cancellation of Temperature Sensor Programming Guide'.

7.6.15. BATTERY MONITORING

This block is used to monitor the voltage level of supplied power. That is, it can monitor external voltage(3V) level. To control the functionality of this block, refer to the section 7.6.12. [Figure 19] shows the output value of the battery monitor according to the input voltage. Since the battery monitor uses 1/3 level of supply power, the connected voltage level to battery monitor becomes 0.8~1.2V. The input voltage range becomes 0.4V and the valid resolution becomes 6 bits.

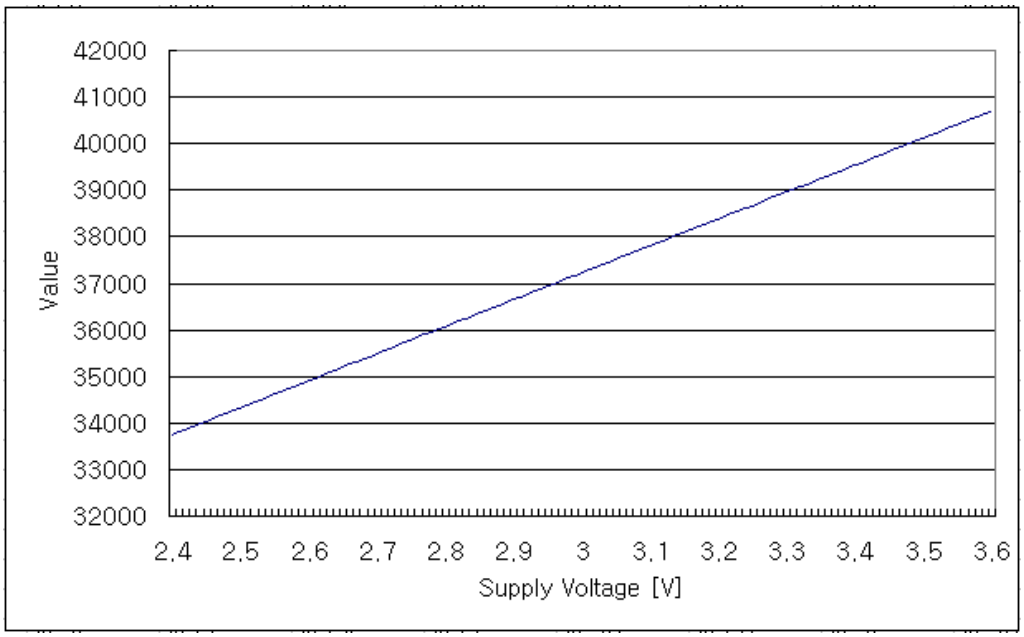


Figure 25. Battery Monitor Characteristics

Note: Y axis of [Figure 25] represents 16-bit value. The valid output of battery monitor lies in the small portion of 16-bit range. To get the valid data, it is recommended to use ADC calibration. To reduce offset between MG245X chips, please refer to 'MG245X Offset Cancellation of BATT Monitor Programming Guide'.

7.7. MAC(Medium Access Control Layer)

The MAC block processes a command received from high layer(MCU), transmits the data received from high layer to baseband modem, or encrypts it and then transmits to baseband modem. In addition, it indicates the status of PHY and transmits the data received from baseband modem to high layer, or transmits the decrypted data to high layer.

The function of the MAC block is to transfer the data from higher layer to PHY block, to send the received data from the PHY to the higher layer with or without encryption or decryption. [Figure 26] shows the MAC block diagram.

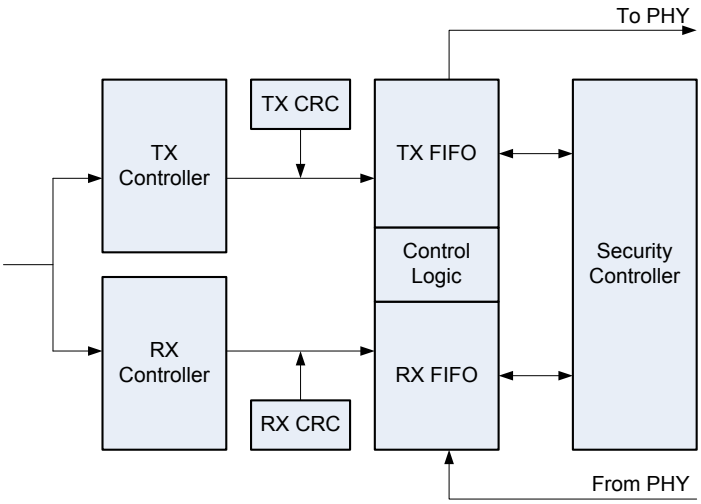


Figure 26. MAC block diagram

IEEE802.15.4 Frame Format

IEEE802.15.4 transmits the data in packets with each packet having a specified frame format. [Figure 27] shows a schematic view of the IEEE 802.15.4 frame format.
The PHY frame to be transmitted consists of preamble, SOF(start of frame delimiter), frame length and PSDU(PHY Service Data Unit) fields. The Preamble is used to adjust the gain of receiving signal and obtain synchronization at the received stage. The start of frame delimiter is used to indicate the starting position of the frame and obtain exact frame timing synchronization. Frame length is 1 byte and it is used to indicate the PSDU length which can vary up to a maximum 127 bytes.

The PSDU contains the MPDU(MAC protocol data unit).

The MPDU means the frame format generated in the MAC layer(medium access control layer) and it is consisted of frame control field, data sequence number, address information, frame payload and FCS(frame check sequence) field.

The area including a frame control field, a data sequence number field, and an address information field, is defined as MAC header. The FCS field is defined as MAC footer. The data which is transmitted from the higher layer is located in the MAC payload. For detailed information on frame format, refer to the IEEE802.15.4 standard.

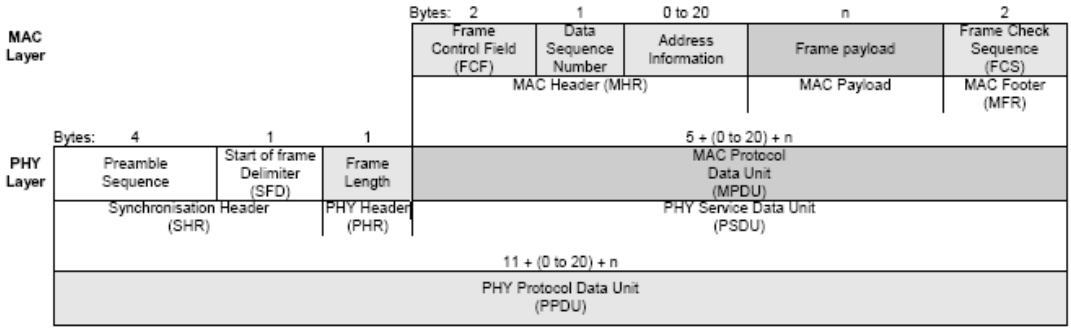


Figure 27. IEEE 802.15.4 Frame Format

Synchronization Header (SHR)

In IEEE802.15.4 standard, a frame format includes SHR(synchronization header) for the purpose of adjusting the gain of the receiving signal, detecting packet and obtaining synchronization.
SHR is consisted of preamble and SFD(Start of Frame Delimiter). The Preamble is formatted by repeating the 8 same symbols('0') in 4 bytes. 1 byte SFD is used to detect the frame start and obtain timing synchronization and it is defined as 0XA7 in IEEE802.15.4 standard.

PHY Header (PHR)

The Length field is used to define the size of the MPDU or the PSDU.
The value clarified in length field doesn't include the length field itself. However, the length of FCS(Frame Check Sequence) is included. The PHY block takes data up to the size defined by

the length field from TX FIFO, and transmits the data.

MAC Header (MHR)

This field is consisted of frame control field (FCF), data sequence number (DSN) and address information. FCF includes the frame information such as frame type or addressing mode and so on. DSN means the sequence of packet. In other words, DSN is incremented after transmitting. Therefore, next packet has a different DSN. For detailed information, refer to the IEEE802.15.4 standard.

MAC Footer (MFR)

This field is called as frame check sequence (FCS) and it follows the last data of MAC payload byte. FCS polynomial is as follows.

$$x16 + x12 + x5 + 1$$

7.7.1. RECEIVED MODE

When receiving the data from PHY block, the MAC block stores the data in RX FIFO.
The data in RX FIFO can be decrypted by PCMD1 (0X2201) register or it can be read by the MRFCPOP(0x2080) register. Data decryption is implemented by AES-128 algorithm, which supports CCM* mode by ZigBee and CTR/CBC-MAC/CCM mode by IEEE 802.15.4. The RX Controller controls the process described above. When decrypting the data, the received frame data length is modified and the modified value is stored in the LSB of each frame by the hardware again.

The size of RX FIFO is 256 bytes and it is implemented by Circular FIFO with a Write Pointer and a Read Pointer. The RX FIFO can store several frame data received from the PHY block. Since the LSB of each frame data represents the frame data length, it can be accessed by the Write pointer and the Read Pointer.

When the data is received from the PHY block, the CRC information is checked to verify data integrity.
When AUTO_CRC control bit of MACCTRL(0x2191) register is set to ‘1’, CRC information is verified by the RX CRC block automatically. To check the result, refer to the CRC_OK field of

MACSTS(0x2180) register. When the value of CRC_OK field is set to ‘1’, there is no problem with CRC information. When the AUTO_CRC control bit of the MACCTRL(0x2191) register is not set to ‘1’, the CRC information should be verified by the software.

When a packet reception is completed in the PHY block, a PHY interrupt is sent to the MCU. In addition, when decryption operation is completed, an AES interrupt is sent to the MCU.

7.7.2. TRANSMIT MODE

To transmit the data from a higher layer(MCU) to the PHY block, the device stores the data in the TX FIFO of the MAC block. When the MCU writes data in MTFCPUSH(0x2000) register, data is stored in TX FIFO of MAC. The size of TX FIFO is 256 byte and it is implemented by a Circular FIFO with a Write Pointer and a Read Pointer. Since each data in TX FIFO is mapped to the memory area in the MCU, it can be written or read directly by the MCU.

The data stored in the TX FIFO can be encrypted by the PCMD1(0x2201) register or is transmitted to PHY block by PCMD0(0x2200) register. The TX Controller controls the process described above. Data encryption is implemented by the AES-128 algorithm, which supports CCM* mode by ZigBee and CTR/CBC-MAC/CCM mode by IEEE 802.15.4. The data length which is to be transmitted is stored in the LSB of each frame by the software when the frame data is stored in TX FIFO by the MCU. When the data in TX FIFO is encrypted, the data length is modified and it is stored by hardware again.

When transmitting the data in TX FIFO, the CRC operation is processed to verify data integrity. When the AUTO_CRC control bit of the MACCTRL (0x2191) register is set to ‘1’, CRC information is generated by TX CRC block automatically. Otherwise, CRC operation should be operated by software.

When data encryption is completed, an AES interrupt is sent to the MCU. When the data transmission to the PHY block is completed, a PHY interrupt is sent to the MCU.

7.7.3. DATA ENCRYPTION AND DECRYPTION

Data encryption or decryption is done by the security controller block. Security Controller consists of the block for processing encryption/decryption operation and the block for controlling. In order to implement CCM* mode by ZigBee and CTR/CBC-MAC/CCM mode by IEEE 802.15.4, 128-bit key value and a nonce are needed. MG245X can have two 128-bit key values, KEY0 and KEY1. For encryption, the desired nonce value should be stored in the TX Nonce and KEY0 or KEY1 should be selected for use. For decryption, the desired nonce value should be stored in the RX Nonce and KEY0 or KEY1 should be selected for use. For more detailed information, refer to the IEEE802.15.4 standard document.

The SAES(0x218E) register is used only for AES operation. In this case, required data for this operation should be stored in SABUF register and KEY0 or KEY1 is should be selected for use.

The following describes the registers for controlling MAC TX FIFO.

MTFCPUSH (TX FIFO PUSH DATA REGISTER, 0x2000)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	MTFCPUSH	When data is written to this register, it is stored in TX FIFO. The size of TX FIFO is 256 byte and it can be accessed by MCU or VTXDMA.	W/O	0x00

MTFCWP (TX FIFO WRITE POINTER REGISTER, 0x2001)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	MTFCWP	TX FIFO Write Pointer Total is 9-bit with MTFCWP8 in MTFCSTS register. It is increased by '1' whenever writing data to TX FIFO.	R/W	0x00

MTFCRP (TX FIFO READ POINTER REGISTER, 0x2002)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	MTFCRP	TX FIFO Read Pointer Total is 9-bit with MTFCRP8 in MTFCSTS register. It is increased by '1' whenever reading data from TX FIFO.	R/W	0x00

MTFCCTL (TX FIFO CONTROL REGISTER, 0x2003)

Bit Field	Name	Descriptions	R/W	Reset Value
7:3		Reserved		0x00
2	ASA	When this field is set to '1', it automatically sets the starting address of packet and the length of packet encrypted by the AES engine to the information of the packet which is to be transmitted.	RW	1
1	ENA	When this field is set to '1', MTXFIFO is enabled.	RW	1
0	CLR	When this field is set to '1', MTFCWP, MTFCRP, MTFCSTS, MTFCSIZE, MTFCRM register are initialized.	RW	0

MTFCSTS (TX FIFO STATUS REGISTER, 0x2004)

Bit Field	Name	Descriptions	R/W	Reset Value
7	MTFCWP8	Total is 9-bit address with MTFCWP register. This field is the MSB, and used to detect wrap around of a circular FIFO.	R/W	0
6	MTFCRP8	Total is 9-bit address with MTFCRP register. This field is MSB, and is used to detect wrap around of circular FIFO.	R/W	0
5:2		Reserved		0
1	FULL	This field is set to '1' when data size in MTXFIFO is 256 byte.	R/O	0
0	EMPTY	This field is set to '1' when data size in MTXFIFO is '0'.	R/O	0

MTFCSIZE (TX FIFO Data Size Register, 0x2005)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	MTFCSIZE	This field represents the number of valid data byte of TX FIFO. This field value is valid when FIFO status is normal and it is calculated by the difference between MTFCWP (0x2001) and MTFCRP (0x2002).	R/O	0x00

MTFCSBASE (TX FIFO AES ENCRYPTION DATA START POINTER REGISTER, 0x2007)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	MTFCSBASE	This field represents the starting address of data to be encrypted by AES engine in the TX FIFO. This field is set by the MCU or is set automatically to the starting address of a packet to be transmitted when the ASA field in the MTFCCTL register is set to '1'.	R/W	0x00

MTFCSLEN (TX FIFO AES ENCRYPTION DATA LENGTH REGISTER, 0x2008)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	MTFCSLEN	This field represents the length of the data to be encrypted by the AES engine in the TX FIFO. This field is set by the MCU or is set automatically to the length of a packet to be transmitted when the ASA field in the MTFCCTL register is set to '1'.	R/W	0x00

The following describes the registers for controlling MAC RX FIFO.

MRFCPOP (RX FIFO POP Data Register, 0x2080)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	MRFCPOP	This register can read data in RX FIFO. The size of RX FIFO is 256 byte and it can be accessed by the MCU or VRXDMA.	W/O	0x00

MRFCWP (RX FIFO WRITER POINTER REGISTER, 0x2081)

Bit Field	Name	Descriptions	R/W	Reset Value
0x2081	MRFCWP	RX FIFO Write Pointer Total is 9-bit with MRFCWP8 in MRFCSTS register. It is increased by '1' whenever data is written to the RX FIFO.	R/W	0x00

MRFCRP (RX FIFO READ POINTER REGISTER, 0x2082)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	MRFCRP	RX FIFO Read Pointer Total is 9-bit with MRFCRP8 in MRFCSTS register. It is increased by '1' whenever reading data from the RX FIFO.	R/W	0x00

MRFCCTL (RX FIFO CONTROL REGISTER, 0x2083)

Bit Field	Name	Descriptions	R/W	Reset Value
7:3		Reserved		0x00
2	ASA	When this field is set to '1', it automatically sets the starting address of a packet and the length of a packet decrypted by the AES engine to the information of received packet.	RW	1
1	ENA	When this field is set to '1', MRXFIFO is enabled.	RW	1

0	CLR	When this field is set to ‘1’, MRFCWP, MRFCRP, MRFCSTS, MRFCSIZE, MRFCRM register are initialized.	RW	0

MRFCSTS (RX FIFO STATUS REGISTER, 0x2084)

Bit Field	Name	Descriptions	R/W	Reset Value
7	MRFCWP8	Total is 9-bit address with MRFCWP register. This field is MSB and is used to detect wrap around of a circular FIFO.	R/W	0
6	MRFCRP8	Total is 9-bit address with MRFCRP register. This field is MSB, and is used to detect wrap around of a circular FIFO.	R/W	0
5:2		Reserved		0
1	FULL	This field is set to ‘1’ when data size in RX FIFO is 256 byte.	R/O	0
0	EMPTY	This field is set to ‘1’ when data size in RX FIFO is ‘0’.	R/O	0

MRFCSIZE (RX FIFO Data Size Register, 0x2085)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	MRFCSIZE	This field represents the number of valid data byte of RX FIFO. This field value is valid when FIFO status is normal and it is calculated by the difference between MRFCWP and MRFCRP.	R/O	0x00

MRFCSBASE (RX FIFO AES DECRYPTION DATA START POINTER REGISTER, 0x2087)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	MRFCSBASE	This field represents the starting address of the data to be decrypted by the AES engine in RX FIFO. This field is set by the MCU or is set automatically to the starting address of the received packet when the ASA field in the MRFCCTL register is set to ‘1’.	R/W	0x00

MRFCSLEN (RX FIFO AES DECRYPTION DATA LENGTH REGISTER, 0x2088)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	MRFCSLEN	This field represents the length of the data to be decrypted by the AES engine in the RX FIFO. This field is set by the MCU or is set automatically to the length of received packet when the ASA field in the MRFCCTL register is set to '1'.	R/W	0x00

The following describes the registers for data transmission /reception and security.

KEY0 (ENCRYPTION KEY0 REGISTERS, 0x2100~0x210F)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	KEY0	This register is 16-byte key used for the AES operation. 0x210F: MSB of KEY value 0x2100: LSB of KEY value	R/W	0x00

RXNONCE (RX NONCE REGISTERS, 0x2110~0x211C)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	RXNONCE	This register is used for decryption operation when receiving a packet. It consists of 13-bytes: the Source Address(8-byte), the Frame Counter(4-byte) and the Key Sequence Counter(1-byte). 0x211C : MSB of Source Address 0x2115 : LSB of Source Address 0x2114 : MSB of Frame Counter 0x2111 : LSB of Frame Counter 0x2110 : Key Sequence Counter	R/W	0x00

SAESBUF (STANDALONE AES OPERATION BUFFER REGISTERS, 0x2120~0x212F)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	SAESBUF	This register is used for storing data only when processing an AES-128 operation by the AES engine. After the AES-128 operation, the result is stored in this register. 0x212F : MSB of Plaintext and Ciphertext 0x2120 : LSB of Plaintext and Ciphertext	R/W	0x00

KEY1 (ENCRYPTION KEY1 REGISTERS, 0x2130~0x213F)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	KEY1	This register is 16-byte KEY for the AES operation. 0x213F : MSB of KEY value 0x2130 : LSB of KEY value	R/W	0x00

TXNONCE (TX NONCE REGISTERS, 0x2140~0x214C)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	TXNONCE	This register is used for the encryption operation when transmitting a packet. It consists of 13-bytes: the Source Address(8-byte), the Frame Counter(4-byte) and the Key Sequence Counter(1-byte). 0x214C : MSB of Source Address 0x2145 : LSB of Source Address 0x2144 : MSB of Frame Counter 0x2141 : LSB of Frame Counter 0x2140 : Key Sequence Counter	R/W	0x00

The following three addresses are used for network compatible with IEEE802.15.4. EXTADDR is the unique address for the chip or module allocated by IEEE 802.15.4. PANID is the network ID which allows each network to be identified when a network is configured. SHORTADDR is the short address of a device in IEEE802.15.4 network. It allows each device to be identified in same network. SHORTADDR can be changed whenever connecting to the network.

EXTADDR (EXTENDED ADDRESS REGISTERS, 0x2150~0x2157)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	EXTADDR	This register stores 64-bit IEEE address. 0x2157 : MSB of IEEE address 0x2150 : LSB of IEEE address	R/W	0x00

PANID (PANID REGISTERS, 0x2158~0x2159)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	PANID	This register stores 16-bit PAN ID. 0x2159 : PAN ID[15:8] 0x2158 : PAN ID[7:0]	R/W	0x00

SHORTADDR (SHORTADDRESS REGISTERS, 0x215A~0x215B)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	SHORTADDR	This register stores Short address(Network address). 0x215B : Short address[15:8] 0x215A : Short address[7:0]	R/W	0x00

MACSTS (MAC STATUS REGISTER, 0x2180)

Bit Field	Name	Descriptions	R/W	Reset Value
7	ENC/DEC	When this field is set to ‘1’, there is data in the AES encryption or decryption operation. Can only be read.	R/O	0
6	TX_BUSY	When this field is set to ‘1’, data in the MAC FIFO is transmitted to a modem. Can only be read.	R/O	0
5	RX_BUSY	When this field is set to ‘1’, data is transmitted from a modem to the MAC FIFO. Can only be read.	R/O	0
4	SAES_DONE	When Standalone AES operation is finished, this field is set to ‘1’. It is cleared by MCU.	R/W	0
3	DECODE_OK	This field checks the validity of data according to the type of data received or the address mode. If there is no problem, this field is set to ‘1’.	R/O	0

		Can only be read.		
2	ENC_DONE	When AES Encryption operation is finished, this field is set to ‘1’. It is cleared by MCU.	R/W	0
1	DEC_DONE	When AES Decryption operation is finished, this field is set to ‘1’. It is cleared by MCU.	R/W	0
0	CRC_OK	If there is no problem for checking CRC of received packet, this field is set to ‘1’.	R/W	0

MACSAES (SAES RUN REGISTER, 0x218E)

Bit Field	Name	Descriptions	R/W	Reset Value
7:1		Reserved	W/O	0
0	SAES	When this field is set to ‘1’, the AES operation is done by data in SAESBUF and KEY selected by the SA_KEYSEL field in the SEC register. This field is automatically cleared.	W/O	0

MACRST (MAC RESET CONTROL REGISTER, 0x2190)

Bit Field	Name	Descriptions	R/W	Reset Value
7	RST_FIFO	When this field is set to ‘1’, the MAC FIFO is initialized.	R/W	0
6	RST_TSM	When this field is set to ‘1’, the MAC Transmitter State Machine is initialized.	R/W	0
5	RST_RSM	When this field is set to ‘1’, the MAC Receiver State Machine is initialized.	R/W	0
4	RST_AES	When this field is set to ‘1’, the AES Engine is initialized.	R/W	0
3:0		Reserved		0

MACCRTL (MAC CONTROL REGISTER, 0x2191)

Bit Field	Name	Descriptions	R/W	Reset Value
7:5		Reserved		0
4	PREVENT_ACK	When this field is set to ‘1’, RX interrupt doesn’t occur when the DSN field of received ACK packet is different from the value in MACDSN	R/W	0

		register during packet reception.		
3	PAN_COORDINATOR	When this field is set to ‘1’, function for PAN Coordinator is enabled.	R/W	0
2	ADR_DECODE	When this field is set to ‘1’, the RX interrupt doesn’t occur when address information of the received packet is not matched with device itself.	R/W	1
1	AUTO_CRC	When this field is set to ‘1’, the RX interrupt doesn’t occur when the CRC of the received packet is not valid.	R/W	1
0		Should be set to ‘0’.		0

MACDSN (MAC DSN REGISTER, 0x2192)

Bit Field	Name	Descriptions	R/W	Reset Value
7:0	MACDSN	Valid if only PREVENT_ACK in MACCTRL is set to ‘1’. This register sets the DSN field value of the received ACK packet, which can cause a PHY(RX) interrupt. In other words, if the DSN field of the received ACK packet is not equal to MACDSN, the PHY(RX) interrupt does not occurred.	R/W	0x00

MACSEC (MAC SECURITY REGISTER, 0x2193)

Bit Field	Name	Descriptions	R/W	Reset Value
7	SA_KEYSEL	Select KEY value for Standalone SAES operation. When this field is ‘1’, KEY1 is selected and when ‘0’, KEY0 is selected.	R/W	0
6	TX_KEYSEL	Selects the KEY value for AES operation during packet transmission. When this field is ‘1’, KEY1 is selected and when ‘0’, KEY0 is select.	R/W	0
5	RX_KEYSEL	Selects KEY value for AES operation when packet reception. When this field is ‘1’, KEY1 is selected and when ‘0’, KEY0 is selected.	R/W	0
4:2	SEC_M	In CBC-MAC operation, it represents the data length used in the	R/W	0

<table>
<tr><td></td><td></td><td>authentication field as byte unit.

<table><tr><th>SEC_M</th><th>Authentication Field Length</th></tr><tr><td>0</td><td>Reserved</td></tr><tr><td>1</td><td>4</td></tr><tr><td>2</td><td>6</td></tr><tr><td>3</td><td>8</td></tr><tr><td>4</td><td>10</td></tr><tr><td>5</td><td>12</td></tr><tr><td>6</td><td>14</td></tr><tr><td>7</td><td>16</td></tr></table></td><td></td><td></td></tr>
<tr><td>1:0</td><td>SEC_MODE</td><td>Security Mode.
0: No Security
1: CBC-MAC mode
2: CTR mode
3: CCM mode</td><td>R/W</td><td>0</td></tr>
</table>

TXAL (TX AUXILIARY LENGTH REGISTER, 0x2194)

Bit Field	Name	Descriptions	R/W	Reset Value
7		Reserved	R/W	0
6:0	TXAL	This field represents the length used in the AES operation for the packet to be transmitted. It has a different meaning for each security mode as follows; Security mode: CTR It represents the number of bytes between length byte and the data to be encoded or decoded of data in FIFO. Security mode: CBC-MAC It represents the number of byte between length byte and the data to be authenticated. Security mode: CCM It represents the length of data which is used not in encoding or decoding but authentication.	R/W	0x00

RXAL (RX AUXILIARY LENGTH REGISTER, 0x2195)

Bit Field	Name	Descriptions	R/W	Reset Value
7		Reserved	R/W	0
6:0	RXAL	This field represents the length used in the AES operation for the received packet and it has a different meaning for each security mode as follows. Security mode: CTR It represents the number of bytes between length byte and the data to be encoded or decoded of data in FIFO. Security mode: CBC-MAC It represents the number of bytes between length byte and the data to be authenticated. Security mode: CCM It represents the length of data which is used not in encoding or decoding but authentication.	R/W	0x00

7.8. PHY

Physical Layer (PHY), also called the modem block, is used as follows;

- With the MAC block, the data to be transmitted is digitally modulated and then sent to the RF block for transmission.
- With the MAC block, the RF signal received via the RF block is digitally demodulated and sent to the MAC block.

The modulation starts from fetching the data in the TX FIFO. After appending the preamble, SFD and length field to the data, a frame, which is compatible to IEEE802.15.4 standard, is generated. This frame is mapped to symbols via Bit-to-Symbol conversion as shown in [Figure 28] below. Bit-to-Symbol conversion maps 4 bit to 1 symbol. Each symbol is spread by Symbol-to-Chip mapping. The Spread symbol is then modulated to a quadrature signal of constant envelope via Offset Quadrature Phase Shift Keying(O-QPSK) modulation and the Half Sine Filtering.

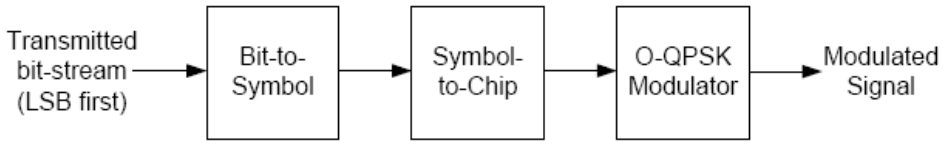


Figure 28. IEEE 802.15.4 Modulation

Symbol-to-Chip mapping is used for spreading the symbol bandwidth to improve the reception performance. [Figure 29] shows the mapping rule of chip sequences corresponding to each symbol.

Symbol	Chip sequence (C_0, C_1, C_2, … , C_{31})
0	1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0
1	1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0
2	0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0
3	0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1
4	0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1
5	0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0
6	1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1
7	1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1
8	1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1
9	1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1
10	0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1
11	0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0
12	0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0
13	0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1
14	1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0
15	1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0

Figure 29. Spreading sequence of 32 chip

[Figure 24] shows the quadrature signal modulated.

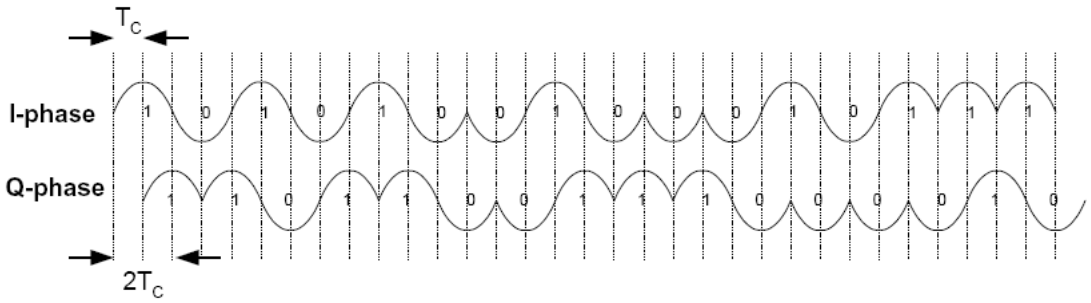


Figure 30. Quadrature modulated finally

The Modulated signal is converted to analog by the DAC and then passed to RF block.

The output signal of the DAC is fed to the Quadrature(I/Q) Up-conversion Mixer through the Low Pass Filter(LPF) and then amplified by the Power Amplifier (PA) and transmitted to the antenna.

When an RF signal is received by the antenna, it is amplified by the LNA(low noise amplifier) in the RF block. It is then down-converted to a base-band signal by the Quadrature Down-conversion Mixer. After low pass filtering, the analog signal is amplified through the Variable Gain Amplifier(VGA) and converted to a digital signal by the ADC.

The output signal of the ADC is digitally demodulated by the modem block. Digital demodulation process includes for example, Automatic Gain Control(AGC), De-spreading, Symbol Detection, and Timing Synchronization. When a frame delimiter is detected on the demodulated signal, a modem block generates the interrupt which indicates the start of a packet.

The length and the frame body followed by frame delimiter are stored in RX FIFO of MAC. When the last data is stored, an interrupt is generated to indicate the end of packet reception. After a packet reception interrupt occurs, a user can read the data in TX FIFO by software.
When a packet is received, a modem block provides Received Signal Strength Indication(RSSI) automatically. RSSI is measured by averaging the power level of received signal for a defined period of time.

It can be used as a LQI(Link Quality Indicator) to decide the quality of the communication channel.

RSSI is stored in a special register and the stored RSSI value is kept until a new packet is received. After a packet reception interrupt occurs, a user can read the value stored in RSSI register by software. While a packet is not being received, the modem block continuously provides the RSSI of the RF signal at antenna. Measured RSSI is used to decide the communication channel state. Clear Channel Assessment(CCA) operation is based on this information. The CCA operation is used to prevent a collision when multiple-users try to use a channel simultaneously. When a channel is determined to be busy, packet transmission is deferred until the channel state changes to idle.

7.8.1. INTERRUPT

The modem block provides four interrupts to notify the MCU of specific events.

▪ RX End Interrupt (RXEND_INT)

This interrupt notifies the MCU of the completion of a packet reception. When this interrupt has been generated, the user can check the received data in RX FIFO.

Also, the quality of the transmission channel is checked by reading the register, which stores the RSSI of the received packet.

▪ RX Start Interrupt (RXSTART_INT)

This interrupt notifies the MCU of the start of a packet reception. When the packet reception has been started, all the reception is processed by the hardware.

Note: It is not recommended to use RX Start Interrupt normally.

▪ TX End Interrupt (TXEND_INT)

This interrupt notifies the MCU of the start of a packet transmission. A new packet cannot be transmitted until a packet transmission is completed. When a communication channel is busy, a TX End Interrupt can be delayed until a communication channel goes to the idle state and the transmission is completed successfully.

▪ Modem Ready Interrupt (MDREADY_INT)

This interrupt notifies the MCU that the modem block has changed from the idle state to the ready state due to the modem-on request. The modem block is in the idle state when the supply power is turned on but needs to be changed to the ready state in order to transmit or receive the packet. This interrupt occurs when RF block has stabilized following the modem-on request.

The user can check whether each interrupt described above occurs through the INTSTS register. The INTCON register can be set to disable the interrupts desired.

The Modem block provides the INTIDX register with information from the INTSTS register to check whether an interrupt occurs has occurred. When multiple interrupts occur simultaneously, INTSTS register shows all the interrupts that have occurred. The INTIDX register notifies whether an interrupt is enabled in the order based on the priority of the interrupt. When a user reads INTSTS or INTIDX register, all interrupts is initialized.

7.8.2. REGISTERS

The registers of the modem block either control or report the state of the modem block. The registers, which influence on transmission performance of the modem block, should be set with the values provided by RadioPulse Inc. and should not be modified by a user application program.

[Table 10] lists the registers in the PHY Layer of the MG245X. The address of each register is assigned to a data memory area in microcontroller, so a user application program can read and write the register as a general memory.

Table 10. PHY Register Address Map

Address (Hex)	Name	Description	Initial Value
2200	PCMD0	PHY Command0	11111100
2201	PCMD1	PHY Command1	11000111
2202	PLLPD	PLL Power-Down	11100000
2203	PLLPU	PLL Power-Up	11111111
2204	RXRFPD	RF RX Path Power-Down	00000000
2205	RXRFPU	RF RX Path Power-Up	11111111
2206	TXRFPD	RF TX Path Power-Down	11010000
2207	TXRFPU	RF TX Path Power-Up	11111111
220D	TRSWBC	TRSWB Control	00000000
2211	RXFRM1	RX Frame Format1	00000010
2212	SYNCWD	SYNC Word Register	10100111
2213	TDCNF3	Operation Delay Control 3	01001111
2217	TDCNF0	Operation Delay Control 0	01100011
2215	TXFRM1	TX Frame Format1	11110010
2223	AGCCNF3	AGC Configuration3	01111111
2248	CCA0	CCA Control0	11000000
2249	CCA1	CCA Control1	10110010
224A	CCA2	CCA Control2	00000001
224B	CCA3	CCA Control3	11110100
2260	TST	Test Register	10000000

2261	TST1	Test Configuration1	01101100
2262	TST2	Test Configuration2	11111111
2263	TST3	Test Configuration3	00001111
226D	TST13	Test Configuration13	00000000
226E	TST14	Test Configuration14	01000000
2270	PHYSTS0	PHY Status0	10000000
2271	PHYSTS1	PHY Status1	11110000
2272	AGCSTS0	AGC Status0	11111111
2273	AGCSTS1	AGC Status1	11011111
2274	AGCSTS2	AGC Status2	00000000
2275	AGCSTS3	AGC Status3	00000000
2277	INTCON	PHY Interrupt Control	11110000
2278	INTIDX	PHY Interrupt Status and Index	11111100
227E	INTSTS	PHY Interrupt Status	11111111
220D	TRSWC0	TRSW Control 0	00000000
2279	TRSWC1	TRSW Control 1	10010000
2286	PLL0	PLL Frequency Control 0	00111000
2287	PLL1	PLL Frequency Control 1	01000000
2288	PLL2	PLL Frequency Control 2	00000000
228B	PLL3	PLL Frequency Control 3	00110010
2289	PLL4	PLL Frequency Control 4	00101111
228A	PLL5	PLL Frequency Control 5	00010100
22A0	TXPA0	TX PA Control 0	00011000
22A1	TXPA1	TX PA Control 1	11111000
22A2	TXPA2	TX PA Control 2	10010110

The following describes PHY registers.

PCMD0 (PHY COMMAND0 REGISTER, 0x2200)

This register is used to control the operation of a modem block.

Bit Field	Name	Descriptions	R/W	Reset Value
7	MDOFF	Modem-off Request. When this field is set to '0', the modem block status is changed to OFF. In the OFF state, the RF block is in a power-down state and the modem block is in the reset state. In this state, the MG245X cannot receive or transmit packets. For the transmission or the reception of a packet, the modem block needs to be changed to ON state. When the modem block goes to OFF state, this field is set to '1' automatically by the hardware.	R/W	1
6	MDON	Modem-on Request. When this field is set to '0', a modem block status is changed to ON. In ON state,the RF and modem blocks are in the TX or RX ready state. In this state, the modem block controls power-down or power-up for the transmitter or the receiver without an active user application program. When the modem block goes to ON status, this field is set to '1' automatically by the hardware.	R/W	1
5:4		Reserved		11
3	TXSTP	Packet Transmission Stop Request. When this field is set to '0' while a packet is being transmitted, the packet transmisson is stops. The modem block changes to the RX ready state after a defined delay.	R/W	1
2	TXREQ	Packet Transmission Request. When this field is set to '0', the modem block transmits a packet. When a packet transmission is requested, the modem block changes to the TX ready state after defined delay. Only when a communication channel is in idle state(CCA='1'), will the packet be transmitted. When the channel is in busy state(CCA='0'), the transmission is deferred until the channel state goes to idle. This field	R/W	1

<table>
<tr><td></td><td></td><td>is set to’1’ automatically by hardware after completing the transmission. When the packet transmission is completed successfully, a TXEND-INT interrupt is sent. If the packet transmission is abnormal, the interrupt in not sent and the TXREQ field is set to ‘1’.</td><td></td><td></td></tr>
<tr><td>1</td><td>TXON</td><td>TX Path On.
With the TXOFF field, enables the modulation circuit. When the TXON field is set to ‘1’, the modulation circuit of the modem block is always enabled. The following table shows whether the modulation circuit is enabled based on the values of the TXON and TXOFF fields. When TXON and TXOFF are both set to ’0’, the modem block automatically enables the modulation circuit during packet transmission and disables the modulation circuit during packet reception. It is recommended that both TXON and TXOFF field be set to ‘0’.

<table><tr><th>TXON</th><th>TXOFF</th><th>Modulation Circuit Status</th></tr><tr><td>1</td><td>1</td><td>Always enabled</td></tr><tr><td>1</td><td>0</td><td>Always enabled</td></tr><tr><td>0</td><td>1</td><td>Always disabled</td></tr><tr><td>0</td><td>0</td><td>Enabled or disabled depending on the control of a modem block.</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>0</td><td>RXON</td><td>RX Path On.
With the RXOFF field, enables the demodulation circuit. When RXON field is set to ‘1’, the demodulation circuit of a modem block is always enabled. The following table shows the status of the the demodulation circuit, based on the values of RXON and RXOFF fields. When RXON and RXOFF are set to ’0’, the modem block automatically enables the demodulation circuit during packet reception and disables the demodulation circuit during packet transmission.</td><td>R/W</td><td>0</td></tr>
</table>

		<table><tr><th>RXON</th><th>RXOFF</th><th>Demodulation Circuit Status</th></tr><tr><td>1</td><td>1</td><td>Always enabled</td></tr><tr><td>1</td><td>0</td><td>Always enabled</td></tr><tr><td>0</td><td>1</td><td>Always disabled</td></tr><tr><td>0</td><td>0</td><td>Enabled or disabled depending on the control of a modem block</td></tr></table>		

PCMD1 (PHY COMMAND1 REGISTER, 0x2201)

This register is used to control the operation of the modem block.

Bit Field	Name	Descriptions	RW	Reset Value
7:6		Reserved		11
5	DECS	Decryption Start. When DECS field is set to '1', the decryption is processed at the MAC block. When the encrypted packet is received, the data stored in RX FIFO should be decrypted. The decrypted data is stored in RX FIFO again.When the decryption is completed, the interrupt occurs at MAC block. The setting of the DECS field is not cleared automatically after completing decryption and therefore, should be cleared by the software.	R/W	0
4	ENCS	Encryption Start When ENCS field is set to '1', the encryption is processed at MAC block. When the transmission of secured packet is needed, the data stored in TX FIFO should be encrypted. The encrypted data is stored in TX FIFO again. When the encryption is completed, the interrupt occurs at MAC block. The setting of ENCS field is not cleared automatically after completing encryption and therefore, should be cleared by the software.	R/W	0
3:2		Reserved		01

1	TXOFF	TX Path Off. It is used to disable the modulation circuit with TXON field. When TXON field is set to '0' and TXOFF field is set to'1', the modulation circuit of a modem block is always disabled.	R/W	1
0	RXOFF	RX Path Off. It is used to disable the demodulation circuit with RXON field. When RXON field is set to '0' and RXOFF field is set to '1', the demodulation circuit of a modem block is always disabled.	R/W	1

PLLPD (PLL POWER-DOWN REGISTER, 0x2202)

This register is used to control the power-down of the circuits related to the PLL.(Phase-locked Loop)

<table>
<tr><th>Bit Field</th><th>Name</th><th>Descriptions</th><th>RW</th><th>Reset Value</th></tr>
<tr><td>7:5</td><td></td><td>Reserved</td><td></td><td>111</td></tr>
<tr><td>4</td><td>PLLRSTS</td><td>PLL Reset Set.
PLLRSTS field is used to reset the PLL circuit. When the PLLRSTS field is set to '0' and PLLRSTC field is set to '1', PLL circuit held in reset. The following table shows PLL circuit reset state based on the values of the PLLRSTC and PLLRSTS fields.
<table>
<tr><th>PLLRSTS</th><th>PLLRSTC</th><th>PLL reset state</th></tr>
<tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr>
<tr><td>1</td><td>0</td><td>Always in non-reset</td></tr>
<tr><td>0</td><td>1</td><td>Always in reset</td></tr>
<tr><td>0</td><td>0</td><td>Always in non-reset</td></tr>
</table></td><td>R/W</td><td>0</td></tr>
<tr><td>3</td><td>VCOBPD</td><td>Voltage Controlled Oscillator Buffer Power-down.
The VCOBPD and VCOBPDU fields control the Voltage Controlled Oscillator (VCO) Buffer circuit. In power-down state, the VCO Buffer circuit is disabled and draws no</td><td>R/W</td><td>0</td></tr>
</table>

<table>
<tr><td></td><td></td><td>current. When the VCOBPU field is set to ‘1’ and the VCOBPD field is set to ‘0’, the VCO Buffer circuit is in the power-down state.The following table shows the VCO buffer circuit state based on the VCOBPD and VCOBPU fields.

<table><tr><th>VCOBPD</th><th>VCOBPU</th><th>VCO Buffer reset state</th></tr><tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr><tr><td>1</td><td>0</td><td>Always in power-up state</td></tr><tr><td>0</td><td>1</td><td>Always in power-down state</td></tr><tr><td>0</td><td>0</td><td>Always in power-up state</td></tr></table></td><td></td><td></td></tr>
<tr><td>2</td><td>VCOPD</td><td>Voltage Controlled Oscillator Power-down. With the VCOPU field, controls the power-down state of the Voltage Controlled Oscillator (VCO) circuit. In power-down state, VCO circuit is disabled and draws no current. When the VCOPU field is set to ‘1’ and the VCOPD field is set to’0’, the VCO circuit is in the power-down state.The following table shows the VCO circuit state based on the values of the VCOPD and VCOPU fields.

<table><tr><th>VCOPD</th><th>VCOPU</th><th>VCO state</th></tr><tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr><tr><td>1</td><td>0</td><td>Always power-up state.</td></tr><tr><td>0</td><td>1</td><td>Always power-down state</td></tr><tr><td>0</td><td>0</td><td>Always power-up state</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>1</td><td>DIVPD</td><td>Divider Power-down.
With the DIVPU field, controls the power-down state of the Divider circuit. In power-down state, the Divider circuit is disabled and draws no current. When DIVPU field is</td><td>R/W</td><td>0</td></tr>
</table>

<table>
<tr>
<td></td>
<td></td>
<td>set to ‘1’ and then DIVPD field is set to’0’, Divider circuit is in power-down state.The following table shows Divider circuit state based on the values of the DIVPD and DIVPU fields.
<table>
<tr><th>DIVPD</th><th>DIVPU</th><th>Divider state</th></tr>
<tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr>
<tr><td>1</td><td>0</td><td>Always power-up state.</td></tr>
<tr><td>0</td><td>1</td><td>Always power-down state</td></tr>
<tr><td>0</td><td>0</td><td>Always power-up state</td></tr>
</table>
</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>CPPD</td>
<td>Charge Pump Power-down.
With the CPPU field, controls the power-down state of the Charge Pump(CP) circuit. In power-down state, the CP circuit is disabled and draws no current. When the CPPU field is set to ‘1’, and the CPPD field is set to’0’, the CP circuit is in power-down state. The following table shows CP circuit state based on the values of the CPPD and CPPU field .
<table>
<tr><th>CPPD</th><th>CPPU</th><th>CP state</th></tr>
<tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr>
<tr><td>1</td><td>0</td><td>Always power-up state.</td></tr>
<tr><td>0</td><td>1</td><td>Always power-down state</td></tr>
<tr><td>0</td><td>0</td><td>Always power-up state.</td></tr>
</table>
</td>
<td>R/W</td>
<td>0</td>
</tr>
</table>

PLLPU (PLL POWER-UP REGISTER, 0x2203)

This register is used to control the power-up of circuits related to PLL (Phase-locked Loop)

Bit Field	Name	Descriptions	R/W	Reset Value
7:5		Reserved		111
4	PLLRSTC	PLL Reset Clear. PLLRSTC field is used to release the reset PLL circuit. When PLLRSTC field is set to '0', the reset of PLL circuit is released.	R/W	1
3	VCOBPU	Voltage Controlled Oscillator Buffer Power-up. It controls the power-up state of the VCO Buffer circuit. In power-up state, the VCO Buffer circuit is enabled. When VCOBPU field is set to '0', the VCO Buffer circuit is in power-up state. See VCOBPD above for the truth table.	R/W	1
2	VCOPU	Voltage Controlled Oscillator Power-up. It controls the power-up state of the VCO circuit. In power-up state, the VCO circuit is enabled. When VCOPU field is set to '0', VCO circuit is in a power-up state. See VCOPD above for the truth table.	R/W	1
1	DIVPU	Divider Power-up. It controls the power-up state of the Divider circuit. In power-up state, the Divider circuit is enabled. When DIVPU field is set to '0', Divider circuit is in power-up state. See DIVPD above for the truth table.	R/W	1
0	CPPU	Charge Pump Power-up. It controls the power-up state of the CP circuit. In power-up state, CP circuit is enabled. When CPPU field is set to '0', CP circuit is in a power-up state. See CPPD above for truth table.	R/W	1

RXRFPD (RF RX PATH POWER-DOWN REGISTER, 0x2204)

This register is used to power down circuits related to reception in RF block.

Bit Field	Name	Descriptions	R/W	Reset Value
7	LNAPD	Low Noise Amplifier Power-down. With the LNAPU field, controls the power-down state of the LNA circuit. In power-down state, the LNA circuit is disabled and draws no current. When the LNAPU field is set to '1' and the LNAPD field is set to'0', the LNA circuit is in power-down state. The following table shows the LNA circuit state based on the values of LNAPD and LNAPU fields.	R/W	0

<table>
<tr><td></td><td></td><td>
<table>
<tr><th>LNAPD</th><th>LNAPU</th><th>LNA state</th></tr>
<tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr>
<tr><td>1</td><td>0</td><td>Always power-up state.</td></tr>
<tr><td>0</td><td>1</td><td>Always power-down state</td></tr>
<tr><td>0</td><td>0</td><td>Always power-up state.</td></tr>
</table>
</td><td></td><td></td></tr>
<tr><td>6</td><td>RMIXPD</td><td>RX Mixer Power-down.
With the RMIXPU field, controls power-down state of the RX Mixer circuit. In power-down state, the RX Mixer circuit is disabled and draws no current. When the RMIXPU field is set to ‘1’ and the RMIXPD field is set to’0’, the RX Mixer circuit is in power-down state. The following table shows RX Mixer circuit state based on the valuesof the RMIXPD and RMIXPU fields.
<table>
<tr><th>RMIXPD</th><th>RMIXPU</th><th>RX Mixer state</th></tr>
<tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr>
<tr><td>1</td><td>0</td><td>Always power-up state.</td></tr>
<tr><td>0</td><td>1</td><td>Always power-down state</td></tr>
<tr><td>0</td><td>0</td><td>Always power-up state</td></tr>
</table>
</td><td>R/W</td><td>0</td></tr>
<tr><td>5</td><td>BBAMPPD</td><td>Base-band Analog Amplifier Power-down.
With the BBAMPPU field, controls the power-down state of the Base-band Analog Amplifier(BBAMP) circuit. In power-down state, BBAMP circuit is disabled and draws no current. When the BBAMPPU field is set to ‘1’ and the BBAMPPD field is set to’0’, BBAMP circuit is in a power-down state.The following table shows BBAMP circuit state based on the values of the BBAMPPD and BBAMPPU fields.
<table>
<tr><th>BBAMPPD</th><th>BBAMPPU</th><th>BBAMP state</th></tr>
<tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr>
<tr><td>1</td><td>0</td><td>Always power-up state.</td></tr>
<tr><td>0</td><td>1</td><td>Always power-down</td></tr>
</table>
</td><td>R/W</td><td>0</td></tr>
</table>

<table>
<tr><td></td><td></td><td><table>
<tr><td></td><td></td><td>state</td></tr>
<tr><td>0</td><td>0</td><td>Always power-up state</td></tr>
</table></td><td></td><td></td></tr>
<tr><td>4</td><td>RMIXBUFPD</td><td>RF RX Mixer Buffer Power-down.
With the RMIXBUFPU field, controls the power-down state of the RX Mixer Buffer circuit. In power-down state, the RX Mixer Buffer circuit is disabled and draws no current. When the RMIXBUFPU field is set to ‘1’ and the RMIXBUFPD field is set to’0’, RX Mixer Buffer circuit is in a power-down state. The following table shows RX Mixer Buffer circuit state based on the values of the RMIXBUFPD and RMIXBUFPU fields.<table>
<tr><th>RMIXBUFPD</th><th>RMIXBUFPU</th><th>RX Mixer Buffer state</th></tr>
<tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr>
<tr><td>1</td><td>0</td><td>Always power-up state.</td></tr>
<tr><td>0</td><td>1</td><td>Always power-down state</td></tr>
<tr><td>0</td><td>0</td><td>Always power-up state.</td></tr>
</table></td><td>R/W</td><td>0</td></tr>
<tr><td>3</td><td></td><td>This field is reserved and should be fixed to ‘0’.</td><td>R/W</td><td>0</td></tr>
<tr><td>2</td><td>RLPFPD</td><td>RX Low-pass Filter Power-down.
With the RLPFPU field, controls the power-down state of the RX Low-pass Filter(LPF) circuit. In power-down state, the RX LPF circuit is disabled and draws no current. When the RLPFPU field is set to ‘1’ and the RLPFPD field is set to’0’, the RX LPF circuit is in power-down state. The following table shows RX LPF circuit state based on the values of the RLPFPD and RLPFPU field.<table>
<tr><th>RLPFPD</th><th>RLPFPU</th><th>RX LPF state</th></tr>
<tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr>
<tr><td>1</td><td>0</td><td>Always power-up state.</td></tr>
<tr><td>0</td><td>1</td><td>Always power-down state.</td></tr>
</table></td><td>R/W</td><td>0</td></tr>
</table>

<table>
<tr><td></td><td></td><td><table><tr><td>0</td><td>0</td><td>Always power-up state.</td></tr></table></td><td></td><td></td></tr>
<tr><td>1</td><td>VGAPD</td><td>Variable Gain Amplifier Power-down.
With the VGAPU field, controls the power-down state of the ADC circuit. In power-down state, the VGA circuit is disabled and draws no current. When VGAPU field is set to ‘1’ and the VGAPD field is set to’0’, the VGA circuit is in power-down state. The following table shows the VGA circuit state based on the values of the VGAPD and VGAPU fields.<table><tr><th>VGAPD</th><th>VGAPU</th><th>VGA state</th></tr><tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr><tr><td>1</td><td>0</td><td>Always power-up state.</td></tr><tr><td>0</td><td>1</td><td>Always power-down state.</td></tr><tr><td>0</td><td>0</td><td>Always power-up state.</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>0</td><td>ADCPD</td><td>Analog-to-Digital Converter Power-down.
With the ASCPU field, controls the power-down state of the ADC circuit. In power-down state, the ADC circuit is disabled and draws no current. When the ADCPU field is set to ‘1’ and the ADCPD field is set to’0’, the ADC circuit is in a power-down state. The following table shows the ADC circuit state based on the values of the ADCPD and ADCPU fields.<table><tr><th>ADCPD</th><th>ADCPU</th><th>ADC state</th></tr><tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr><tr><td>1</td><td>0</td><td>Always power-up state.</td></tr><tr><td>0</td><td>1</td><td>Always power-down state.</td></tr><tr><td>0</td><td>0</td><td>Always power-up state.</td></tr></table></td><td>R/W</td><td>0</td></tr>
</table>

RXRFPU (RF RX PATH POWER-UP REGISTER, 0x2205)

This register is used to power up the circuits related to reception in RF block.

Bit Field	Name	Descriptions	R/W	Reset Value
7	LNAPU	Low Noise Amplifier Power-up. It controls the power-up state of the LNA circuit. In power-up state, the LNA circuit is enabled When the LNAPU field is set to '0', the LNA circuit is in power-up state. See LNAPD above fot truth table.	R/W	1
6	RMIXPU	RX Mixer Power-up. It controls the power-up state of the RX Mixer circuit. In power-up state, RX Mixer circuit is enabled.When the RMIXPU field is set to '0', the RX Mixer circuit is in power-up state. See RMIXPD above for truth table.	R/W	1
5	BBAMPPU	Base-band Analog Amplifier Power-up. It controls the power-up state of the BBAMP circuit. In power-up state, the BBAMP circuit is enabled. When the BBAMPPU field is set to '0', the BBAMP circuit is in power-up state. See BBAMPPD above for truth table.	R/W	1
4	RMIXBUFPU	RFRX-path Mixer Buffer Power-up. It controls the power-up state of the RX Mixer Buffer circuit. In power-up state, the RX Mixer Buffer circuit is enabled. When the RXMIXBUFPU field is set to '0', the RX Mixer Buffer circuit is in a power-up state. See RXMIXBUFPD above for truth table.	R/W	1
3		This field is reserved and should be fixed to '1'.	R/W	1
2	RLPFPU	RX Low-pass Filter Power-up. It controls the power-up state of the RX LPF circuit. In power-up state, the RX LPF circuit is enabled. When the RLPFPU field is set to '0', the RX LPF circuit is in the power-up state. See RLPFPD above for truth table.	R/W	1
1	VGAPU	Variable Gain Amplifier Power-up. It controls the power-up state of the VGA circuit. In power-up state, the VGA circuit is enabled. When the VGAPU field is set to '0', the VGA circuit is in a power-up state. See VGAPD for truth table.	R/W	1
0	ADCPU	Analog-to-Digital Converter Power-up. It controls the power-up state of the ADC circuit. In power-up state, the ADC circuit is enabled. When ADCPU field is set to '0', the ADC circuit is in a power-up state. See ADCPD for truth table.	R/W	1

TXRFPD (RF TX PATH POWER-DOWN REGISTER, 0x2206)

This register is used to power down circuits related to transmission in RF block.

<table>
<tr><th>Bit Field</th><th>Name</th><th>Descriptions</th><th>RW</th><th>Reset Value</th></tr>
<tr><td>7:6</td><td></td><td>Reserved</td><td></td><td>11</td></tr>
<tr><td>5</td><td>TXUMBUFPD</td><td>TX Up-mixer Buffer Power-down.
With the TXUMBUFPU field, controls the power-down state of the TX Up-mixer Buffer circuit. In power-down state, the TX Up-mixer Buffer circuit is disabled and draws no current. When TXUMBUFPU field is set to ‘1’ and the TXUMBUFPD field is set to’0’, the TX Up-mixer Buffer circuit is in a power-down state.
The following table shows TX Up-mixer Buffer circuit state based on the values of the TXUMBUFPD and TXUMBUFPU fields.
<table><tr><th>TXUMBUFPD</th><th>TXUMBUFPU</th><th>TX Up-mixer Buffer state</th></tr><tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr><tr><td>1</td><td>0</td><td>Always power-up state.</td></tr><tr><td>0</td><td>1</td><td>Always power-down state.</td></tr><tr><td>0</td><td>0</td><td>Always power-up state.</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>4</td><td></td><td>Reserved</td><td></td><td>1</td></tr>
<tr><td>3</td><td>PAPD</td><td>Power Amplifier Power-down.
With PAPU field, controls the power-down state of the Power Amplifier(PA) circuit. In power-down state, the PA circuit is disabled and draws no current. When the PAPU field is set to ‘1’ and the PAPD field is set to ’0’, the PA circuit is in a power-down state.The following table shows the PA circuit state based on the values of the PAPD and PAPU fields.</td><td>R/W</td><td>0</td></tr>
</table>

<table>
<tr><td></td><td></td><td>
<table>
<tr><th>PAPD</th><th>PAPU</th><th>PA state</th></tr>
<tr><td>1</td><td>1</td><td>Controlled by a modem block</td></tr>
<tr><td>1</td><td>0</td><td>Always power-up state.</td></tr>
<tr><td>0</td><td>1</td><td>Always power-down state.</td></tr>
<tr><td>0</td><td>0</td><td>Always power-up state.</td></tr>
</table>
</td><td></td><td></td></tr>
<tr><td>2:1</td><td>TXUMPD</td><td>TX Up-mixer Power-down.
With the TXUMPU field, controls the power-down state of the TX Up-mixer circuit. In power-down state, the TX Up-mixer circuit is disabled and draws no current. When the TXUMPU field is set to ‘3’ and the TXUMPD field is set to’0’, TX Up-mixer circuit is in power-down state. The following table shows TX Up-mixer circuit state based on the values of the TXUMPD and TXUMPU fields. The values of ‘1’ and ‘2’ are not used in these fields.
<table>
<tr><th>TXUMPD</th><th>TXUMPU</th><th>TX Up-mixer state</th></tr>
<tr><td>3</td><td>3</td><td>Controlled by a modem block</td></tr>
<tr><td>3</td><td>0</td><td>Always power-up state.</td></tr>
<tr><td>0</td><td>3</td><td>Always power-down state.</td></tr>
<tr><td>0</td><td>0</td><td>Always power-up state.</td></tr>
<tr><td>others</td><td>others</td><td>Reserved</td></tr>
</table>
</td><td>R/W</td><td>00</td></tr>
<tr><td>0</td><td>DACPD</td><td>Digital-to-Analog Converter Power-down.
With the DACPU field, controls the power-down state of the Digital-to-Analog converter(DAC) circuit. In power-down state, the DAC circuit is disabled and draws no current. When the DACPU field is set to ‘1’ and the DACPD field is set to’0’, the DAC circuit is in a power-down state. The following table shows DAC circuit state based on the values of the DACPD and DACPU fields.
<table>
<tr><th>DACPD</th><th>DACPU</th><th>DAC state</th></tr>
<tr><td>1</td><td>1</td><td>Controlled by a modem</td></tr>
</table>
</td><td>R/W</td><td>0</td></tr>
</table>

				block		
		1	0	Always power-up state.		
		0	1	Always power-down state.		
		0	0	Always power-up state.		

TXRFPU (RF TX PATH POWER-UP REGISTER, 0x2207)

This register is used to power up the circuits related to transmission in RF block.

Bit Field	Name	Descriptions	R/W	Reset Value
7:6		Reserved		11
5	TXUMBUFPU	TX Up-mixer Buffer Power-up. It controls the power-up state of the TX Up-mixer Buffer circuit. In a power-up state, TX Up-mixer Buffer circuit is enabled. When TXUMBUFPU field is set to '0', the TX Up-mixer Buffer circuit is in a power-up state. See TXUMBUFPD above for truth table.	R/W	1
4		Reserved		1
3	PAPU	Power Amplifier Power-up. It controls the power-up state of the PA circuit. In power-up state, the PA circuit is enabled. When the PAPU field is set to '0', the PA circuit is in a power-up state.	R/W	1
2:1	TXUMPU	TX Up-mixer Power-up. It controls the power-up state of the TX Up-mixer circuit. In power-up state, the TX Up-mixer circuit is enabled. When the TXUMPU field is set to '0', the TX Up-mixer circuit is in a power-up state. See TXUMPD above for truth table.	R/W	1
0	DACPU	Digital-to-Analog Converter Power-up. It controls the power-up of the TX Up-mixer circuit. In power-up state, the TX Up-mixer circuit is enabled. When the TXUMPU field is set to '0', the TX Up-mixer circuit is in a power-up state. See DACPD for truth table.	R/W	1

RXFRM1 (RX FRAME FORMAT1 REGISTER, 0x2211)

This register is used to set the frame format of RX Packet.

Bit Field	Name	Descriptions	R/W	Reset Value
7:6	RXRATE	Receptable RX Packet Rate. It sets the receptable RX data rate. MG245X supports 250kbps compatible with IEEE802.15.4 standard and 500kbps or 1Mbps extended data rate provided by RadioPulse Inc. 0: Supports only 250kbps data rate (compatible with IEEE802.15.4 standard) 1: Support 250kbps and 500kbps data rates 2 or 3: 250kbps and 1Mbps data rates	R/W	00
5:4	TXRATE	Transmission Rate. It sets the transmisson data rate. MG245X supports 250kbps compatible with IEEE802.15.4 standard and 500kbps or 1Mbps extended data rate provided by RadioPulse Inc. 0: Supports only 250kbps data rate (compatible with IEEE802.15.4 standard) 1: Support 250kbps and 500kbps data rates 2.3: 250kbps and 1Mbps data rates	R/W	00
3:0	RXPRMLNG	RX Preamble Length. It sets preamble length of the received packet. MG245X supports a preamble of 8 symbol length defined in the IEEE 802.15.4 standard. At the same time, MG245X provides a configurable preamble length. When ‘n’ value is set in RXPRMLNG field, the length of preamble is set to (n+6)symbol. The length of preamble can be varied from 6 symbol to 21 symbol. The value of this field should be set as same as it of TXPRMLNG field.It is recommended to use default value of ‘2’.	R/W	0010

SYNCWD (SYNCWORD REGISTER, 0x2212)

It sets a byte data to be used as the SFD(Start-of-Frame Delimiter). IEEE802.15.4 standard uses 2 symbols as an SFD. The 2 symbols are ‘0xA7’. The ‘7’ is the first of the 2 symbols transmitted .

TDCNF3 (OPERATION DELAY CONTROL 3 REGISTER, 0x2213)

This register sets the delay to power down RF after TX.

Bit Field	Name	Descriptions	R/W	Reset Value
7:4	TXPDTM	This field sets the delay time between a packet transmission and RF TX-path power-down. The delay time is set in 16μs unit. The minimum and maximum value are 0μs and 240μs respectively.	R/W	0100
3:0		Reserved	R/W	1111

TDCNF0 (OPERATION DELAY CONTROL 0 REGISTER, 0x2217)

This register sets delay for switching between TX and RX.

Bit Field	Name	Descriptions	R/W	Reset Value
7:4	TXRXTM	This field sets the delay time of the transition from TX to RX state. The delay time is set in16 μs increments. The minimum and maximum values are 0μs and 240μs respectively.	R/W	0110
3:0	RXTXTM	This field sets the delay time of the transition from RX to TX. The delay time is set in16μs increments. The minimum and maximum values are 0μs and 240μs respectively.	R/W	0011

TXFRM1 (TX FRAME FORMAT1 REGISTER, 0x2215)

This register is used to set the frame format of TX packet.

Bit Field	Name	Descriptions	R/W	Reset Value
7:4		Reserved		1111
3:0	TXPRMLNG	TX Packet Preamble Length. It sets the preamble length of the transmission packet. The MG245X supports a preamble of 8 symbol length defined in the IEEE 802.15.4 std. At the same time, the MG2450 provides a configurable preamble length. When 'N' value is set in TXPRMLNG field, the length of preamble is set to (N+6)symbol. The length of preamble can be varied from 6 symbol to 21 symbol. Note: The value of this field should be set as same as it of RXPRMLNG field. It is recommended to use a default value of '2'.	R/W	0010

AGCCNF3 (AGC CONFIGURATION3 REGISTER, 0x2223)

This register sets AGC operation environment.

<table>
<tr><th>Bit Field</th><th>Name</th><th>Descriptions</th><th>R/W</th><th>Reset Value</th></tr>
<tr><td>7:5</td><td></td><td>Reserved</td><td></td><td>111</td></tr>
<tr><td>4:3</td><td>RXEAWS</td><td>RX Energy Accumulator Window size.
AGC calculates the average of the received signal energy for a defined time when measuring RSSI. RXEAWS field is used to set the defined time.
<table>
<tr><th>RXEAWS</th><th>Average Calculation Duration</th></tr>
<tr><td>0</td><td>16μs</td></tr>
<tr><td>1</td><td>32μs</td></tr>
<tr><td>2</td><td>64μs</td></tr>
<tr><td>3</td><td>128μs</td></tr>
</table></td><td>R/W</td><td></td></tr>
<tr><td>2:0</td><td></td><td>Reserved</td><td></td><td>111</td></tr>
</table>

CCA0 (CCA CONTROL CONFIGURATION0 REGISTER, 0x2248)

This register is used to set CCA operation environment.

<table>
<tr><th>Bit Field</th><th>Name</th><th>Descriptions</th><th>R/W</th><th>Reset Value</th></tr>
<tr><td>7</td><td></td><td>Reserved</td><td></td><td>1</td></tr>
<tr><td>6:4</td><td>CCAAWS</td><td>When CCA uses energy detection method, it sets the averaging duration for the received signal energy.
<table>
<tr><th>CCAAWS</th><th>Average Calculation Duration</th></tr>
<tr><td>0</td><td>1μs</td></tr>
<tr><td>1</td><td>2μs</td></tr>
<tr><td>2</td><td>4μs</td></tr>
<tr><td>3</td><td>8μs</td></tr>
<tr><td>others</td><td>16μs</td></tr>
</table></td><td>R/W</td><td>100</td></tr>
<tr><td>3</td><td>CCAFIX</td><td>CCA Indication Lock-up.
It fixes the communication channel state to idle. A communication channel state is determined by the CCA circuit in MG245X. When a channel state is busy, a packet is not transmitted. This field allows packet transmission regardless of the channel state. When this field is set to ‘1’, the channel is always in idle state.</td><td>R/W</td><td>0</td></tr>
</table>

<table>
<tr><td>2</td><td></td><td>Reserved</td><td></td><td>1</td></tr>
<tr><td>1:0</td><td>CCAMD</td><td>CCA Indication Mode
This field sets the method to determine the communication channel state. The following describes the three methods to detect the channel state.

ED (Energy Detection): This method determines the channel state as ‘busy’ when the energy of received signal is higher than the defined level.

CD (Carrier Detection): This method determines the channel state as ‘busy’ when an IEEE802.15.4 carrier is detected.

FD (Frame Detection): This method determines the channel state as ‘busy’ when the normal IEEE802.15.4 packet is detected.

<table><tr><td>CCAMD</td><td>Method</td></tr><tr><td>0</td><td>ED</td></tr><tr><td>1</td><td>CD</td></tr><tr><td>2</td><td>FD</td></tr><tr><td>3</td><td>reserved</td></tr></table></td><td>R/W</td><td>00</td></tr>
</table>

CCA1 (CCA CONTROL CONFIGURATION1 REGISTER, 0x2249)

R/W. CCA Decision Threshold.

This register defines threshold of energy level to determine whether a channel state as busy. This register is used only when CCA methods based on energy detection are used. The CCATHRS is stored as 2’s complement integer in dBm. The default value of CCATHRS register is 0xB2 and corresponds to ‘-78dBm’.

CCA2 (CCA CONTROL CONFIGURATION2 REGISTER)

R/W. Energy Calculation Offset(ENRGOFST)

The MG245X calculates the energy level of the received signal based on the gain of RF block per the following equation.

Energy Level(dBm) = CCA2 – RF_GAIN

As the equation described above, the CCA2 register compensates for an offset of calculated energy level for the received signal. A user can set the difference between the energy level calculated on a developed system and the real energy level of the received signal in the CCA2

register.

CCA3 (CCA CONTROL CONFIGURATION3 REGISTER, 0x224B)

The small change in energy level may cause some uncertainty in determining the channel state when that state is defined using only the threshold of the CCA1 register.

To prevent that uncertainty, the MG245X can define a hysteresis value to define a minimum drop in energy level to initiate a change in the channel state from busy to the idle state. The CCA3 register is used to set that hysteresis.

Bit Field	Name	Descriptions	RW	Reset Value
7:4				1111
3:0	CCAHYST	CCA Hysteresis Level Once the channel is determined to be in a busy state, it can be changed to an idle state only when the calculated energy level is decreased more than the level defined in CCAHYST field. The CCAHYST field is stored as a 2's complement integer and the unit is dB.	R/W	0100

TST0 (TEST CONFIGURATION0 REGISTER, 0x2260)

This register is used to control the test of a modem and RF block.

Bit Field	Name	Descriptions	RW	Reset Value
7	TSTEN	Test Enable This register is used to change MG245X to a test mode. When TSTEN field is set to '0', the modem block controls the RF block according to the test mode which is set by STAMD and TSTMD fields. The TSTEN field should be set after setting the registers that are required to set up a test mode. In order to set a new test mode, TSTEN field should be set to '1' before setting a new test mode. After that, TESTEN field should be set to '0'.	R/W	1
6:5	STAMD	Station Mode. This field sets MG245X to a transmitter during a test mode. 1: Set as a transmitter 2: Set as a receiver 3: Set as a transceiver	R/W	00

4:0	TSTMD	Test Mode. This field sets a test mode. Refer to the [Table 11] for the various modes based on the setting of the STAMD and TSTMD fields.	R/W	00000

Table 11. Test Mode Setting

Mode	STAMD [1:0]	TSTMD [4]	TSTMD [3:2]	TSTMD [1]	TSTMD [0]	Operation
Single-tone Generation for RF Test	01	0	00	0	0	I=cos, Q=sin single-tone generation
	01	0	01	0	0	I=8'h80, Q=sin single-tone generation
	01	0	10	0	0	I=cos, Q=8'h80 signel-tone generation
	01	0	11	0	0	I=8'h80, Q=8'h80
	01	1	00	0	0	I=cos, Q=cos single-tone generation
	01	1	01	0	0	I=8'h80, Q=cos single-tone generation
	01	1	10	0	0	I=cos, Q=8'h80 signel-tone generation
	01	1	11	0	0	I=8'h80, Q=8'h80
				0	0	No-operation
Modulated Carrier Generation for RF Test	01	X	XX	1	0	Continous 802.15.4 Modulated Signal
	others			1	0	No-operation

TST1 (TEST CONFIGURATION1 REGISTER,0x2261)

This register defines the fixed symbol to be modulated for generating a test packet. TST1 register sets two fixed symbols.

Bit Field	Name	Descriptions	RW	Reset Value
7:4	TSTSYML	Test Symbol, Low Nibble. This field sets the symbol to be transmitted first in fixed symbols.	R/W	0110
3:0	TSTSYMH	Test Symbol, High Nibble. This field sets the symbol to be transmitted later in fixed symbols.	R/W	1100

TST2 (TEST CONFIGURATION2 REGISTER, 0x2262)

This register sets the inter-packet time interval when the test mode transmits the modulated packet of a random data. The inter-packet time interval is needed for setting-up EVM measurement.

Bit Field	Name	Descriptions	RW	Reset Value
7:3	IFS	Inter-frame Space. Sets the number of the symbols corresponding to the inter-packet time interval in the IFS field. The duration of 1 symbol is 16μs. Therefore, if IFS is set to 'N', inter-packet time interval is set to (16*N) μs. The defined value of IFS field is valid only when the TSTMD field is set to '23'.	R/W	11111
2:0		Reserved		111

TST3 (TEST CONFIGURATION3 REGISTER, 0x2263) R/W.

This register is used to support the generation of a random symbol for the modulation in a test mode. The RNG generates the random number by CRC-16. TST3 register stores the seed for RNG circuit. Any number except '0' can be used as the seed for RNG circuit.

TST13 (TEST CONFIGURATION13 REGISTER, 0x226D) R/W.

This register sets the length of transmitting packet in a test mode. The length of packet can be set from 1 byte to 127 byte and the duration of each packet is 256μs or 4,256μs.

TST14 (TEST CONFIGURATION14 REGISTER, 0x226E) R/W.

This register sets the frequency of single-tone in a test mode for transmitting single-tone.

TST14 register can set from a 1/4 frequency of DAC operating clock to a 1/256 frequency of DAC operating clock. This single-tone signal can be used to test RF block characteristics. Cosine and sine signal can be selectively assigned to I-phase or Q-phase of RF block.

The frequency of single-tone is defined by following equation.

$$\text{Frequency} = \frac{f_{DAC} \cdot CFRQ}{1024} Hz$$

PHYSTS0 (PHY STATUS0 REGISTER, 0x2270)

This registers are used to monitor or control the state of the modulation block or demodulation

blocks in the modem block.

<table>
<tr><th>Bit Field</th><th>Name</th><th>Descriptions</th><th>R/W</th><th>Reset Value</th></tr>
<tr><td>7</td><td>RXSTSF</td><td>RX Status Lock-up.
This field fixes the state of the demodulation block to a defined state. With a desired state in the RXSTS field, setting ‘0’ in the RXSTSF field, caused the state of the demodulation block to be fixed and retained until RXSTSF is set to ‘1’.</td><td>R/W</td><td>1</td></tr>
<tr><td>6:4</td><td>RXSTS</td><td>RX Block Status.
This field shows the state of the demodulation block in a modem block. RXSTS field can read the current state of the demodulation block. This field stores the state to be changed.
However, the state of the demodulation block is not changed as a new state is only recorded to this field. In order to be changed to the recorded state, RXSTSF field should be set to ‘0’.
The state in RXSTS field can be different from the recorded state because RXSTS shows the current state of demodulation block which is updated from the recorded state.
The following table shows the state in RXSTS.
<table>
<tr><td>RXSTS=’000’</td><td>RX_IDLE
In RX_IDLE state, the demodulation block cannot receive a packet.</td></tr>
<tr><td>RXSTS=’001’</td><td>RX_PKTD
In RX_PKTD state, the demodulation block waits a reception of a packet (RX ready state).</td></tr>
<tr><td>RXSTS=’010’</td><td>RX_WAIT
In RX_WAIT state, the demodulation block waits the completion of the timing synchronization following the packet detection.</td></tr>
<tr><td>RXSTS=’011’</td><td>RX_CFE1, coarse carrier frequency offset
In RX_CFE1 state, the demodulation block is in the first stage of coarse carrier frequency offset estimation (CFE). During the first stage, the demodulation block waits for the received signal which is adequate for CFE.</td></tr>
<tr><td>RXSTS=’100’</td><td>RX_CFE2
In RX_CFE2 state, the demodulation block is in the second stage of CFE. During the second stage, the demodulation block estimates the coarse</td></tr>
</table></td><td>R/W</td><td>000</td></tr>
</table>

<table>
<tr><td></td><td></td><td>
<table>
<tr><td></td><td>offset of the carrier frequency.</td></tr>
<tr><td>RXSTS=’101’</td><td>RX_SYMD1
In RX_SYMD1 state, the demodulation block is in the first stage of symbol detection(SYMD)
During the first stage, the demodulation block waits for the received signal which is adequate for SYMD.</td></tr>
<tr><td>RXSTS=’110’</td><td>RX_SYMD2
In RX_SYMD2 state, the demodulation block is in the second stage of the SYMD. During the second stage, the demodulation block detects symbol from the received signal.</td></tr>
<tr><td>RXSTS=’111’</td><td>RX_PKTEND
In RX_PKTEND state, the demodulation block ends the successful packet reception.</td></tr>
</table>
</td><td></td><td></td></tr>
<tr><td>3:0</td><td>TXSTS</td><td>TX Block Status.
This field shows the state of the modulation block in the modem block. TXSTS field can read the current state of the modulation block. This field stores the state to be changed. However, the state of the modulation block is not changed as a new state is only recorded to this field. In order to be changed to the recorded state, TXSTSF field should be set to ‘0’. The state in TXSTS field can be different from the recorded state because TXSTS shows the current state of modulation block. The following table shows the state in TXSTS.
<table>
<tr><td>TXSTS=’0000’</td><td>TX_IDLE
In TX_IDLE state, the modulation block cannot transmit a packet.</td></tr>
<tr><td>TXSTS=’0001’</td><td>TX_WAIT1
In TX_WAIT1 state, the modulation block is waiting for the TX FIFO to be ready before packet transmission.</td></tr>
<tr><td>TXSTS=’0010’</td><td>TX_WAIT2
In TX_WAIT2 state, the modulation block is waiting for the TX FIFO to be ready before the packet transmission.</td></tr>
<tr><td>TXSTS=’0011’</td><td>TX_CHK
In TX_WAIT1 state, the modulation</td></tr>
</table>
</td><td>R/W</td><td>0000</td></tr>
</table>

	block checks the validity of the transmission packet length.
TXSTS=’0100’	TX_PRM In TX_PRM state, the modulation block transmits the SFD.
TXSTS=’0101’	In TX_SFD state, the modulation block transmits the SFD.
TXSTS=’0110’ TXSTS=’0111’	TX_TAIL In TX_LNG state, the modulation block transmits the length.
TXSTS=’1000’	TX_BDY In TX_BDY state, the modulation block transmits the frame body of transmission packet.
TXSTS=’1001’	TX_TAIL In TX_TAIL state, the modulation block transmits the tail data of frame body.
TXSTS=’1010’	TX_CONT In TX_CONT, the modulation block transmits the modulated signal for a test mode.
TXSTS=’111’	Reserved

PHYSTS1 (PHY STATUS1 REGISTER, 0x2271)

This register is used to monitor or control the state of a modem block.

Bit Field	Name	Descriptions	R/W	Reset Value
7	TXSTSF	TX Status Lock-up. This field fixes the state of the modem block to the defined state. When recording the desired state to TXSTS field and setting ‘0’ to TXSTSF field, the state of the demodulation block is fixed to the recorded state. The state of the modem block is retained until TXSTSF is set to ‘1’.	R/W	1
6:5		Reserved	R/W	11

4	MDSTSF	Modem Status Lock-up. This field fixes the state of the modem block to a defined state. When recording the desired state to MDSTS field and setting '0' to MDSTSF field, the state of the demodulation block is fixed to the recorded state. The state of the modem block is retained until MDSTSF is set to '1'.	R/W	1
3:0	MDSTS	Modem State. This field shows the state of the modem block. MDSTS field can read the current state of the modem block. When a new state is recorded in this field, it is stored. The state of the modem block is not changed when only recording a state in MDSTS field. In order to be changed to the recorded state, MDSTSU or MDSTSF field should be set to '0'. The state in MDSTS field can be different from the recorded state because MDSTS shows the current state of the modem block. [Table 12] shows the state in MDSTS.	R/W	0000

Table 12. MDSTS Field

MDSTS='0000'	MD_IDLE In MD_IDLE state, the modem block is in idle state. The modem block cannot transmit or receive a packet. The modem block consumes the minimum current. The transmission or reception of a packet is available only when the modem block is in a modem ready state.
MDSTS='0001'	MD_DCCAL In MD_DCCAL state, it does the calibration of DC cancellation block. After calibration, PLL is powered-up PLL automatically.
MDSTS='0010'	MD_WAITON In MD_WAITON state, the modem block is in midterm to a modem ready state and waits the stabilization of the supply power to PCC circuit.
MDSTS='0011'	MD_WAITLCK In MD_WAITLCK state, PLL is waiting to be locked.
MDSTS='0100'	MD_RDY In MD_RDY state, the modem block is in already state. The supply power to PLL circuit is stabilized and the PLL is locked.
MDSTS='0101'	MD_TXCAL In MD_TXCAL state, the modem block is waiting for the transmitter of the RF block to be stabilized before the packet transmission. After the stabilization, the state of the modem block is changed to MD_TXPKT state.
MDSTS='0110'	MD_TXPKT In MD_TXPKT state, the modem block transmits a packet.
MDSTS='0111'	MD_RXCAL In MD_RXCAL state, the modem block is waiting for the receiver of the RF block to be stabilized before the packet reception. After the stabilization, the state of the modem block is changed to MD_RXON state.
MDSTS='1000'	MD_RXON In MD_RXON state, the modem block is waiting for the reception of a packet. During this state, the modem block continuously monitors the reception of a

	packet.
MDSTS='1001'	MD_RXPKT In MD_RXPKT state, the modem block performs the demodulation of the received packet. After the completion of the packet reception, the state of the modem block is changed to MD_RXON state.
MDSTS='1010'	Reserved
MDSTS='1011'	MD_RFTST In MD_RFTST state, the modem block works in a selected test mode.
MDSTS='1100'	MD_IFS In MD_IFS state, the modem block is ready for transmitting the next packet after the completion of a packet transmission in a test mode.
MDSTS='1101'	MD_CLR In MD_CLR state, the modem block ends the packet transmission and sets TXREQ field to '1' automatically. The state of the modem block is changed to MD_RXON state when TXREQ field is set to '1'.
MDSTS='1110' MDSTS='1111'	Reserved

AGCSTS0 (AGC STATUS0 REGISTER, 0x2272)

This register is used to monitor and control the gain of LNA or RX Mixer in RF block.

Bit Field	Name	Descriptions	R/W	Reset Value
7	MGF	Mixer Gain Lock-up. This field sets the gain of RX Mixer to a fixed value recorded in MG field. When the MGF field is set to '0', the RX Mixer gain is set to the value recorded in MG field. Only when the MGF field is set to '1', can the RX Mixer gain be adjusted by the AGC block.	R/W	1
6	LGF	LNA Gain Lock-up. This field sets the gain of LNA to a fixed value recorded in the LG field. When the LGF field is set to '0', LNA gain is set to the value recorded in the LG field. Only when LGF field is set to '1', can the LNA gain be adjusted by the AGC block.	R/W	1
5	MG	RX Mixer Gain. This field is used to monitor the RX Mixer gain set by AGC block. The RX Mixer gain with MG='1' is 25 dB higher than with MG='0'. When the value of the MGF field is '0', the MG field sets the gain of RX Mixer.	R/W	1
4	LG	LNA Gain. This field is used to monitor the LNA gain set by AGC block. The LNA gain with LG='1' is 25 dB higher than with LG='0'. When the value of the	R/W	1

		LGF field is ‘0’, the LG field sets the gain of LNA.		
3:0		Reserved		1111

AGCSTS1 (AGC STATUS1 REGISTER, 0x2273)

This registers is used to monitor and control the gain of VGA in RF block.

Bit Field	Name	Descriptions	R/W	Reset Value
7	VGF	VGA Gain Lock-up. This field sets the gain of VGA as the fixed value recorded in VG field. When the VGF field is set to ‘0’, VGA gain is changed according to the value recorded in VG field. Only when VGF field is set as ‘1’, VGA gain can be adjusted by AGC block.	R/W	1
6:1	VG	VGA Gain. This field is used to monitor the VGA gain set by the AGC block. The VGA consists of three stages and the gain of the VGA can be set from 0 to 63dB with 1 dB steps. When the value of VGF field is ‘0’, the VG field sets the gain of VGA. VG[1:0] — Stage 1 gain(0 ~ 3dB) ‘00’ : 0dB ‘01’ : 1dB ‘10’ : 2dB ‘11’ : 3dB VG[3:2] — Stage 2 amplifier gain(0 ~ 12dB) ‘00’ : 0dB ‘01’ : 4dB ‘10’ : 8dB ‘11’ : 12dB VG[5:4] — Stage 3 amplifier gain(0 ~ 32dB) ‘00’ : 0dB ‘01’ : 16dB ‘10’ : 32dB ‘11’ : reserved	R/W	101111
0		reserved		1

AGCSTS2 (AGC STATUS2 REGISTER, 0x2274) R/W.

This register stores the average energy level of the received RF signal at antenna. The stored energy level is the average of the received signal energy which is measured for the time interval defined in RXEAWS field. The indicated value at AGCSTS2 register is stored as a 2’s complement integer in dBm.

AGCSTS3 (AGC STATUS3 REGISTER, 0x2275) R/W.

This register stores the average energy level of the received packet. AGCSTS2 register indicates the average of received signal's energy level for a defined time interval. AGCSTS3 register shows the energy level of the last received packet. The value in AGCSTS3 register is retained until another packet is received.

INTCON (PHY INTERRUPT CONTROL REGISTER, 0x2277)

This register is used to mask off the interrupt of a modem block.

Bit Field	Name	Descriptions	R/W	Reset Value
7:4		Reserved		111
3	RXENDMSK	RXEND_INT Interrupt Mask. This field masks RXEND_INT off. When RXENDMSK field is set to '0', RXEND_INT interrupt is not generated. This interrupt should be used to support the successful packet reception.	R/W	0
2	RXSTMSK	RXSTART_INT Interrupt Mask. This field masks RXEND_START off. When RXSTMSK field is set to '0', RXSTART_INT interrupt is not generated. RXSTART_INT is not a mandatory interrupt. It is recommended to mask off RXSTART_INT interrupt when the rapid packet reception is needed.	R/W	0
1	TXENDMSK	TXEND_INT Interrupt Mask. This field masks TXEND_INT off. When TXENDMSK field is set to '0', TXEND_INT interrupt is not generated. This interrupt should be used to support the successful packet transmission.	R/W	0
0	MRDYMSK	MDREADY_INT Interrupt Mask. This field masks MDRDY_INT off. When MRDYMSK field is set to '0', MDRDY_INT interrupt is not generated. This interrupt should be used to check whether a modem block is ready for transmission /reception or not.	R/W	0

INTIDX (PHY INTERRUPT STATUS AND INDEX REGISTER, 0x2278)

This register is used to indicate the kinds of the interrupt when it occurs

Bit Field	Name	Descriptions	R/W	Reset Value

<table>
<tr><td>7:5</td><td></td><td>Reserved</td><td></td><td>111</td></tr>
<tr><td>4</td><td>FRMDX</td><td>Reception of Extended Transfer Rate Packet.
This field indicates the data rate of the received packet when an RXEND_INT interrupt occurs.
When FRMDX field is set to ‘0’ and RXRATE field in RXFRM1 register is set to ‘1’, it indicates the packet reception of 500kbps data rate. When RXRATE field is set to ‘2’, it indicates the packet reception data rate of 1Mbps.</td><td>R/W</td><td>1</td></tr>
<tr><td>3</td><td>ALLINTCLR</td><td>All Interrupt Clear.
This field disables all interrupts when they occur. This field clears all interrupts occurred.
When multiple interrupts occur at the same time, the modem block stores them in a buffer and processes them in order. When INTIDX field is read, the executed interrupts are cleared in order. When ALLINTCLR field is set to ‘0’, all the interrupts in buffer are cleared at the same time.</td><td>R/W</td><td>1</td></tr>
<tr><td>2</td><td></td><td>Reserved</td><td></td><td>1</td></tr>
<tr><td>1:0</td><td>INTIDX</td><td>Interrupt Table Index.
This register shows the kind of the interrupt when an interrupt occurs, in order if multiple interrupts occur simultaneously. The INTSTS field in the INTSTS register should be used for looking through a list of all interrupts that have been triggered. After reading INTIDX field, executed interrupts are cleared automatically.
<table>
<tr><th>INTIDX</th><th>Interrupt</th></tr>
<tr><td>0</td><td>MDREADY_INT interrupt</td></tr>
<tr><td>1</td><td>TXEND_INT interrupt</td></tr>
<tr><td>2</td><td>RXSTART_INT interrupt</td></tr>
<tr><td>3</td><td>RXEND_INT interrupt</td></tr>
</table>
</td><td>R/W</td><td>00</td></tr>
</table>

INTSTS (PHY INTERRUPT STATUS REGISTER, 0x227E)

This register is used to indicate the kinds of the interrupt when the multiple interrupts occur.

Bit	Name	Descriptions	R/W	Reset Value
7:5		Reserved		111
4	FRMDX	Reception of Extended Transfer Rate Packet. This field is equal to FRMDX field in INTIDX register.	R/W	1
3:0	INTSTS	Multiple Interrupt Status.	R/W	1111

		This register shows the interrupt status when multiple interrupts occur currently. Each bit in INTSTS field represents the status of a specific interrupt. A table of Bit vs. Interrupt is shown below. INTSTS[0] : MDREADY_INT interrupt INTSTS[1] : TXEND_INT interrupt INTSTS[2] : RXSTART_INT interrupt INTSTS[3] : RXEND_INT interrupt When an interrupt is triggered, the INTSTS field corresponding to each interrupt is set to '0'. To clear the executed interrupt, the bit for each of the executed interrupts should be reset to '1' by software. INTSTS[0] : MDREADY_INT interrupt INTSTS[1] : TXEND_INT interrupt INTSTS[2] : RXSTART_INT interrupt INTSTS[3] : RXEND_INT interrupt		

TRSWC0 (TX/RX SWITCH CONTROL0 REGISTER, 0x220D) R/W.

This register is used to set two GPIO pins (P1.6, P1.7) as TX/RX switching control pins.

P1.6 and P1.7 can be used to control TX/RX switching when the TRSWC0 register is set to '0x50'. When TRSWC0 is set to '0x00', two pins are used as GPIO pins. TRSWC1 register should be set the same as TRSWC0 to avoid collision.

TRSWC1 (TX/RX SWITCH CONTROL0 REGISTER, 0x2279) R/W.

This register is used to output TRSW and TRSWB signal at P1.6 and P1.7. TRSW signal remains as a logic '1' during packet transmission and as a logic '0' during packet reception. TRSWB, the complementary signal of TRSW, remains as a logic '0' during packet transmission and as a logic '1' during packet reception. TRSWC1 register should be set to '0x00' to output TRSW and TRSWB signal.

PLL0/1/2/3 (PLL CONTROL 0/1/2/3 REGISTER, 0x2286, 0x2287, 0x2288, 0x228B) R/W.

To modify PLL offset frequency, refer to [Table 13] below. As shown in [Table 13], the delta K correction factor is determined based on the values in the FRAC_K[19:0] registers as follows.

Register Name / Offset frequency	PLL0 Address: 0x2286 FRAC_K[19:12]	PLL1 Address: 0x2287 FRAC_K[11:4]	PLL2[3:0] Address: 0x2288 FRAC_K[3:0]
1MHz	01	40	0
100kHz	00	20	0
10kHz	00	03	3
1kHz	00	00	5
*195.31Hz	00	00	1

Table 13. FRAC_K[19:0] Register

**1LSB = 195.31Hz*

** The values of PLL0, PLL1, PLL2[3:0] in [Table 13] are HEX.*

When using 16MHz crystal, the values of PLL0, PLL1 and PLL2 need to be adjusted in order to define the adjustment to the channel frequency as shown in [Table 10].

New Frequency = Original Frequency + Frequency Offset. Here, delta K, which is the Freqneucy Offset, can be derived from the following formula.

delta K= Frequency Offset / 195.31Hz

The New Frequency can be obtained by converting the delta K calculated above to Hex format and adding it to the value of the registers for the current frequency.
In order to adjust the frequency of channel 26, set PLL3(0x228B) to 0x32 and then adjust it.

PLL4(PLL CONTROL 4 REGISTER, 0x2289)

This register is used to process an automatic frequency calibration(AFC) when changing the locking frequency of the PLL.

Bit	Name	Descriptions	R/W	Reset Value
7	AFCSTART	Automatic Frequency Calibration Start.	R/W	0

		This field is used to request the start of AFC. AFC is processed when the AFCSTART is set to '1'. After the AFC process, AFCSTART field is automatically cleared to '0'.		
6	AFCEN	Automatic Frequency Calibration Enable. This field is used to enable the AFC process and should be set to '1' to run AFC.	R/W	0
5:0		Reserved		111111

PLL5 (PLL CONTROL 5 REGISTER, 0x228A)

This register is used to check whether PLL is locked or not.

Bit	Name	Descriptions	R/W	Reset Value
7		Reserved	R/W	0
6	PLLOCK	This field shows the locking status of PLL circuit. When this field is set to '1', the PLL circuit is locked. When '0', the PLL circuit is not locked.	R/W	0
5:0		Reserved		111111

To change the channel setting, the PLL0, PLL1, PLL2, PLL3, PLL4 registers need to be changed by the following procedure;

1) Change the RF RX-path to power-down state by setting the RXRFPD register to 00000000.
2) Change the RF TX-path to power-down state by setting the TXRFPD register to 11010000.
3) Set the value of the PLL0, PLL1, PLL2, PLL3 registers.
4) Start the AFC by setting 11101111 to PLL4 register.
5) Retain Stand-by state until setting PLLLOCK in PLL5 register to '1'.
6) Change the RF TX-path from the power-down state to the normal state by setting the TXRFPD register to 11111111 after setting the PLLLOCK to '1'.
7) Change the RF RX-path from the power-down state to the normal state by setting RXRFPD register to 11111111.

TXPA0/1/2 (POWER AMPLIFIER OUTPUT CONTROL REGISTER, 0x22A0/1/2) R/W.

This register determines the power out of the device. For the linear output level, TXPA0, TXPA1 and TXPA2 should be adjusted per the following table.

TX Output Power Level(dBm)	TXPA0(0xA0)	TXPA1(0xA1)	TXPA2(0xA2)

8	10011111	11111111	01101111
7	10011111	11110101	01101111
6	10011101	11110000	01101111
5	10011111	11101101	01101111
4	10010101	11101101	01101111
3	00011111	11110011	01101111
2	00011111	11101100	01101111
1	00011110	11101010	01101111
0	00011100	11101001	01101111
-5	00011110	11100011	01101111
-7	00011000	11100011	01101111
-10	00011000	11100010	01101111
-15	00010011	11100010	01101111
-20	00010010	11100010	01101110

7.9. IN-SYSTEM PROGRAMMING(ISP)

In-system programming(ISP) function enables a user to download an application program to the internal flash memory. When Power-on, the MG245X checks the value of MS[2:0] pin. When the value of the MS[2] pin is '1' and the value of the MS[1:0] is '0', ISP mode is selected. The following procedure is to use ISP function.

1. In MS[2:0] pin, MS[2] should be set to'1'. MS[1] and MS[0] should be set to '0'.
2. Make RS-232 connection with PC by using Serial port1.
   The configuration is 8-bit, no parity, 1 stop bit and 115200 baud rate.
3. Power up a device.
4. Execute ISP program.(included in Development Kit)
5. Load an application program in Intel HEX format.
6. Download.

When the procedure above is finished, an application program is stored in the internal flash memory. To execute the application program, a device should be reset after setting MS[2:0] pin to '0'.

After reset, the application program in the internal flash memory is executed by the internal MCU.

7.10. MG245X INSTRUCTION SET SUMMARY

Table 14. Instruction Set Summary

MNEMONIC	DESCRIPTION	BYTE	CYCLE
ARITHMETIC OPERATIONS			
ADD A,Rn	Add register to Accumulator	1	1
ADD A,direct	Add direct byte to Accumulator	2	1
ADD A,@Ri	Add indirect RAM to Accumulator	1	1
ADD A,#data	Add immediate data to Accumulator	2	1
ADDC A,Rn	Add register to Accumulator with Carry	1	1
ADDC A,direct	Add direct byte to Accumulator with Carry	2	1
ADDC A,@Ri	Add indirect RAM to Accumulator with Carry	1	1
ADDC A,#data	Add immediate data to Accumulator with Carry	2	1
SUBB A,Rn	Subtract register to Accumulator with borrow	1	1
SUBB A,direct	Subtract direct byte to Accumulator with borrow	2	1
SUBB A,@Ri	Subtract indirect RAM to Accumulator with borrow	1	1
SUBB A,#data	Subtract immediate data to Accumulator with borrow	2	1
INC A	Increment Accumulator	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	2
INC @Ri	Increment direct RAM	1	1
DEC A	Decrement Accumulator	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	2
DEC @Ri	Decrement direct RAM	1	1
INC DPTR	Increment Data Pointer	1	3
MUL AB	Multiply A & B	1	3
DIV AB	Divide A by B	1	10
DA A	Decimal Adjust Accumulator	1	1
LOGICAL OPERATIONS			
ANL A,Rn	AND register to Accumulator	1	1
ANL A,direct	AND direct byte to Accumulator	2	2
ANL A,@Ri	AND indirect RAM to Accumulator	1	1
ANL A,#data	AND immediate data to Accumulator	2	1
ANL direct,A	AND Accumulator to direct byte	2	2
ANL direct,#data	AND immediate data to direct byte	3	2
ORL A,Rn	OR register to Accumulator	1	1
ORL A,direct	OR direct byte to Accumulator	2	2
ORL A,@Ri	OR indirect RAM to Accumulator	1	1
ORL A,#data	OR immediate data to Accumulator	2	1
ORL direct,A	OR Accumulator to direct byte	2	2
ORL direct,#data	OR immediate data to direct byte	3	2
XRL A,Rn	Exclusive-OR register to Accumulator	1	1
XRL A,direct	Exclusive-OR direct byte to Accumulator	2	2
XRL A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL A,#data	Exclusive-OR immediate data to Accumulator	2	1
XRL direct,A	Exclusive-OR Accumulator to direct byte	2	2
XRL direct,#data	Exclusive-OR immediate data to direct byte	3	2
CLR A	Clear Accumulator	1	1

CPL A	Complement Accumulator	1	1
RL A	Rotate Accumulator Left	1	1
RLC A	Rotate Accumulator Left through the Carry	1	1
RR A	Rotate Accumulator Right	1	1
RRC A	Rotate Accumulator Right through the Carry	1	1
SWAP A	Swap nibbles within the Accumulator	1	1
DATA TRANSFER			
MOV A,Rn	Move register to Accumulator	1	1
MOV A,direct	Move direct byte to Accumulator	2	1
MOV A,@Ri	Move indirect RAM to Accumulator	1	1
MOV A,#data	Move immediate data to Accumulator	2	3
MOV Rn,A	Move Accumulator to register	1	3
MOV Rn,direct	Move direct byte to register	2	2
MOV Rn,#data	Move immediate data to register	2	2
MOV direct,A	Move Accumulator to direct byte	2	2
MOV direct,Rn	Move register to direct byte	2	2
MOV direct,direct	Move direct byte to direct	3	3
MOV direct,@Ri	Move indirect RAM to direct byte	2	2
MOV direct,#data	Move immediate data to direct byte	3	2
MOV @Ri,A	Move Accumulator to indirect RAM	1	2
MOV @RI,direct	Move direct byte to indirect RAM	2	3
MOV @Ri,#data	Move immediate data to indirect RAM	2	2
MOV DPTR,#data16	Load Data Pointer with a 16-bit constant	3	3
MOVC A,@A+DPTR	Move Code byte relative to DPTR to Accumulator	1	2
MOVC A,@A+PC	Move Code byte relative to PC to Accumulator	1	1
MOVX A,@Ri	Move External RAM(8-bit addr) to Accumulator	1	1
MOVX A,@DPTR	Move External RAM(16-bit addr) to Accumulator	1	1
MOVX @Ri,A	Move Accumulator to External RAM(8-bit addr)	1	2
MOVX @DPTR,A	Move Accumulator to External RAM(16-bit addr)	1	1
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A,Rn	Exchange register with Accumulator	1	2
XCH A,direct	Exchange direct byte with Accumulator	2	2
XCH A,@Ri	Exchange indirect RAM with Accumulator	1	2
XCHD A,@Ri	Exchange low-order Digit indirect RAM with Accumulator	1	2
BOOLEAN VARIABLE MANUPULATION			
CLR C	Clear Carry	1	1
CLR bit	Clear direct bit	2	1
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	1
CPL C	Complement Carry	1	1
CPL bit	Complement direct bit	2	1
ANL C,bit	AND direct bit to Carry	2	2
ANL C,/bit	AND complement of direct bit	2	2
ORL C,bit	OR direct bit to Carry	2	1
ORL C,/bit	OR complement of direct bit to Carry	2	1
MOV C,bit	Move direct bit to Carry	2	1
MOV bit,C	Move Carry to direct bit	2	1
JC rel	Jump if Carry is set	2	2
JNC rel	Jump if Carry is not set	2	2

JB bit.rel	Jump if direct Bit is set	3	2
JNB bit,rel	Jump if direct Bit is Not set	3	3
JBC bit,rel	Jump if direct Bit is set & clear bit	3	3
PROGRAM BRANCHING			
ACALL addr11	Absolute Subroutine Call	2	3
LCALL addr16	Long Subroutine Call	3	3
RET	Return from Subroutine	1	3
RETI	Return from interrupt	1	3
AJMP addr11	Absolute Jump	2	3
LJMP addr16	Long Jump	3	3
SJMP rel	Short Jump (relative addr)	2	2
JMP @A+DPTR	Jump indirect relative to the DPTR	1	2
JZ rel	Jump if Accumulator is Zero	2	2
JNZ rel	Jump if Accumulator is Not Zero	2	2
CJNE A,direct,rel	Compare direct byte to Accumulator and Jump if Not Equal	3	3
CJNE A,#data,rel	Compare immediate to Accumulator and Jump if Not Equal	3	3
CJNE Rn,#data,rel	Compare immediate to register and Jump if Not Equal	3	3
CJNE @Ri,#data,rel	Compare immediate to indirect and Jump if Not Equal	3	3
DJNZ Rn,rel	Decrement register and Jump if Not Zero	2	2
DJNZ direct,rel	Decrement direct byte and Jump if Not Zero	3	2
NOP	No Operation	1	1

8. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}	Chip Core Supply Voltage	-0.3 to 1.65	V
V_{DDIO}	I/O Supply Voltage	-0.3 to 3.3	V
RF_{IN}	Input RF Level	10	dBm
T_{STG}	Storage Temperature	-40 to 85	°C

Exceeding one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “ELECTRICAL SPECIFICATIONS” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE1: All voltage values are based on V_{SS} and V_{SSIO}.
NOTE2: These values were obtained under worst-case test conditions specially prepared for the MG245X and these conditions are not sustained in normal operation environment.

CAUTION: *ESD(Electrostatic Discharge) sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

9. DC CHARACTERISTICS

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DD}	Core Supply voltage (DVDD, AVDD_VCO,AVDD_RF1, AVDD_DAC,AVDD_XOSC,AVDD ,AVDD_CP)	1.35	1.5	1.65	V
V_{DDIO}	I/O Supply voltage(DVDD3V)	1.35	3.0	3.3	V
AGND	Chip Ground		0		V
V_{IH}	High level input voltage	$0.7\times V_{DDIO}$		V_{DDIO}	V
V_{IL}	Low level input voltage	0		$0.3\times V_{DDIO}$	V
V_{OH}	High level output voltage	V_{DDIO}-0.5		V_{DDIO}	V
V_{OL}	Low level output voltage	0		0.4	V
T_A	Air temperature	-40		85	°C

V_{DD} = 1.5 V, V_{DDIO} = 3.0 V, T_A (air temperature) = 25°C if nothing else stated.

NOTE 1: All voltage values are based on AGND. All input and output voltage levels are TTL-compatible. XOSCI can be driven by CMOS clock.

NOTE 2: I/O Supply Voltage(DVDD3) is recommended to use less than twice of Core Supply Voltage.

NOTE 3: Driving electricity (I_{OH}) (V_{OH} is V_{DDIO}-0.5V)

V_{DDIO} [V]	I_{OH} [mA]	Comment
3.0	5.36	@ V_{DD}=1.5V
2.5	4.44	
2.0	3.31	
1.8	2.80	
1.5	1.96	
1.35	1.51	@ V_{DD}=1.35V

NOTE 4: Driving electricity(I_{OL}) (V_{OL} is 0.4V)

V_{DDIO} [V]	I_{OL} [mA]	Comment
3.0	4.38	@ V_{DD}=1.5V
2.5	3.72	
2.0	2.79	
1.8	2.32	
1.5	1.50	
1.35	1.04	@ V_{DD}=1.35V

10. ELECTRICAL SPECIFICATIONS

Temp = 25˚C, VDD=3.0V, Core Voltage[1]=1.5V, MCU Clock:8MHz[2]

Parameter	MIN	TYP	MAX	UNIT
Current Consumption				
Active MCU without RX/TX Operation (AES, Peripheral, SADC Disabled)		3.35		mA
Active MCU with TX Mode (AES, Peripheral, SADC Disabled)				mA
@+8dBm Output Power		42.1		
@+7dBm Output Power		40.2		
@+6dBm Output Power		38.5		
@+5dBm Output Power		38.4		
@+4dBm Output Power		34.8		
@+3dBm Output Power		33.2		
@+2dBm Output Power		31.8		
@+1dBm Output Power		30.9		
@+0dBm Output Power		29.7		
Active MCU with RX Mode (AES, Peripheral, SADC Disabled)		32.2		mA
PM1		25	110	μA
PM2		1.7		μA
PM3		0.3[3]		μA
AES		2.1		mA
Peripheral		2.2		mA
Sensor ADC		1		mA
RF Characteristic				
RF Frequency Range	2.400		2.4835	GHz
Transmit Data Rate (Normal Mode[4])		250		kbps

[1] AVDD_VCO, AVDD_RF1, AVDD_CP, AVDD_DAC, AVDD, DVDD_XOSC, DVDD
[2] Refer to **Section 7.3** in this document for register setting of MCU clock.
[3] Based on the Teradyne J750 MP(Mass Production) test equipment
[4] ZigBee Standard

Transmit Data Rate (Turbo Mode)		500		kbps
Transmit Data Rate (Premium Mode)		1000		kbps
Transmit Chip Rate		2000		kChips/s
Maximum Output Power			8	dBm
Programmable Output Power Range		30		dB
Receiver Sensitivity Normal Mode Turbo Mode Premium Mode		 -98 -95 -91		dBm
Adjacent Channel Rejection +5MHz -5MHz		 49 48.8		dB
Alternate Channel Rejection +10MHz -10MHz		 56.1 56.8		dB
Others Channel Rejection ≥+15MHz ≥-15MHz		 52.7 58.3		dB
Co-channel Rejection		-10.7		dB
Blocking/Desensitization +/- 5 MHz +/- 10 MHz +/- 15 MHz +/- 20 MHz +/- 30 MHz +/- 50 MHz		 -45 -42 -48 -40 -43 -46		dBm
Spurious Emission (30Hz~1GHz)		-50		dBm
Spurious Emission (1GHz~2.5GHz)		-40		dBm
Spurious Emission (2.5~12.7GHz)		-50		dBm
2nd Harmonics		-50		dBm
3rd Harmonics		-70		dBm
Frequency Error Tolerance			±200	kHz
Error Vector Magnitude (EVM)		9.8		%
Saturation(Maximum Input Level)		5		dBm

RSSI Dynamic Range		90		dB
RSSI Accuracy		±1.2	+6/-3	dB
RSSI Linearity		±0.2	±6	dB
RSSI Average Time		128		μsec
Frequency Synthesizer				
Phase Noise @ ±100kHz offset @ ±1MHz offset @ ±2MHz offset @ ±3MHz offset @ ±5MHz offset		 -80.3 -108.8 -113.3 -120.4 -124.2		dBc/Hz
PLL Lock Time		110		μsec
PLL Jitter		16		psec
Crystal Oscillator Frequency		16		MHz
Crystal Frequency Accuracy Requirement	-10		+10	ppm
On-chip RC Oscillator				
Frequency		32.78		KHz
Sensor ADC				
Number of Bits		8		bits
Conversion Time		256		μsec
Differential Nonlinearity(DNL)		±1.7		LSB
Integral Nonlinearity(INL)		±2.4		LSB
SINAD(Sine Input)		51.0		dB
On-chip Voltage Regulator				
Supply range for Regulator	1.9	3.0	3.6	V
Regulated Output		1.5		V
Maximum Current			140[5]	mA
No Load Current		15		μA
Start-up Time		260[6]		μsec

[5] Voltage Regulator Input Voltage=3V, 80mV voltage drop
[6] 10μF and 100pF load capacitor

Temp = 25˚C, VDD=3.0V, Core Voltage[7]=1.5V, MCU Clock:16MHz[8]

Parameter	MIN	TYP	MAX	UNIT
Current Consumption				
Active MCU without RX/TX Operation (AES, Peripheral, SADC Disabled)		4.6		mA
Active MCU with TX Mode (AES, Peripheral, SADC Disabled) @+8dBm Output Power @+7dBm Output Power @+6dBm Output Power @+5dBm Output Power @+4dBm Output Power @+3dBm Output Power @+2dBm Output Power @+1dBm Output Power @+0dBm Output Power		 45.1 43.2 41.5 41.4 37.8 36.2 34.8 33.9 32.7		mA
Active MCU with RX Mode (AES, Peripheral, SADC Disabled)		35.2		mA
PM1		25	110	μA
PM2		1.7		μA
PM3		0.3[9]		μA
AES		3.1		mA
Peripheral		2.6		mA
Sensor ADC		1		mA
RF Characteristic				
RF Frequency Range	2.400		2.4835	GHz
Transmit Data Rate (Normal Mode[10])		250		kbps
Transmit Data Rate (Turbo Mode)		500		kbps
Transmit Data Rate (Premium Mode)		1000		kbps

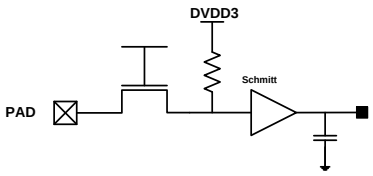
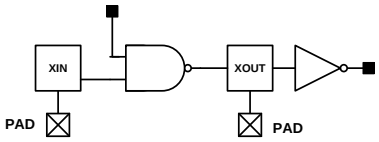
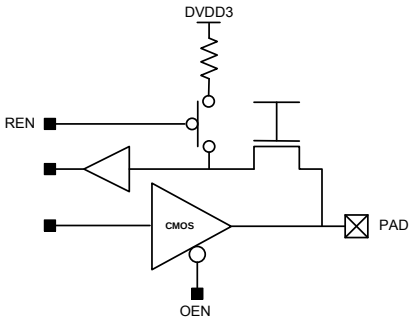
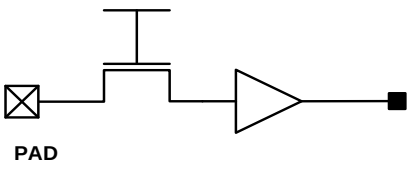
[7] AVDD_VCO, AVDD_RF1, AVDD_CP, AVDD_DAC, AVDD, DVDD_XOSC, DVDD
[8] Refer to **Section 7.3** in this document for register setting of MCU clock.
[9] Based on the Teradyne J750 MP(Mass Production) test equipment
[10] ZigBee Standard

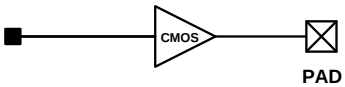
Transmit Chip Rate		2000		kChips/s
Maximum Output Power			8	dBm
Programmable Output Power Range		30		dB
Receiver Sensitivity Normal Mode Turbo Mode Premium Mode		 -98 -95 -91		dBm
Adjacent Channel Rejection +5MHz -5MHz		 49 48.8		dB
Alternate Channel Rejection +10MHz -10MHz		 56.1 56.8		dB
Others Channel Rejection ≥+15MHz ≥-15MHz		 52.7 58.3		dB
Co-channel Rejection		-10.7		dB
Blocking/Desensitization +/- 5 MHz +/- 10 MHz +/- 15 MHz +/- 20 MHz +/- 30 MHz +/- 50 MHz		 -45 -42 -48 -40 -43 -46		dBm
Spurious Emission (30Hz~1GHz)		-50		dBm
Spurious Emission (1GHz~2.5GHz)		-40		dBm
Spurious Emission (2.5~12.7GHz)		-50		dBm
2nd Harmonics		-50		dBm
3rd Harmonics		-70		dBm
Frequency Error Tolerance			±200	kHz
Error Vector Magnitude (EVM)		9.8		%
Saturation(Maximum Input Level)		5		dBm
RSSI Dynamic Range		90		dB
RSSI Accuracy		±1.2	+6/-3	dB

RSSI Linearity		±0.2	±6	dB
RSSI Average Time		128		μsec
Frequency Synthesizer				
Phase Noise @ ±100kHz offset @ ±1MHz offset @ ±2MHz offset @ ±3MHz offset @ ±5MHz offset		 -80.3 -108.8 -113.3 -120.4 -124.2		dBc/Hz
PLL Lock Time		110		μsec
PLL Jitter		16		psec
Crystal Oscillator Frequency		16		MHz
Crystal Frequency Accuracy Requirement	-10		+10	ppm
On-chip RC Oscillator				
Frequency		32.78		KHz
Sensor ADC				
Number of Bits		8		bits
Conversion Time		256		μsec
Differential Nonlinearity(DNL)		±1.7		LSB
Integral Nonlinearity(INL)		±2.4		LSB
SINAD(Sine Input)		51.0		dB
On-chip Voltage Regulator				
Supply range for Regulator	1.9	3.0	3.6	V
Regulated Output		1.5		V
Maximum Current			140[11]	mA
No Load Current		15		μA
Start-up Time		260[12]		μsec

[11] Voltage Regulator Input Voltage=3V, 80mV voltage drop
[12] 10μF and 100pF load capacitor

11. DIGITAL I/O

EQUIVALENT SCHEMATIC	POWER(uW/MHz)	MAX DRIVE (mA)
RESET#		
	4.67	N.A
XOSCI/XOSCO, RTCI/RTCO		
	53.86	N.A
GPIO (P0, P1, P3)		
	82.08	4
MS2,MS1, MS0,MSV		
	3.53	N.A.
TSRW, CSROM#		

	55.67	4

12. AC CHARACTERISTIC

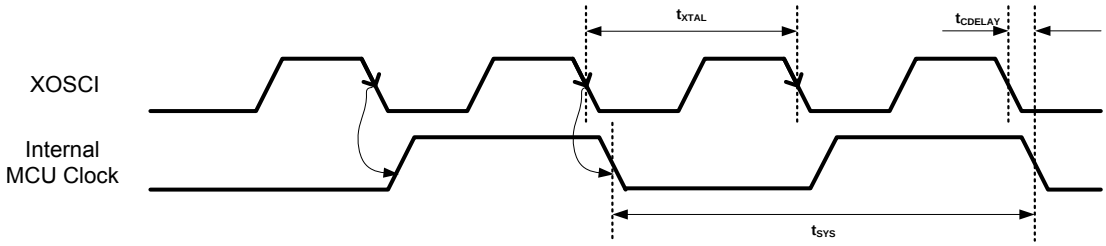


Figure 31. Internal MCU Clock Timing

Parameter	MIN	TYP	MAX	UNIT
Internal MCU Clock Timing				
t_{XTAL}(Crystal Oscillator Duration)		62.5		ns
t_{SYS} (Internal MCU Clock Duration)		125		ns
t_{CDELAY} (Internal MCU Clock Delay)			0.5	ns

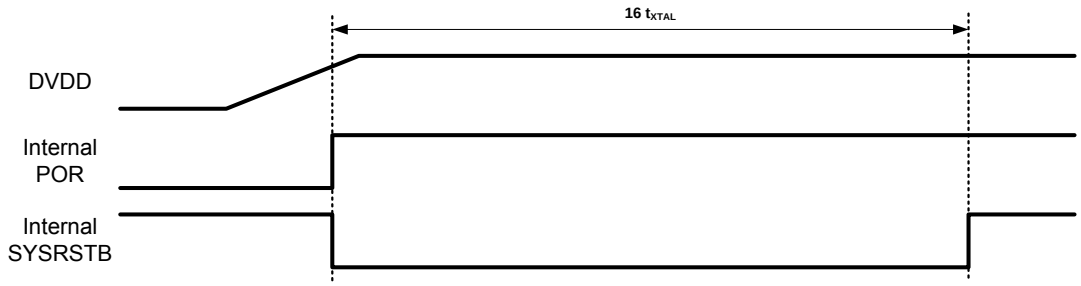


Figure 32. POR Timing

Parameter	MIN	TYP	MAX	UNIT
POR Timing				
16 t_{XTAL}		16 x 62.5		ns

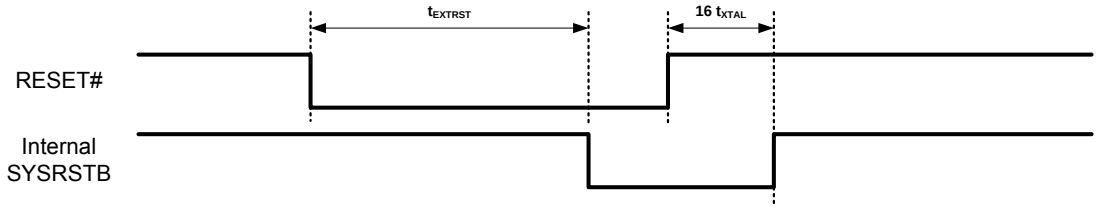


Figure 33. RESET# Timing

Parameter	MIN	TYP	MAX	UNIT
RESET# Timing				
t_{EXTRST} (RESET# Interval)	1			ms
16 t_{XTAL}		16 x 62.5		ns

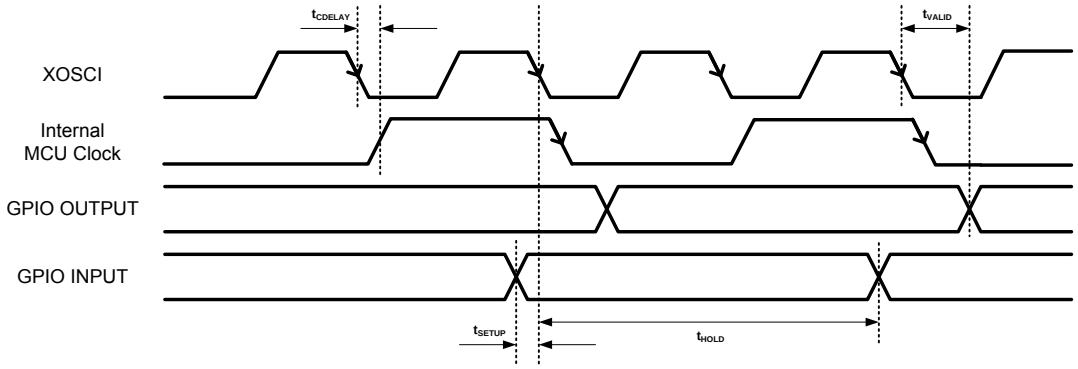


Figure 34. GPIO Timing

Parameter	MIN	TYP	MAX	UNIT
GPIO Timing				
t_{SETUP}	1			ns
t_{HOLD}	1			ns
t_{VALID}			10	ns

13. PACKAGE INFORMATION

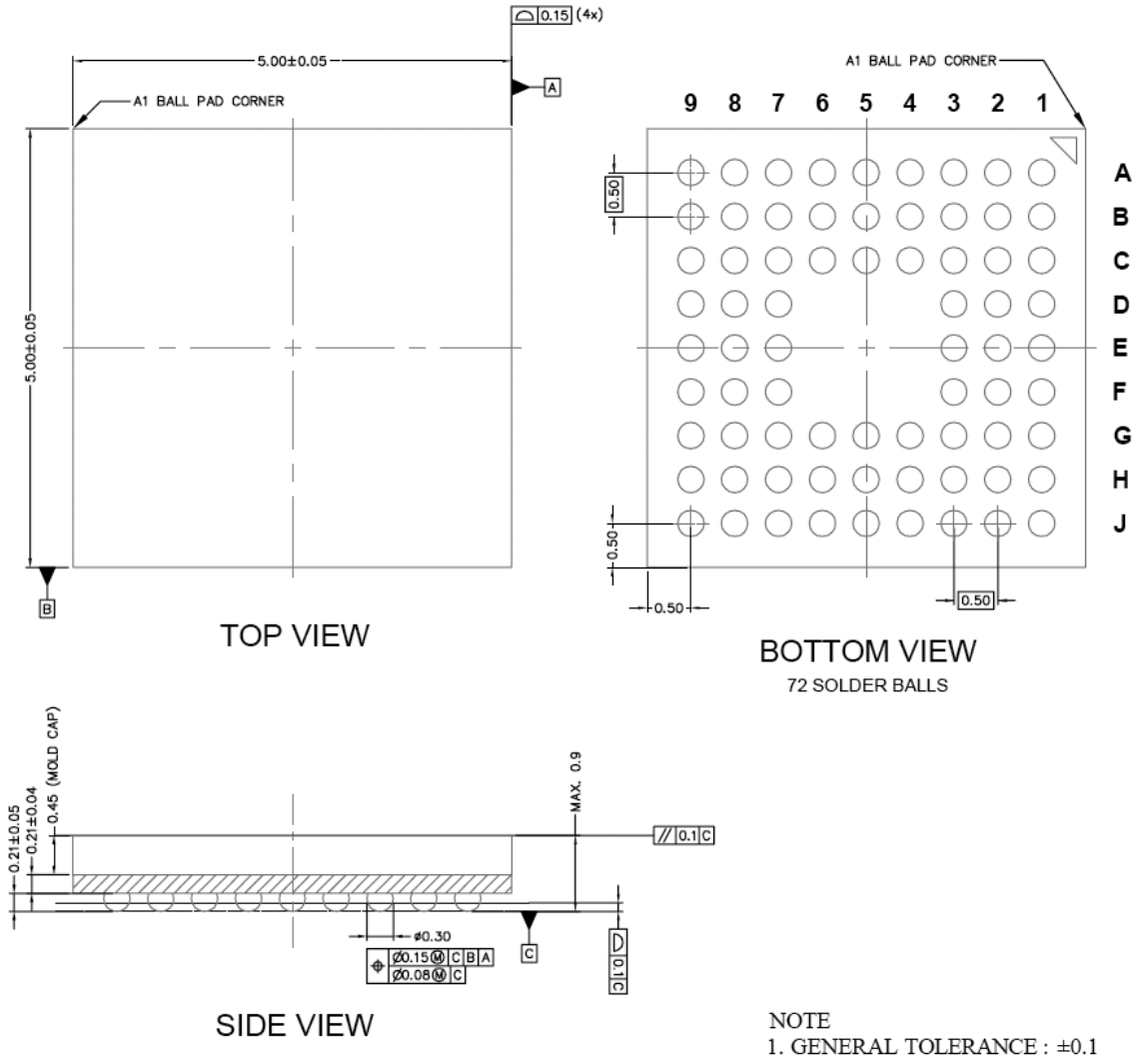
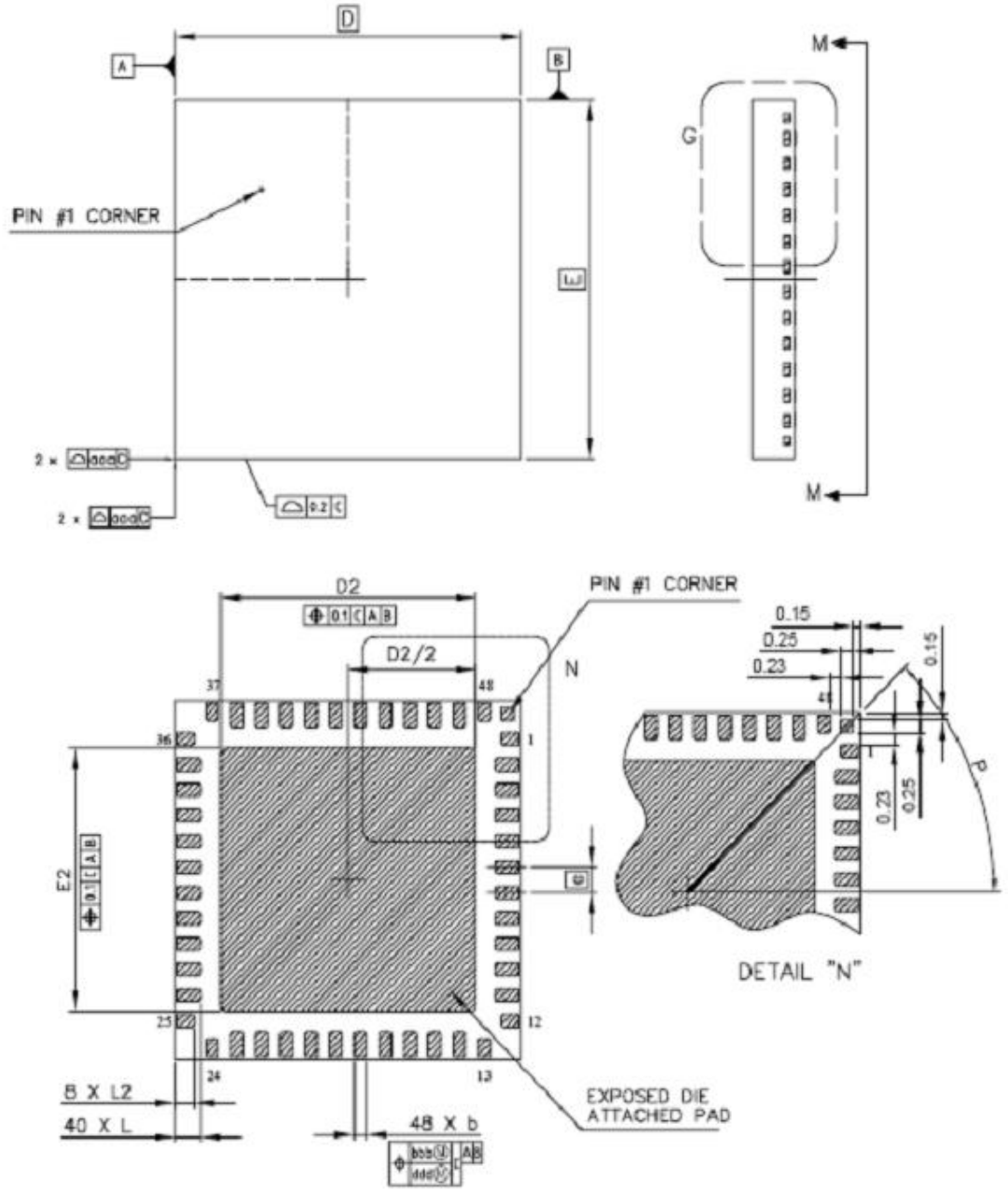
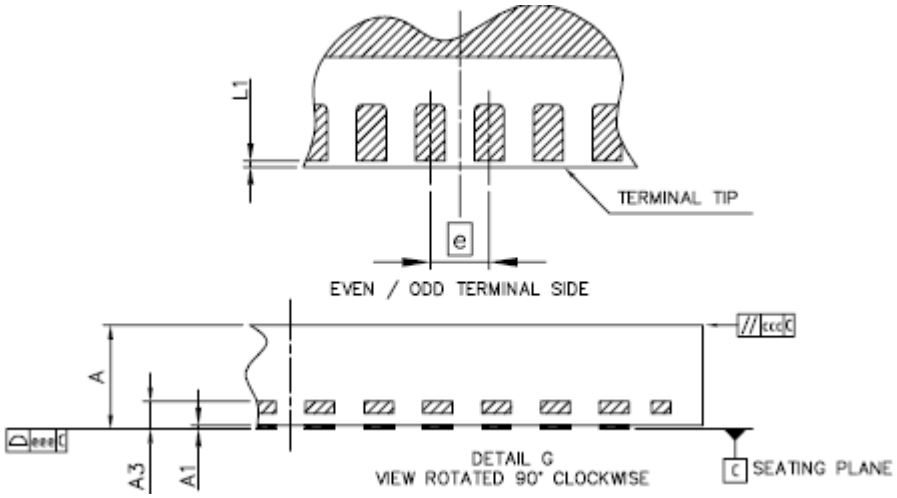


Figure 35.Package Drawing of MG2450


D
A
B
PIN #1 CORNER
G
M
M
2 x aaa C
2 x aaa C
0.2 C
D2
0.1 C A B
D2/2
PIN #1 CORNER
N
37
48
1
36
12
25
24
13
E2
0.1 C A B
e
B X L2
40 X L
48 X b
bbb M C A B
ddd M C
EXPOSED DIE
ATTACHED PAD
0.15
0.25
0.23
0.15
0.23
0.25
R
DETAIL "N"



DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00		0.05
A3		0.203 REF	
b	0.18	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
D2	5.04	5.14	5.24
E2	5.04	5.14	5.24
e		0.50 BSC	
L	0.48	0.53	0.58
L1	0.00		0.10
L2	0.35	0.40	0.45
P		45° BSC	
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

Figure 36. Package Drawing of MG2455

13.1. TRAY SPECIFICATION

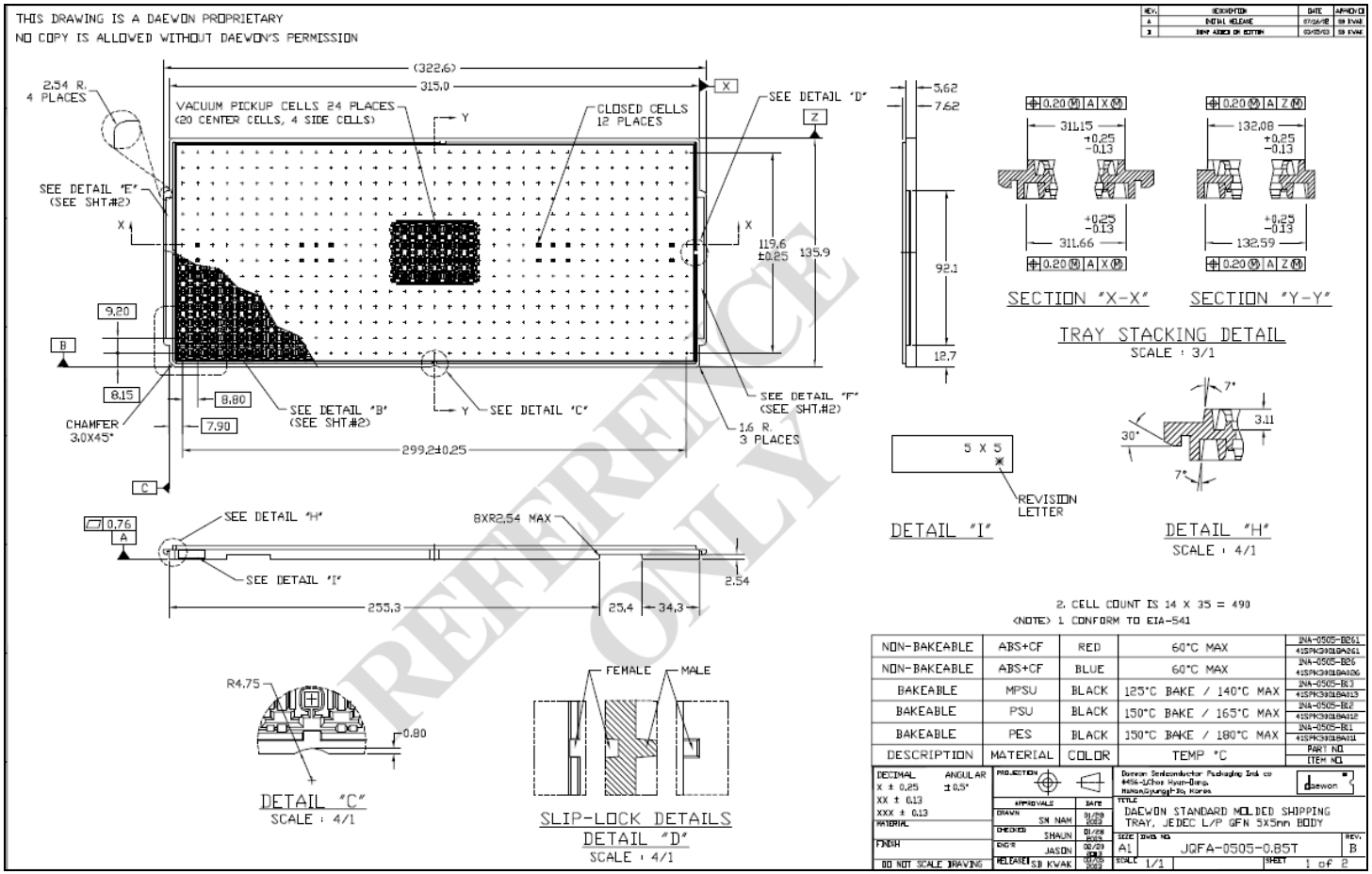
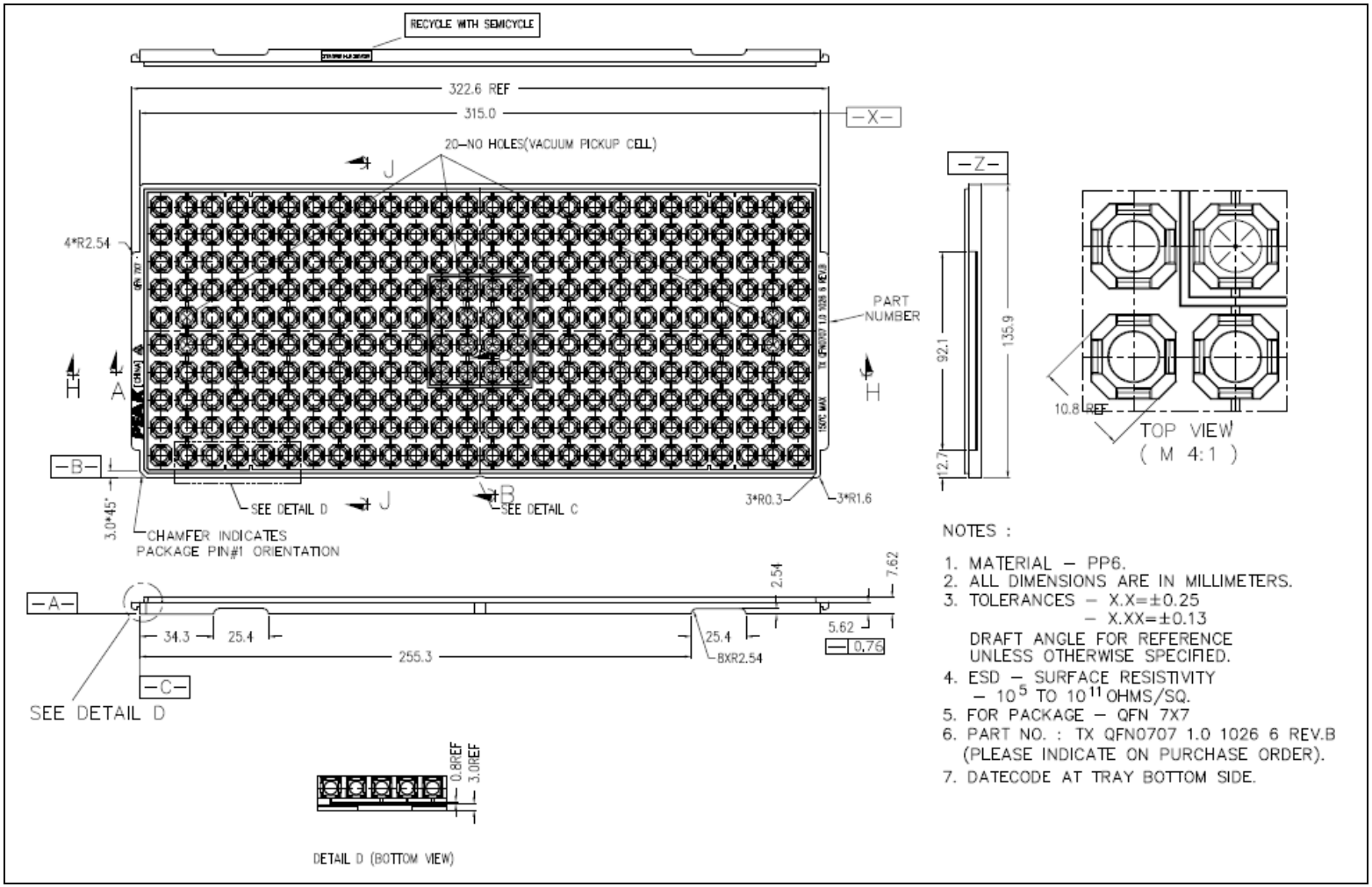


Figure 37. Tray of MG2450


RECYCLE WITH SEMICYCLE
322.6 REF
315.0
-X-
20-NO HOLES(VACUUM PICKUP CELL)
4*R2.54
PART NUMBER
-Z-
92.1
135.9
12.7
10.8 REF
TOP VIEW
(M 4:1)
-B-
3.0*45°
CHAMFER INDICATES
PACKAGE PIN#1 ORIENTATION
SEE DETAIL D
SEE DETAIL C
3*R0.3
3*R1.6
-A-
34.3
25.4
255.3
2.54
7.62
5.62
0.76
8XR2.54
-C-
SEE DETAIL D
0.8REF
3.0REF
DETAIL D (BOTTOM VIEW)
NOTES :
1. MATERIAL - PP6.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. TOLERANCES - X.X=±0.25
- X.XX=±0.13
DRAFT ANGLE FOR REFERENCE
UNLESS OTHERWISE SPECIFIED.
4. ESD - SURFACE RESISTIVITY
- 10^5 TO 10^{11} OHMS/SQ.
5. FOR PACKAGE - QFN 7X7
6. PART NO. : TX QFN0707 1.0 1026 6 REV.B
(PLEASE INDICATE ON PURCHASE ORDER).
7. DATECODE AT TRAY BOTTOM SIDE.

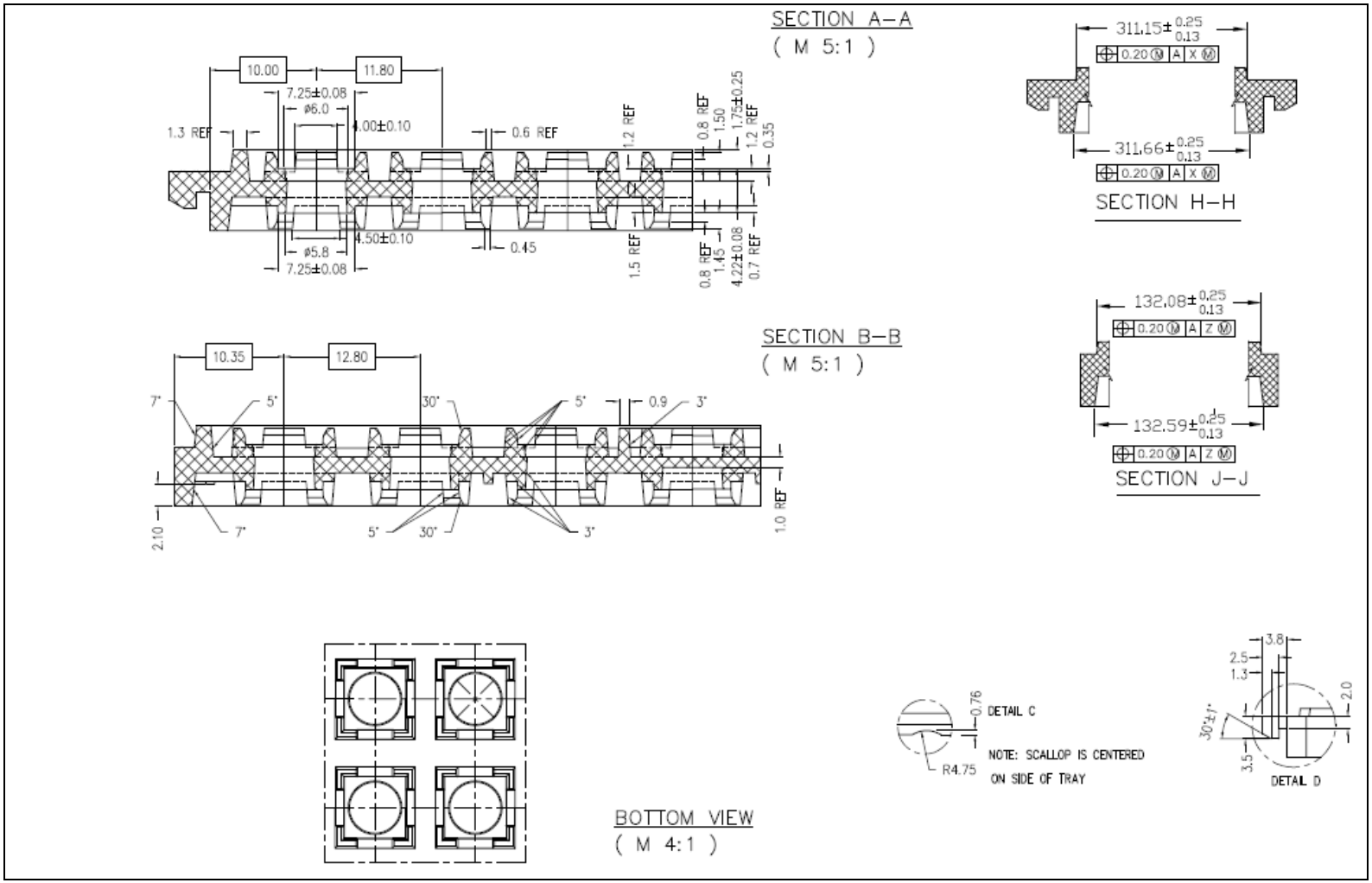
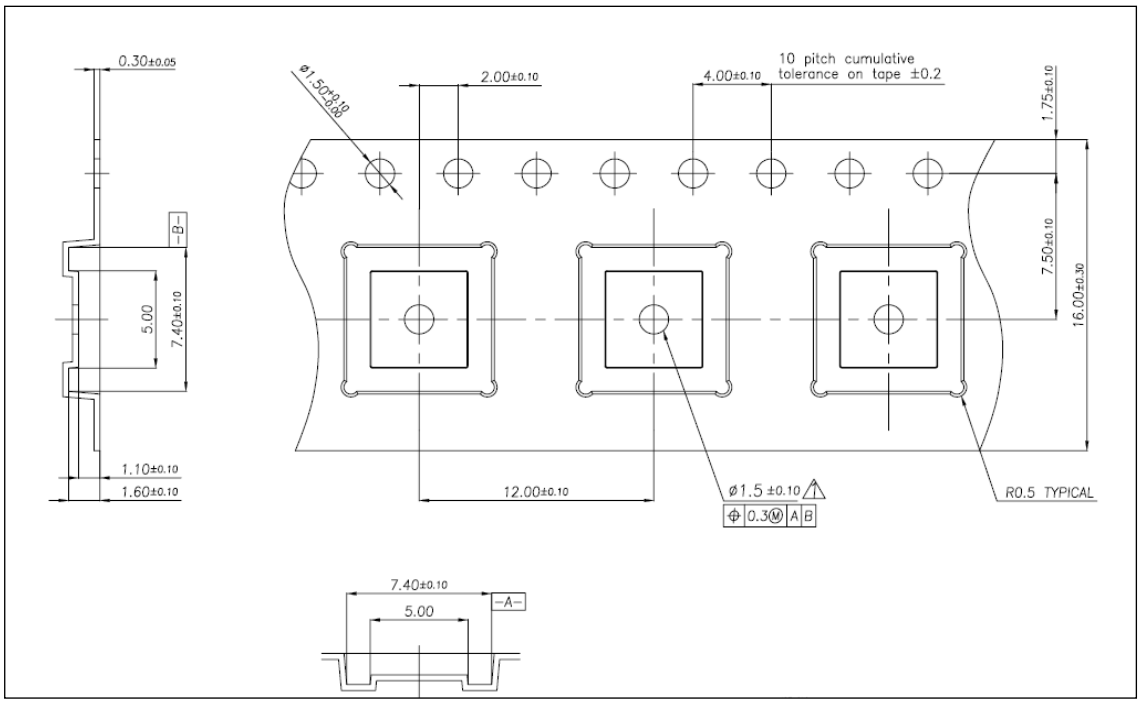
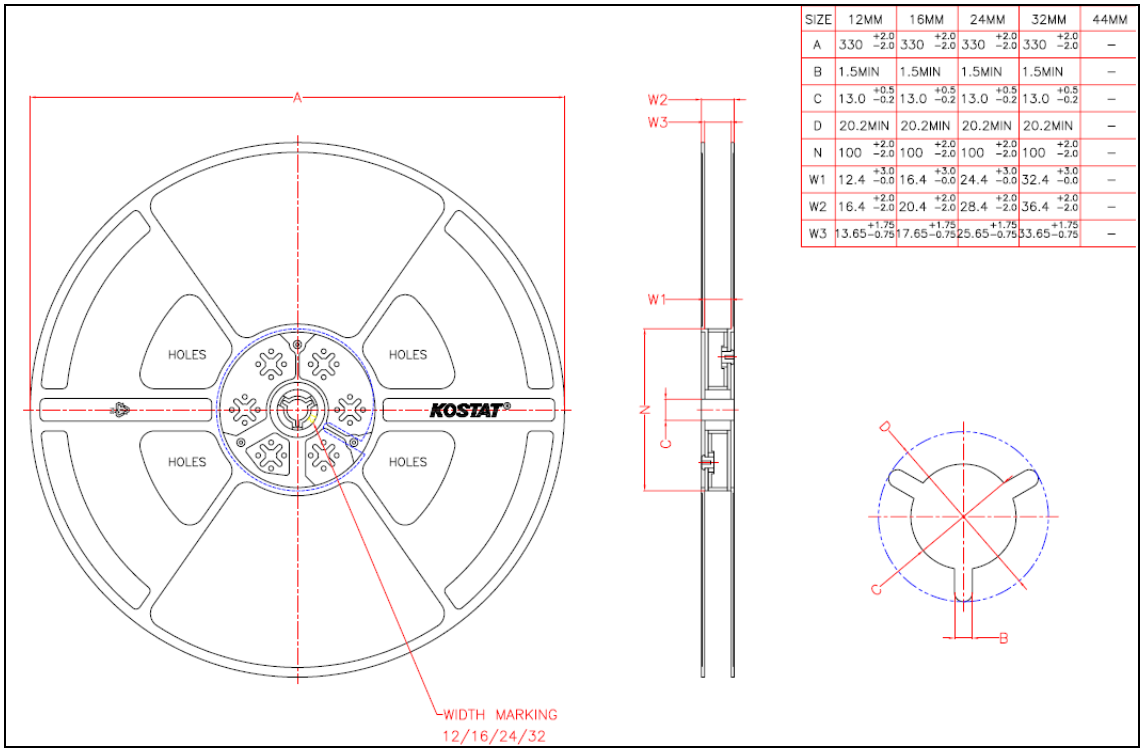


Figure 38. Tray of MG2455

13.2. CARRIER TAPE AND REEL SPECIFICATION





SIZE	12MM	16MM	24MM	32MM	44MM
A	330 +2.0 −2.0	330 +2.0 −2.0	330 +2.0 −2.0	330 +2.0 −2.0	–
B	1.5MIN	1.5MIN	1.5MIN	1.5MIN	–
C	13.0 +0.5 −0.2	13.0 +0.5 −0.2	13.0 +0.5 −0.2	13.0 +0.5 −0.2	–
D	20.2MIN	20.2MIN	20.2MIN	20.2MIN	–
N	100 +2.0 −2.0	100 +2.0 −2.0	100 +2.0 −2.0	100 +2.0 −2.0	–
W1	12.4 +3.0 −0.0	16.4 +3.0 −0.0	24.4 +3.0 −0.0	32.4 +3.0 −0.0	–
W2	16.4 +2.0 −2.0	20.4 +2.0 −2.0	28.4 +2.0 −2.0	36.4 +2.0 −2.0	–
W3	13.65 +1.75 −0.75	17.65 +1.75 −0.75	25.65 +1.75 −0.75	33.65 +1.75 −0.75	–

14. ORDERING INFORMATION

Ordering Part Number	Description	Minimum Order Quantity(MOQ)
MG2450-B72	72-pin VFBGA Package	490(tray),2500(reel)
MG2455-F48	48-pin QFN Package	260(tray),2500(reel)

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About RadioPulse Inc.

RadioPulse is a Being Wireless solution provider offering wireless communication & network technologies and developing next generation wireless networking technologies.

The new wireless networking solutions envisioned by RadioPulse will enable user to enjoy wireless technologies with easy interface.

Founded in April of 2003, the company maintains it headquarters and R&D center in Seoul, Korea.