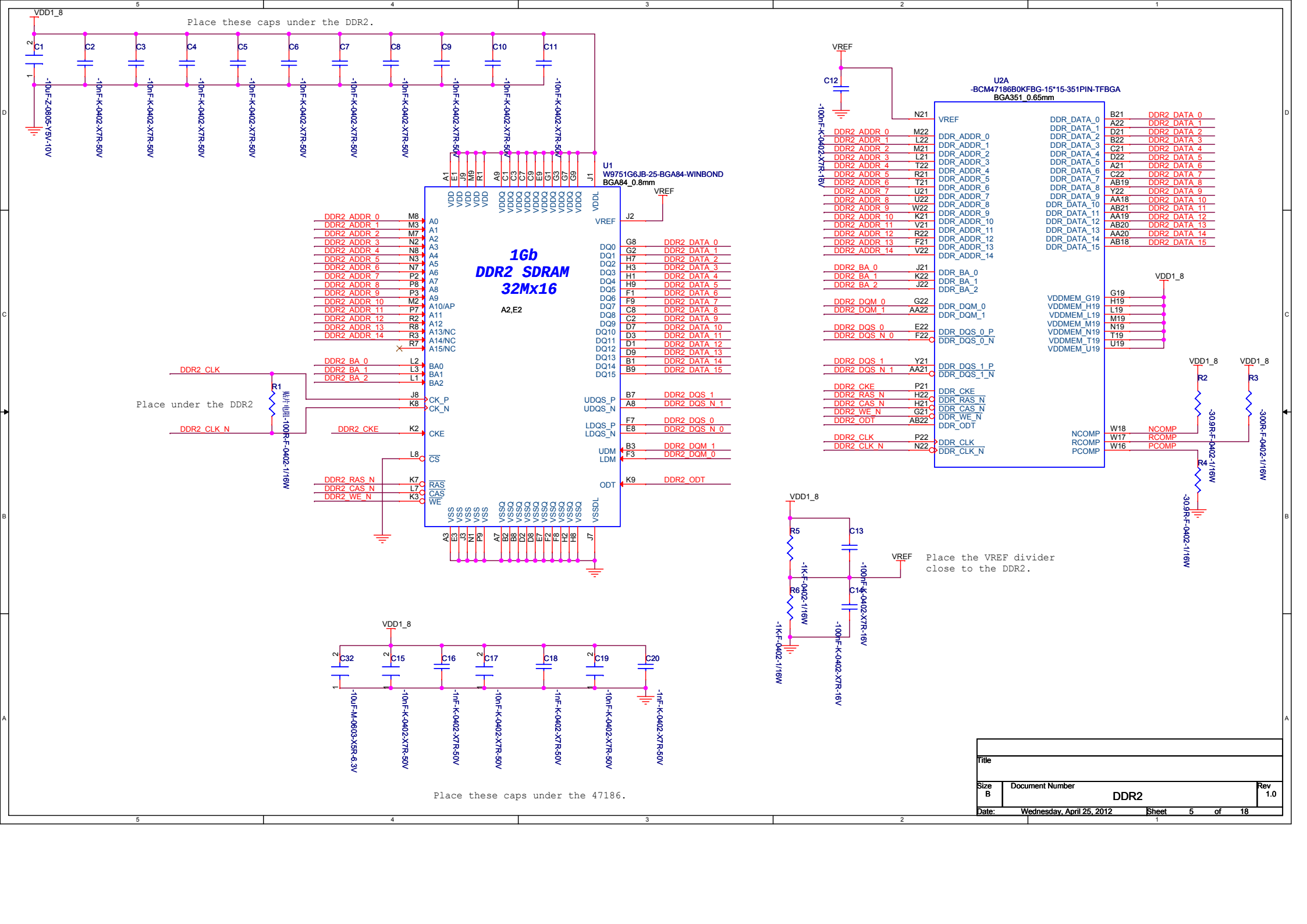
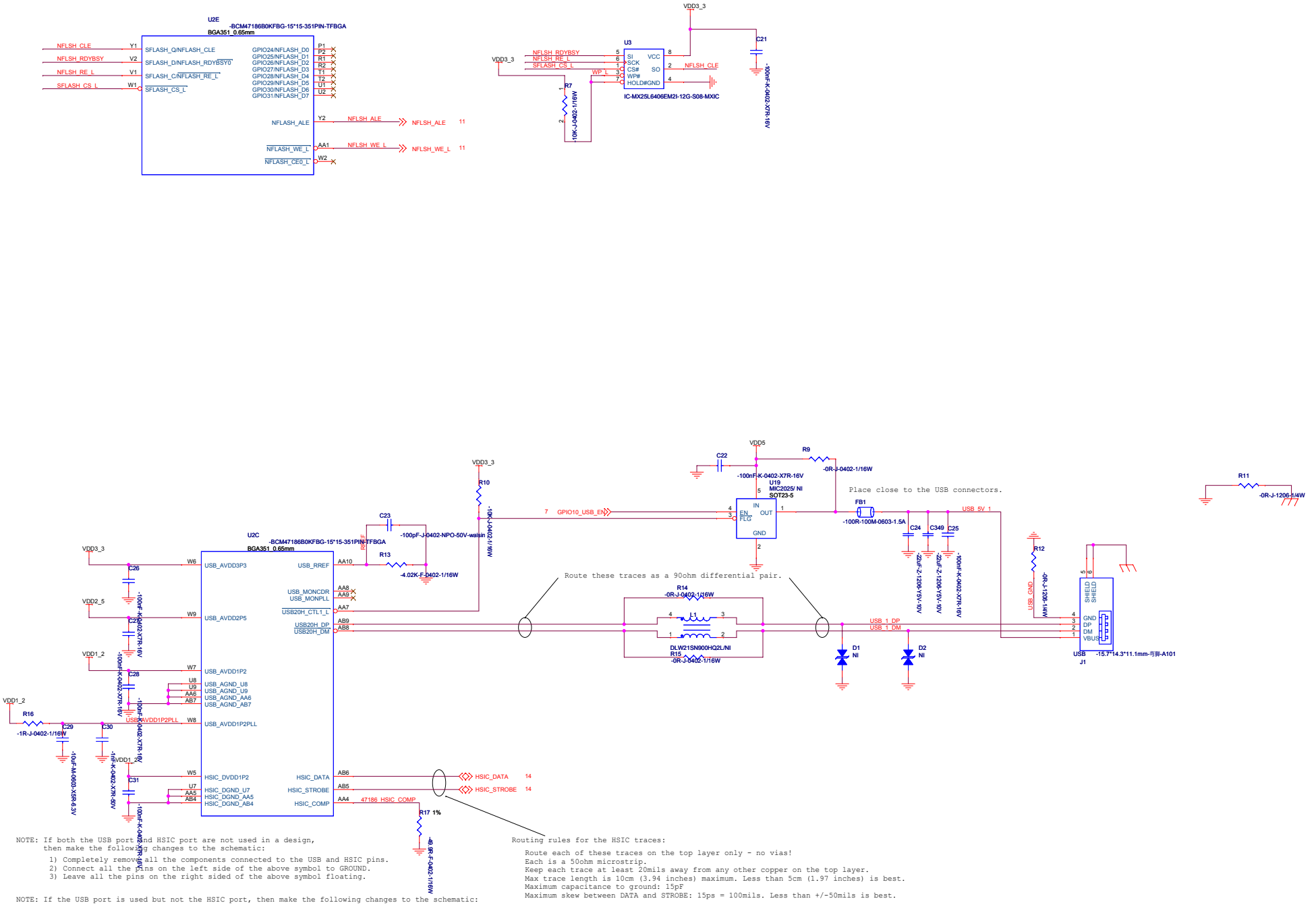

Place these caps under the DDR2.
VDD1_8
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
-10uF-Z-0805-Y5V-10V
-10nF-K-0402-X7R-50V
U1
W9751G6JB-25-BGA84-WINBOND
BGA84_0.8mm
1Gb
DDR2 SDRAM
32Mx16
A2,E2
VREF
DDR2_ADDR_0
DDR2_ADDR_1
DDR2_ADDR_2
DDR2_ADDR_3
DDR2_ADDR_4
DDR2_ADDR_5
DDR2_ADDR_6
DDR2_ADDR_7
DDR2_ADDR_8
DDR2_ADDR_9
DDR2_ADDR_10
DDR2_ADDR_11
DDR2_ADDR_12
DDR2_ADDR_13
DDR2_ADDR_14
DDR2_BA_0
DDR2_BA_1
DDR2_BA_2
DDR2_CLK
DDR2_CLK_N
DDR2_CKE
DDR2_RAS_N
DDR2_CAS_N
DDR2_WE_N
DDR2_ODT
DDR2_DQS_0
DDR2_DQS_N_0
DDR2_DQS_1
DDR2_DQS_N_1
DDR2_DQM_0
DDR2_DQM_1
DDR2_DATA_0
DDR2_DATA_1
DDR2_DATA_2
DDR2_DATA_3
DDR2_DATA_4
DDR2_DATA_5
DDR2_DATA_6
DDR2_DATA_7
DDR2_DATA_8
DDR2_DATA_9
DDR2_DATA_10
DDR2_DATA_11
DDR2_DATA_12
DDR2_DATA_13
DDR2_DATA_14
DDR2_DATA_15
R1
贴片电阻-100R-F-0402-1/16W
Place under the DDR2
U2A
-BCM47186B0KFBG-15*15-351PIN-TFBGA
BGA351_0.65mm
C12
-100nF-K-0402-X7R-16V
VDD1_8
R2
R3
R4
-30.9R-F-0402-1/16W
-300R-F-0402-1/16W
NCOMP
RCOMP
PCOMP
R5
R6
-1K-F-0402-1/16W
C13
C14
-100nF-K-0402-X7R-16V
Place the VREF divider close to the DDR2.
C32
C15
C16
C17
C18
C19
C20
-10uF-M-0603-X5R-6.3V
-1nF-K-0402-X7R-50V
Place these caps under the 47186.
Title
Size B
Document Number
DDR2
Rev 1.0
Date: Wednesday, April 25, 2012
Sheet 5 of 18



NOTE: If both the USB port and HSIC port are not used in a design, then make the following changes to the schematic:

1) Completely remove all the components connected to the USB and HSIC pins.
2) Connect all the pins on the left side of the above symbol to GROUND.
3) Leave all the pins on the right sided of the above symbol floating.

NOTE: If the USB port is used but not the HSIC port, then make the following changes to the schematic:

1) Connect the HSIC_DVDD1P2 to 1.2V.
2) Connect the HSIC_DGND pins to GROUND.
3) Leave the HSIC_DATA, HSIC_STROBE, and HSIC_COMP pins floating.

NOTE: If the USB port is not used but the HSIC port used, then make the following changes to the schematic:

1) Connect the USB power and ground pins as shown above.
2) Leave the USB_RREF, USB20H_CTL1, USB20H_DP, and USB20H_DM pins floating.

Routing rules for the HSIC traces:

Route each of these traces on the top layer only - no vias!
Each is a 50ohm microstrip.
Keep each trace at least 20mils away from any other copper on the top layer.
Max trace length is 10cm (3.94 inches) maximum. Less than 5cm (1.97 inches) is best.
Maximum capacitance to ground: 15pF
Maximum skew between DATA and STROBE: 15ps = 100mils. Less than +/-50mils is best.

Title			
Size: Custom	Document Number: Flash, USB, HSIC		Rev: 1.0
Date: Wednesday, April 25, 2012	Sheet 6 of 18		

50 OHMs

11 TXG_0 >> TXG_0 — C166 — C169 IN — C170 IN — 47186_TXG_0_MID — C171 1pF-C-0402-NPO-50V-walsin/NI — L24 1.8nH-S-0402-MLK1005S1N8ST-TDK/NI — C167 — L23 2.7nH-S-0402-MLG1005S2N7ST-TDK/NI — 15pF-J-0402-NPO-50V-walsin

11 47186_VRXA0_0 >> 47186_VRXA0_0 — R84 -0R-J-0402-1/16W — 2G_VRXA0_0 — C168 4.7pF-C-0402-NPO-50V-walsin

U8 Switch-GW1179-SOT323-6-Qwaye: SW1 VCC2 (6) / GND ANT (5) / SW2 VCC1 (4); ANT0_2G_OUT — C172 1ANT0_2G_MID — C173 15pF-J-0402-NPO-50V-walsin — ANT0_2G >> ANT0_2G 18; L25 NI; L26 NI

50 OHMs

50 OHMs

11 RXG_0 >> RXG_0 — C174 -9pF-C-0402-NPO-50V-GRM1555C1H9R0CA01D — 47186_RXG_0_MID — C176 NI — L28 NI — L27 NI — C175 -9pF-C-0402-NPO-50V-GRM1555C1H9R0CA01D

11 47186_VTXA0_0 >> 47186_VTXA0_0 — R85 0R-J-0402-1/16W — 2G_VTXA0_0 — C178 4.7pF-C-0402-NPO-50V-walsin

50 OHMs

11 RXG_1 >> RXG_1 — C180 -9pF-C-0402-NPO-50V-GRM1555C1H9R0CA01D — 47186_RXG_1_MID — C182 NI — L30 NI — L29 NI — C181 -9pF-C-0402-NPO-50V-GRM1555C1H9R0CA01D

11 47186_VTXA1_1 >> 47186_VTXA1_1 — R86 -0R-J-0402-1/16W — 2G_VTXA1_1 — C185 4.7pF-C-0402-NPO-50V-walsin

U9 Switch-GW1179-SOT323-6-Qwaye: SW1 VCC2 (6) / GND ANT (5) / SW2 VCC1 (4); ANT1_2G_OUT — C186 1ANT1_2G_MID — C187 9pF-C-0402-NPO-50V-GRM1555C1H9R0CA01D — ANT1_2G >> ANT1_2G 18; L31 NI; L32 NI

50 OHMs

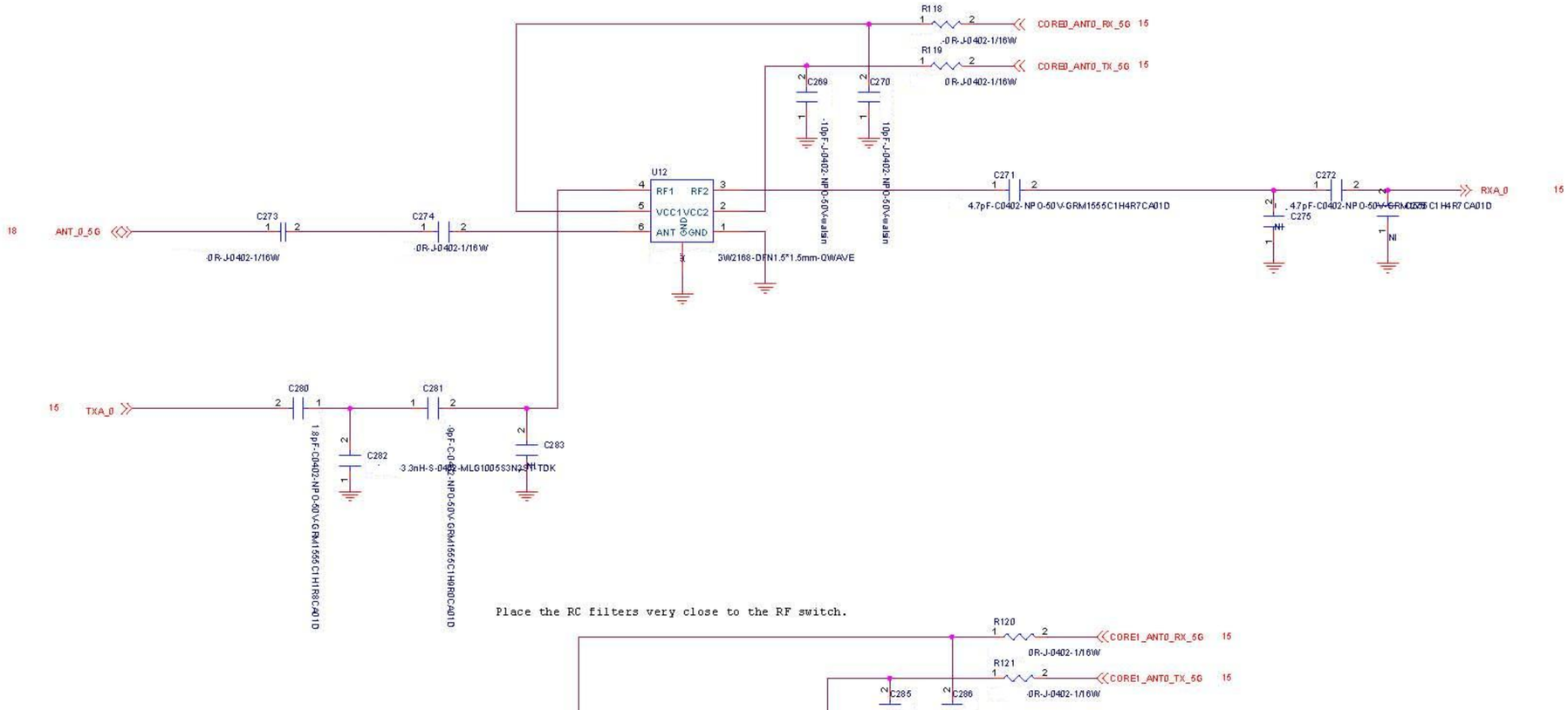
50 OHMs

11 TXG_1 >> TXG_1 — C188 -9pF-C-0402-NPO-50V-GRM1555C1H9R0CA01D — C189 IN — C190 NI — 47186_TXG_1_MID — C191 1pF-C-0402-NPO-50V-walsin/NI — L34 1.8nH-S-0402-MLK1005S1N8ST-TDK/NI — C192 — L33 2.7nH-S-0402-MLG1005S2N7ST-TDK/NI — 9pF-C-0402-NPO-50V-GRM1555C1H9R0CA01D

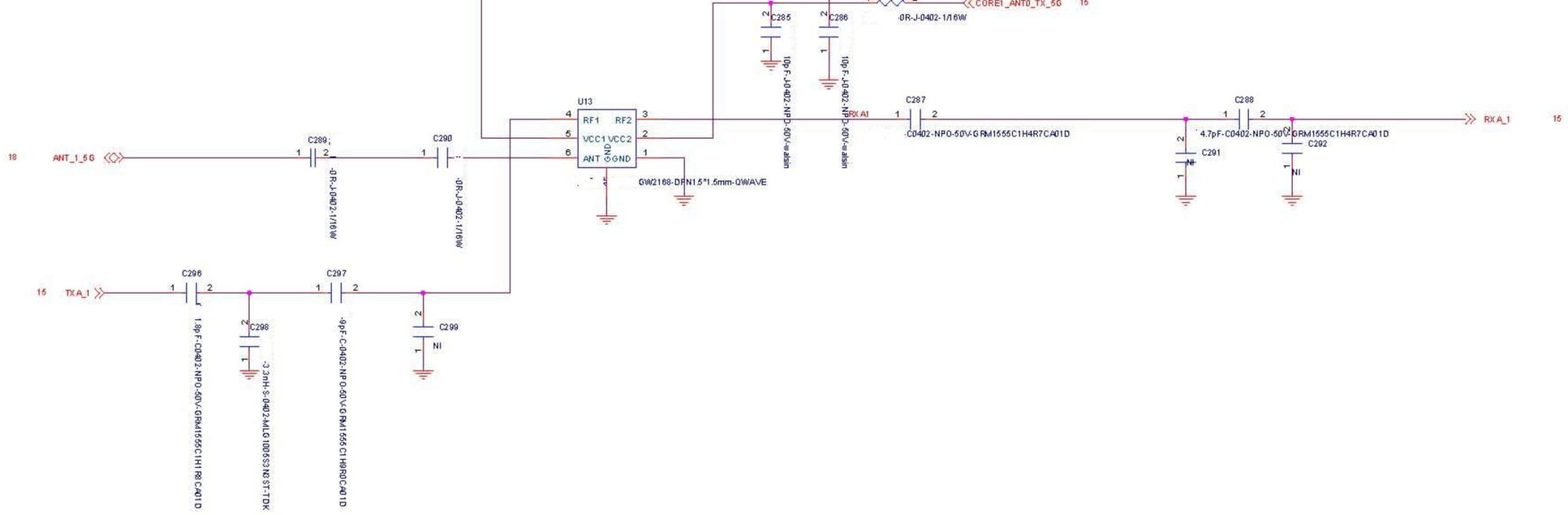
11 47186_VRXA1_1 >> 47186_VRXA1_1 — R87 -0R-J-0402-1/16W — 2G_VRXA1_1 — C193 4.7pF-C-0402-NPO-50V-walsin

Title			
Size C	Document Number 2.4G RF		Rev 1.0
Date: Wednesday, April 25, 2012	Sheet 12 of 18		

Place the RC filters very close to the RF switch.



Place the RC filters very close to the RF switch.

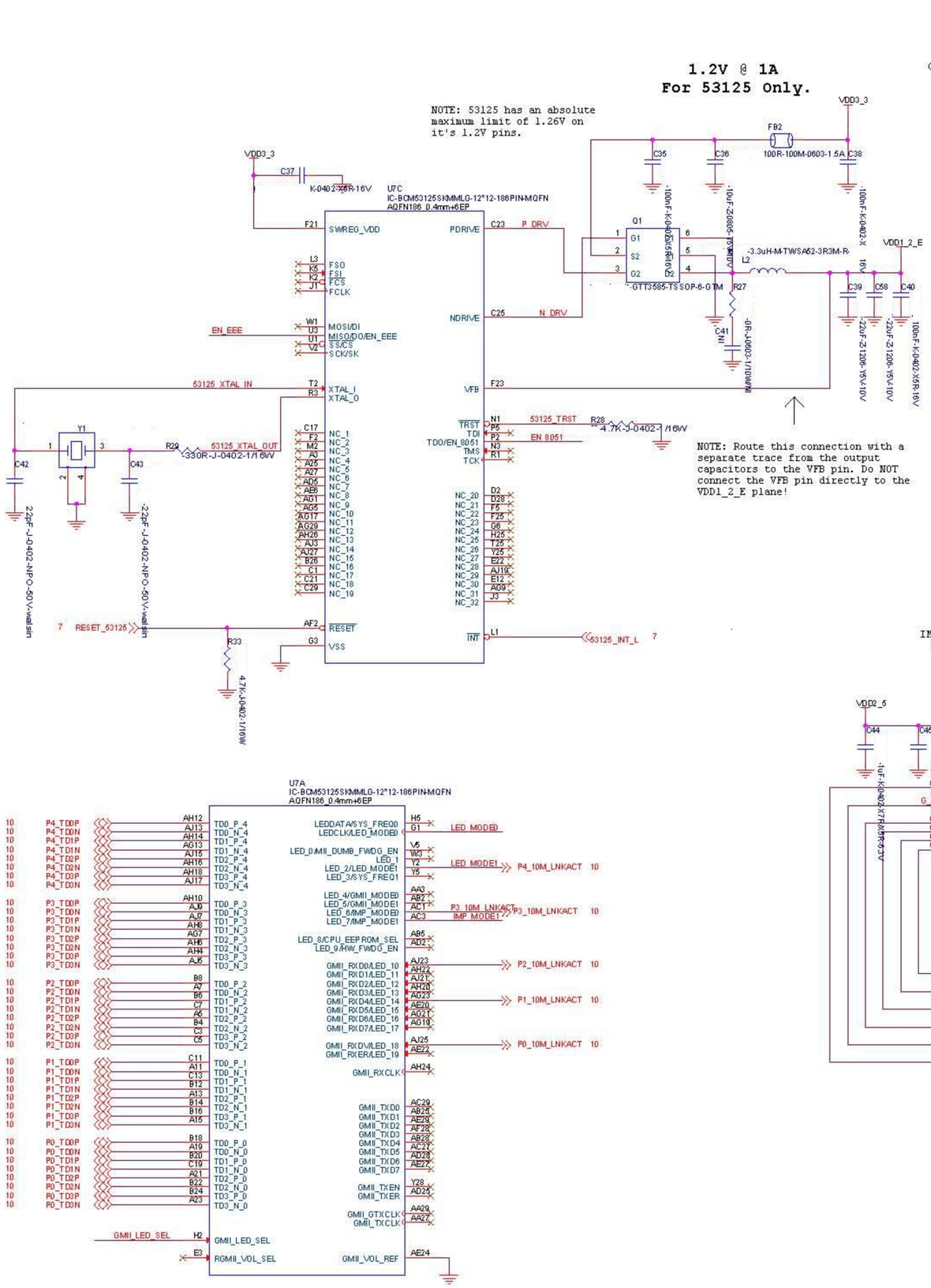


Title		
Size C	Document Number 5G RF	Rev 1.0
Date: Wednesday, April 25, 2012	Sheet 16 of 18	

U7D
IC-BCM53125SKMMLG-12*12-186PIN-MQFN
AQFN186_0.4mm+6EP

DVDD decoupling
OVDD decoupling
OVDD2 decoupling
OTP_VDD decoupling
OVDD3 decoupling
AVDDL decoupling
AVDDH decoupling

Title		
Size B	Document Number 53125 Power	Rev 1.0
Date: Wednesday, April 25, 2012	Sheet 9 of 18	



VDD3_3 R24 GMII_LED_SEL 4.7K-J-0402-1/16W

GMII_LED_SEL Strapping option:
Set port 5 pins as LED signals.

VDD3_3 R25 EN_8051 4.7K-J-0402-1/16W

EN_8051 Strapping option:
Disable internal 8051.

VDD3_3 R26 LED_MODE0 4.7K-J-0402-1/16W/NI

LEDMODE[1:0] Strapping option:
Set LEDMODE = 11b
LEDMODE[1] has internal pullup.

LED Functions
1G Link/Activity
100M Link/Activity
10M Link/Activity
Duplex (not used)

R31 IMP_MODE1 4.7K-J-0402-1/16W
R32 P3_10M_LNKACT 4.7K-J-0402-1/16W

IMPMODE[1:0] Strapping option:
Set IMPMODE = 00b = RGMII

Strap Pin	Function	Setting	Default	LED Polarity
IMP_VOL_SEL	Voltage used when IMP port is in RGMII mode: 0=2.5V 1=1.5V	0*	0	-
RGMII_VOL_SEL	Voltage used when Port 5 is in RGMII mode: 0=2.5V 1=1.5V	0*	0	-
GMII_LED_SEL	Port 5 signal select: 0=Port 5 signals 1=LED outputs	1	0	-
EN_8051	Enable the embedded 8051 microcontroller: 0=Disable, 1=Enable	0	1	-
MII_DUMB_FWDG_EN	IMP port configuration: 0=Require special header for all traffic 1=Forward all traffic	1*	1	LED0: low
LEDMODE[1:0]	LED Mode (see datasheet for settings)	10	10	LED2: low
SYS_FREQ[1:0]	System clock: 00: 83MHz 01: 91MHz 10: 100MHz 11: 111MHz	10*	10	LED3: low
GMII_MODE[1:0]	Interface Mode for WAN/port 5: 00: RGMII, 01: MII, 10: RvMII, 11: GMII	11*	11	LED4: low LED5: low
IMP_MODE[1:0]	IMP Port Mode: 00: RGMII 01:MII 10: RvMII 11:GMII	00	11	LED6: high LED7: high
CPU_EEPROM_SEL	0: Enable EEPROM Interface 1: Enable SPI & MDC/MDIO Interface	1*	1	LED8: low
HW_FWDG_EN	Fordwarding enabled at reset: 0=Disabled (needs S/W enable) 1=Enabled (no S/W config needed)	1*	1	LED9: low
EN_EEE	Energy Efficient Ethernet: 0=Disabled 1=Enabled	0	1	-

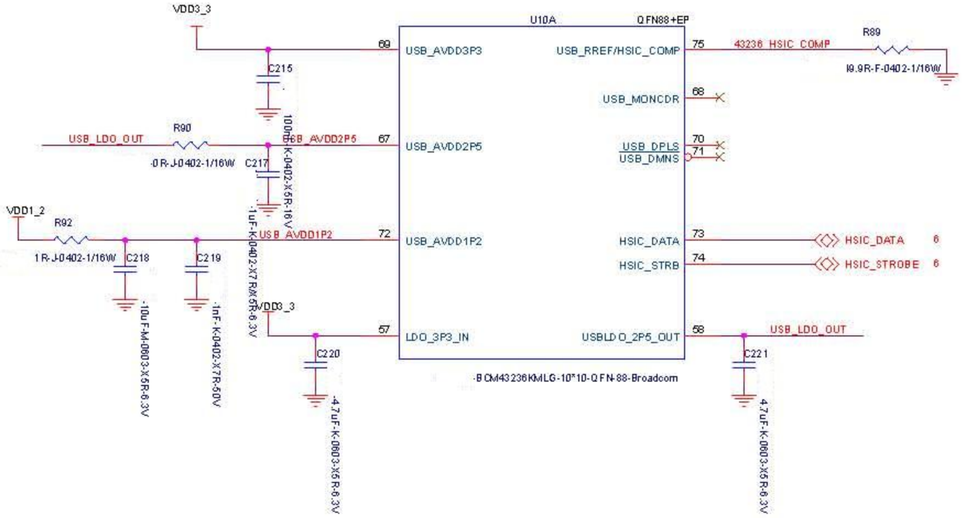
* = Strapping option set at default with no option to change.

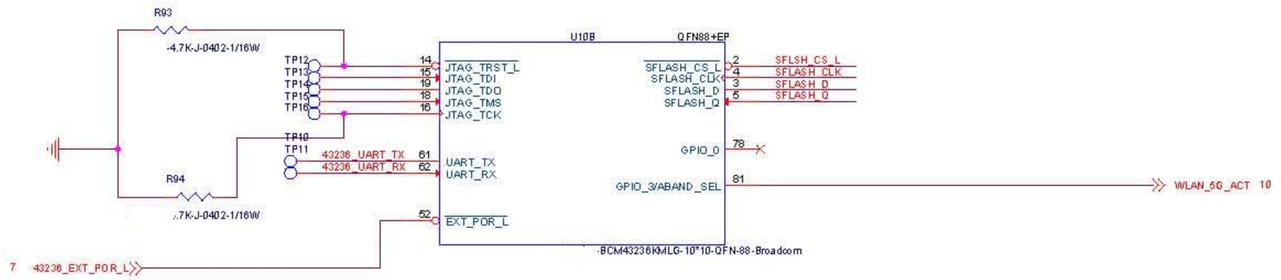
R30 EN_EEE 4.7K-J-0402-1/16W

EN_EEE Strapping option:
Disable Energy Efficient Ethernet due to 53125 erratas.

Note: 1) Both the 53125 and the 47186 have built in series terminators for a 50ohm output impedance. All RGMII traces should have a 50-60ohm impedance.
2) The TX traces, G_TXD[3:0] and G_TXCTRL, must be length matched to the G_TXC trace length to within +/-100mils. Same for RX traces relative to G_RXC.

Title			
Size C	Document Number 53125 GigE Switch		Rev 1.0
Date: Wednesday, April 25, 2012	Sheet 8 of 18		





Title		
Size C	Document Number 43236 HSIC, JTAG, etc	Rev 1.0
Date: Wednesday, April 25, 2012	Sheet 14 of 18	

Connections from C223 to R96 & R97
needs to be a "star-point". Place the
0.1uF caps right at the 43236 pins.

Connections from C248 to R103 & R105
needs to be a "star-point". Place the
0.1uF caps right at the 43236 pins.

Place the 100pF caps
right at pins 29 & 38.

NOTE: Keep the 43236_GPAIO
trace as short as possible.

43236 Strapping Option Pin	Function	Setting	Default Pull
CORE1_ANT0_TX	0 = Serial Flash NOT present [default] 1 = Serial Flash present	0	PD
CORE0_ANT0_RX	0 = Serial Flash Type is ST Micro [default] 1 = Serial Flash Type is Atmel	0*	PD
CORE0_ANT1_TX	0 = HSIC mode (board setting) 1 = USB 2.0 PHY mode [default]	0	PU
CORE0_ANT1_RX	0 = backplane at 96 (98.4) MHz 1 = backplane at 120 (123) MHz [default]	1	PU
CORE0_ANT0_TX	0 = Do not use OTP for configuration (setting) 1 = Use OTP for configuration [default]	0	PU
GPIO[7:6] LNA_5G_PU_1/ LNA_5G_PU_0	00 = boot from RAM, ARM held in reset 01 = boot from ROM [default] 10 = Reserved 11 = Reserved	01	none

* = Strapping option set at the detfault with no option to change.

GPIO[7:6] Strapping Options:
Set to boot from ROM. If serial flash is present and programmed, 43236 will boot from serial flash.

A standard 4.7K pullup will not be able to overpower the R174/Q6 load on page 14 so a strong external pullup is needed to assure a "1" is read for the strapping option when "Boot from ROM" is set.

CORE0_ANT1_TX Strapping Option:
Set HSIC mode.

CORE0_ANT1_RX Strapping Option:
Option to set 96(98.4) backplane clock.

CORE0_ANT0_TX Strapping Option:
Set to NOT use OTP for configuration.

CORE1_ANT0_TX Strapping Option:
Set serial flash NOT PRESENT.

Title		
Size: C	Document Number: 43236 Xtal, Analog, RF	Rev: 1.0
Date: Wednesday, April 25, 2012	Sheet 15 of 18	