RM2-1000 EnviroGrid Controller

RF Theory of operation

DESCRIPTION

RF Circuit

The RF circuit consists of the following sections:

1. MRF24J40 transceiver with balun and bias network.
2. Two 2/1 switches separating the TX and RX branches.
3. A power amplifier along with a band-pass filter in the TX branch.

The diagram is shown in Fig 1.

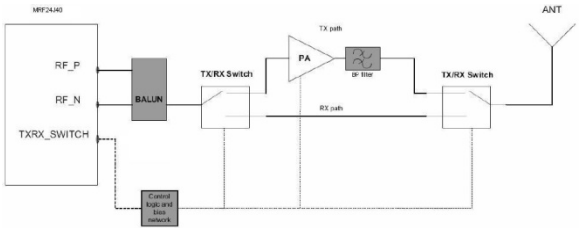

Fig 1

MRF24J40 Transceiver

The block diagram of the Microchip MRF24J40 transceiver module is shown in Fig 2.

The MRF24J40 device integrates a receiver, transmitter, VCO and PLL into a single integrated circuit. It uses advanced radio architecture to minimize external part count and power consumption. The MRF24J40 MAC/base band provides hardware architecture for both IEEE 802.15.4 MAC and PHY layers. It mainly consists of TX/RX FIFOs, a CSMA-CA controller, superframe constructor, receive frame filter, security engine and digital signal processing module.

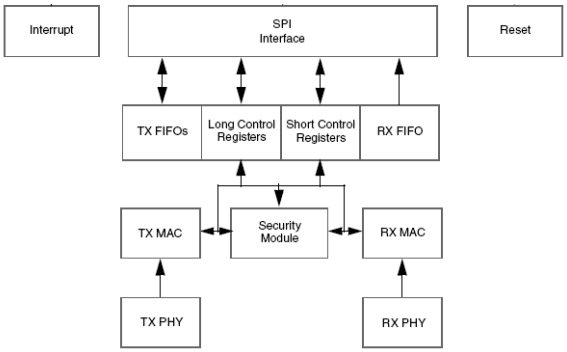

Fig 2

The MRF24J40 consists of four major functional blocks:

1. An SPI interface that serves as a communication channel between the host controller and the MRF24J40.
2. Control registers which are used to control and monitor the MRF24J40.
3. The MAC (Medium Access Control) module that implements IEEE 802.3™ compliant MAC logic.
4. The PHY (Physical Layer) driver that encodes and decodes the analog data.

© 2008 Copyright REGEN Energy Inc.

The device also contains other support blocks, such as the on-chip voltage regulator, security module and system control logic.

The MRF24J40 is designed to operate at 20 MHz. It has an internal PLL that must lock before the device is capable of transmitting or receiving packets.
The MRF24J40 receiver features a low IF architecture and consists of an LNA, a pair of down conversion mixers, polyphase channel filters, baseband limiter amplifiers and RSSI technology. An ADC is used to sample the RSSI value and the sampled data is stored in a register from which the data can be read out via the SPI bus. The local oscillator generation circuits (VCO, PLL and buffers) are shared with the receiver and transmitter. The Low Noise Amplifier (LNA) features a differential input for high performance. The RX/TX switch is integrated and LNA input and Power Amplifier (PA) output share the same pins. The transmitter features a direct conversion architecture and has a 0 to -38.75 dBm output power. The output power adjustment is in 1.25 dB step. The TX gain is programmed by the SPI bus.

The MRF24J40 features differential RF input/output circuit. The balun converts a differential unbalanced input and converts it to a balanced singled-ended output and visa versa.

2/1 Switches

The µPG2214TB is a GaAs MMIC for L, S-band SPDT (Single Pole Double Throw) switch which was developed for mobile phone and other L, S-band applications.

This device can operate 2 controls switching by control voltage 1.8 to 5.3 V. This device can operate frequency from 0.05 to 3.0 GHz, having the low insertion loss and high isolation.

Power Amp and Bandpass Filter

The µPG2314T5N is GaAs HBT MMIC for power amplifier which was developed for Bluetooth Class 1. This device realizes high efficiency, high gain and high output power by using InGaP HBT. This is shown in Fig 3.

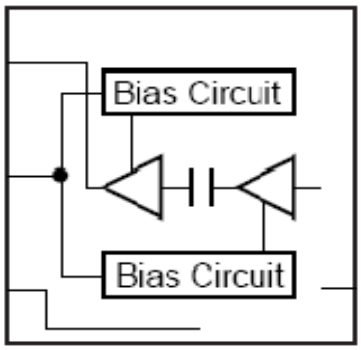

Fig 3

The 2450BP14C0100 2.45 GHz Band Pass Filter at the output of the amplifier attenuates noise and harmonics as shown below in Fig 4.

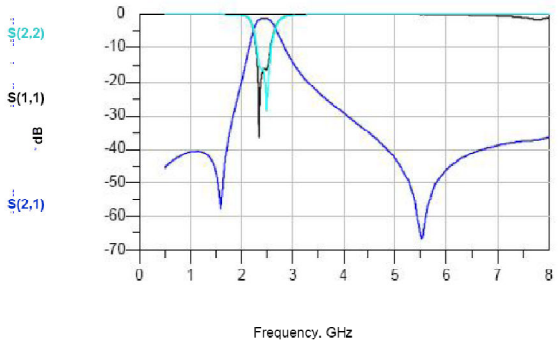

Fig 4

.

© 2008 Copyright REGEN Energy Inc.