Last Metre Connectivity™

K2-MSP6150 Bluetooth Module

Datasheet

KTwo Technology Solutions

North Block, 1st Floor IT-BT Park, Rajajinagar Industrial Estate, Bangalore - 560 010

Phone: +91-80-23144422 Fax: +91-80-23144411 Web: www.ktwo.co.in

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Revision History

#	Date	Document Version No.	Change Description	Reason for Change
1.	28th Mar 2008	1.0	Created	
2.	11th Jun 2008	1.1	Added few missing pin descriptions	
3.	25th Jun 2008	1.2	Added List of Tables	
4.	16th Jul 2008	1.3	Added U.S. Regulatory wireless notice	

Definitions, Acronyms and Abbreviations

Abbreviations	Description
BT	Bluetooth
SPP	Serial Port Profile
OPP	Object Push Profile
HFP	Hands Free Profile
HSP	Head Set Profile
GPIO	General Purpose Input Output
UART	Universal Asynchronous Receive transmit
I2C	Inter IC Communication
SPI	Synchronous serial Port Interface
PCM	Pulse Code Modulation
I2S	Inter IC Sound
BER	Bit Error Rate
bps	Bits per second

1 Features

- Class 2 Bluetooth® module
- Bluetooth 2.0 Specification Conformance
- Texas Instruments HPABT6150 base-band with integrated 2.4GHz RF Transceiver
- On-Board 2.4GHz antenna
- On-board Texas Instruments MSP430 processor with application specific Bluetooth stack and profiles
- PCM interface for voice channel: Linear, A-law and u-law companding
- Low power consumption
- General I/O interface
- H4 interface for HCI transport

2 Applications

- Medical Systems
- Digital Camera
- Industrial and Domestic appliances
- Embedded systems
- Automotive applications
- Handheld, laptop and Desktop Computers
- Computer Peripherals (keyboard, mouse etc.)

3 Description

The K2-MSP6150 Bluetooth Module is suitable for wireless applications involving data and voice communications. The developers can easily integrate Bluetooth wireless into their product. The Bluetooth module provides plug and go solution, hence reducing the time to market for the products.

The on-board MSP430 microcontroller enables the user to embed their Bluetooth stack above HCI layer, Bluetooth profiles and custom application.

The Bluetooth module is readily available with application for transferring the wireless data over SPP/OPP seamlessly to the connected device from KTwo. Custom applications may be made available upon request, using KTwo's Stack and profiles: SPP, HSP, HFP, OPP, HID etc.

4 Device Pinouts

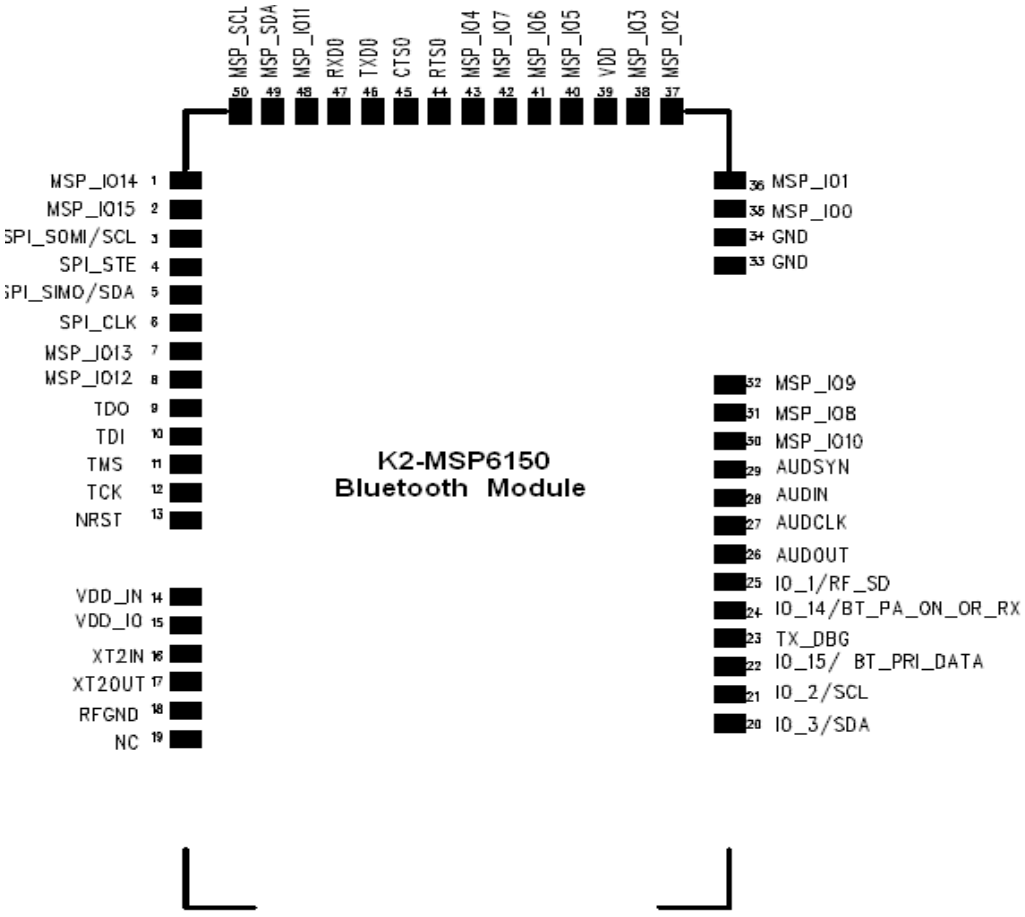


Figure 1 Pinouts for K2-MSP6150 BT module

5 Device Terminal functions

Table 1 Device Terminal Functions

Pin Name	Pin No.	Pin Type	Description
VDD_IO	15	Power	Supply for I/O ring
VDD_IN	14	Power	Supply for RF and baseband
VDD	39	Power	Supply for MSP430 micro-controller
GND	33, 34	Ground	Ground
RF_GND	18	Ground	Ground
TX_DBG	23	CMOS Output	Debug UART transmit data
TXD0	46	CMOS Output	MSP430 UART data transmit
RXD0	47	CMOS Input	MSP430 UART data receive
CTS0	45	CMOS Input	MSP430 UART clear-to-send (GPIO reserved for CTS0)
RTS0	44	CMOS Output	MSP430 UART request-to-send (GPIO reserved for RTS0)
AUDIN	28	CMOS Input	Codec Audio data input
AUDOUT	26	CMOS Output	Codec Audio data output
AUDCLK	27	CMOS Input/Output	Codec transmit/Receive clock
AUDSYN	29	CMOS Input/Output	Codec frame synchronization control
IO_1/RF_SD	25	CMOS Input/Output	General purpose I/O / WLAN Control signal
IO_2/SCL	21	CMOS Input/Output	General purpose I/O / I2C clock
IO_3/SDA	20	CMOS Input/Output	General purpose I/O / I2c data
IO_14/ BT_PA_ON_ OR_TX	24	CMOS Input/Output	General purpose I/O / WLAN Control signal
IO_15/	22	CMOS	General purpose I/O / WLAN Control

BT_PRI_DATA		Input/Output	signal
MSP_IO0	35	CMOS Input/Output	General-purpose digital I/O pin/Timer_A, clock signal TACLK input/Comparator_A output
MSP_IO1	36	CMOS Input/Output	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output
MSP_IO2	37	CMOS Input/Output	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
MSP_IO3	38	CMOS Input/Output	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2
MSP_IO4	43	CMOS Input/Output	General-purpose digital I/O pin/SMCLK signal output
MSP_IO5	40	CMOS Input/Output	General-purpose digital I/O pin/Timer_A, compare: Out0 output
MSP_IO6	41	CMOS Input/Output	General-purpose digital I/O pin/Timer_A, compare: Out1 output
MSP_IO7	42	CMOS Input/Output	General-purpose digital I/O pin/Timer_A, compare: Out2 output
MSP_IO8	31	CMOS Input/Output	General-purpose digital I/O pin/analog input a3 – 12-bit ADC
MSP_IO9	32	CMOS Input/Output	General-purpose digital I/O pin/analog input a4 – 12-bit ADC
MSP_IO10	30	CMOS Input/Output	General-purpose digital I/O pin/analog input a1 – 12-bit ADC
MSP_IO11	48	CMOS Input/Output	General-purpose digital I/O pin/analog input a2 – 12-bit ADC
MSP_IO12	8	CMOS Input/Output	General-purpose digital I/O pin/sub-main system clock SMCLK output
MSP_IO13	7	CMOS Input/Output	General-purpose digital I/O pin/main system clock MCLK output

MSP_IO14	1	CMOS Input/Output	General-purpose digital I/O pin/Timer_B, capture: CCI1A/B input, compare: Out1 output
MSP_IO15	2	CMOS Input/Output	General-purpose digital I/O pin/Timer_B, capture: CCI2A/B input, compare: Out2 output
TDI	10	CMOS Input	Test data input or test clock input.
TDO	9	CMOS Output	Test data output port.
TMS	11	CMOS Input	Test mode select. TMS is used as an input port for device programming and test.
TCK	12	CMOS Input	Test clock (JTAG). TCK is the clock input port for device programming test and bootstrap loader start
NRST	13	CMOS Input	Reset input, non-maskable interrupt input port, or bootstrap loader start.
SPI_SOMI/SCL	3	CMOS Input/Output	General-purpose digital I/O pin/USCI B1slave out/master in SPI mode, SCL I2C clock in I2C mode
SPI_SIMO/SDA	5	CMOS Input/Output	General-purpose digital I/O pin/USCI B1slave in/master out in SPI mode, SDA I2C data in I2C mode
SPI_CLK	6	CMOS Input/Output	General-purpose digital I/O/USCI B1 clock input/output, USCI A1 slave transmit enable
SPI_STE	4	CMOS Input/Output	General-purpose digital I/O pin/USCI B1 slave transmit enable
XT2IN	16	CMOS Input	Input port for crystal oscillator XT2
XT2OUT	17	CMOS Output	Output terminal of crystal oscillator XT2
MSP_SDA	49	CMOS Input/Output	General-purpose digital I/O pin/USCI B0 slave in/master out in SPI mode, SDA I2C data in I2C mode
MSP_SCL	50	CMOS Input/Output	General-purpose digital I/O pin/USCI B0 slave out/master in SPI mode, SCL I2C clock in I2C mode

6 K2-MSP6150 Bluetooth module Block Diagram

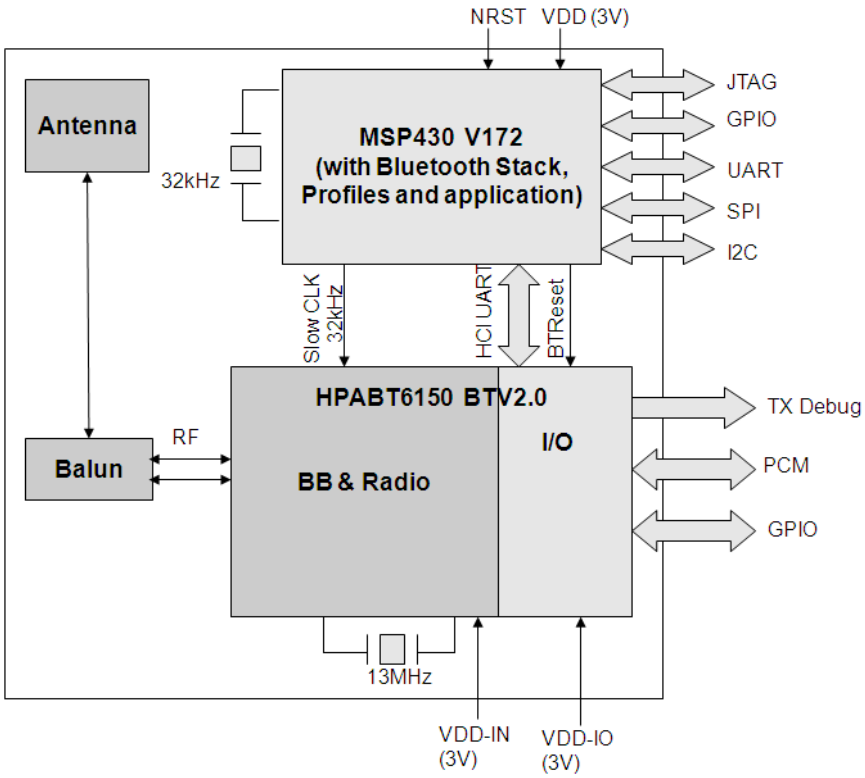


Figure 2 Block Diagram of K2-MSP6150 Module

K2-MSP6150:

This module is based on HPABT6150 Bluetooth RF and Baseband chip. It consists of on-board MSP430 low power micro-controller with 56kB flash and 4kB RAM. The upper layer Bluetooth protocol stack and application reside on the MSP430. The clocks necessary for HPABT6150 and MSP430 are made available through on-board crystals. The K2-MSP6150 module also contains on-boa **Crystals:**

The 32.768 kHz crystal is used by MSP430 as the reference clock for all peripherals. The on-board 13MHz crystal is used as fast clock for HPABT6150.

Balun:

The Balun changes the balanced input/output signal of the HPABT6150 to unbalanced signal to feed to the monopole antenna. The filter is a band pass filter (ISM band).

Matching:

Antenna matching components match the antenna to 50 Ohms.

Antenna:

The chip antenna from Fractus is used to send and receive Bluetooth RF signals.

HCI UART:

The HCI UART is the transport layer protocol used for communication between HPABT6150 and MSP430.

BT Reset:

The reset to HPABT6150 is supplied from the MSP430 processor.

Slow Clock:

The slow clock for the HPABT6150 is supplied by MSP430 processor.

PCM Interface:

The audio pulse code modulation (PCM) Interface supports continuous transmission and Reception of PCM encoded audio data over Bluetooth.

TX Debug Interface:

The Transmit Debug interface supports logging the Bluetooth transactions. This is used for Debugging only.

UART Interface:

The standard Universal Asynchronous Receiver Transmitter (UART) interface from MSP430 is provided for communicating with other serial devices.

SPI Interface:

The synchronous serial port interface (SPI) from MSP430 is provided for interfacing with other digital devices.

I2C interface:

The Inter IC Communication interface (I2C) from MSP430 is provided for interfacing with other devices.

GPIO:

There are 16 General Purpose Input/Output signals from MSP430, which can be programmed for other alternate functionalities. Also 5 General Purpose Input/Output signals from HPABT6150, configurable for alternate functions.

JTAG interface:

This is the standard JTAG interface for programming the on-board MSP430 flash.

NRST:

Reset input to the MSP430.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Rating	Min	Max	Unit
Supply voltage VDD_IN	-0.5	+4.2	V
Supply voltage VDD_IO	-0.5	+4.2	V
Supply voltage VDD	-0.3	+4.1	V
Input voltage to all MSP_IO pins	-0.3	VDD+0.3	V
Input voltage to Analog pins	-0.5	+2.1	V
Input voltage to all other pins	-0.5	VDD_IO	V
Operating Ambient Temperature	-40	+85	°C
Storage Temperature	-40	+105	°C
Peak Current Consumption		TBD	mA

7.2 Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Characteristics	Min	Max	Unit
Supply voltage VDD_IN	1.9	3.6	V
Supply voltage VDD_IO	1.65	3.6	V
Supply voltage VDD	1.8	3.6	V
Supply voltage during flash programming	2.2	3.6	V
Processor frequency, with VDD = 1.8V, and duty cycle 50% ±10%	dc	6	MHz
Processor frequency, with VDD = 2.7V, and duty cycle 50% ±10%	dc	12	MHz
Processor frequency, with VDD = 3.3V, and duty cycle 50% ±10%	dc	16	MHz
Positive-going input threshold voltage for MSP430 I/Os (VDD= 2.2V)	1	1.65	V
Positive-going input threshold voltage for MSP430 I/Os (VDD= 3V)	1.35	2.25	V
Negative-going input threshold voltage for MSP430 I/Os (VDD= 2.2V)	0.55	1.2	V
Negative-going input threshold voltage for MSP430 I/Os (VDD= 3V)	0.75	1.65	V
Pull--up/pull--down resistor (Pull--up: VIN = 0V, Pull--down: VIN = VDD)	20	50	kΩ
Pulse length at NRST pin to accept a reset	2		µs
High-level input voltage for HPABT6150 I/Os	0.7 X VDD_IO – 50mV	VDD_IO	V

Characteristics	Min	Max	Unit
Low-level input voltage for HPABT6150 I/Os	0	0.3 X VDD_IO + 50mV	V
High-level output voltage for HPABT6150 I/Os	0.8 X VDD_IO	VDD_IO	V
Low-level output voltage for HPABT6150 I/Os	0	0.22 X VDD_IO	V
Input transitions time from 10% to 90% (digital pins of HPABT6150 I/Os)	0	25	ns
Output rise time from 10% to 90% (digital pins of HPABT6150 I/Os)	-	4	ns
Output fall time from 10% to 90% (digital pins of HPABT6150 I/Os)	-	3	ns
Ambient Temperature	-40	85	°C
Storage Temperature	-55	125	°C

7.3 Current Consumption

Table 4 K2-MSP6150 Module Current Consumption

Module State	State Description	Current Consumption (mA)
Power Down	BT and MSP430 in Shutdown	0.032
Waiting for Connection	BT in Page and inquiry Scan and MSP430 in Low Power Mode	0.55
Connected State	BT in 1.28sec Sniff mode and MSP430 in Low Power Mode	0.73
Data Transfer State	BT in data Tx/Rx mode and MSP430 in Active mode (UART at 9600bps)	7.09

7.4 Radio Characteristics

All parameters are assured over the recommended voltage range and process types. Also, all the parameters with the Bluetooth specification column value are also assured over the extreme temperature conditions (if applicable) as defined in the Bluetooth spec.

All the Radio characteristics shown below are of HPABT6150 IC.

7.4.1 Receiver

Table 5 Receiver Characteristics

CHARACTERISTICS	CONDITION	BLUETOOTH SPECIFICATIONS	MIN	TYP	MAX	UNIT
Operation frequency range			2402		2408	MHz
Channel spacing				1		MHz
Sensitivity at matching network input	At BER = 0.1%	-70	-82	-85		dBm
Maximum useable input power at matching network input	At BER = 0.1%	-20	-5	-2		dBm
C/I performance†	Cochannel	11		9.8	10.6	dBm
	Adjacent 1 MHz/image freq	0		-5	-3	
	Adjacent −1 MHz	0		-8	-6	
	Adjacent 2 MHz/image +1 MHz freq	-20		-26	-23	
	Adjacent −2 MHz	-30		-35	-33	
	Adjacent 3 MHz¶	-40		-40	-37	
	Adjacent −3 MHz	-40		-47	-42	
	Adjacent > 3 MHz	-40		-47	-43	
Blocking performance‡	30 – 2000 MHz	-10	-10			dBm
	2000 – 2399 MHz	-27	-27			
	2484 – 3000 MHz	-27	-27			
	3000 – 12.75 GHz	-10	-10			
Blocking performance§ for various cellular standards Wanted signal at −72dBm, hopping on, DH1, BER = 0.1%, PER =	824−828 MHz (GSM)			-27		dBm
	828−848 MHz (GSM)			-11		
	824−828 MHz (CDMA)			-27		
	828−848 MHz			-23		

1%, continuous blocker, without BPF	(CDMA)					
	880–900 MHz (GSM)			-9		
	900–915 MHz (GSM)			-20		
	1710–1800 MHz (GSM)			-6		
	1800–1862 MHz (GSM)			-19		
	1862–1910 MHz (GSM)			-8		
	1710–1785 MHz (DCS)			-6		
	1850–1910 MHz (PCS)			-19		
	1850–1910 MHz (CDMA)			-20		
	1850–1910 MHz (WCDMA)			-14		
	1920–1980 MHz (WCDMA)			-15		

§ From host cellular transmitter modulated according to all listed cellular systems (GSM, CDMA etc.). All the results are given with –72 dBm wanted signal. All numbers are at the balun single ended.

¶ One exception out of the total five allowed in the Bluetooth spec

7.4.2 Transmitter

7.4.2.1 TX Amplifier (PA)

Table 6 Transmitter Characteristics – TX Amplifier

CHARACTERISTICS	CONDITION	BLUETOOTH SPECIFICATIONS	MIN	TYP	MAX	UNIT
RF output power at matching network output†	Default values		2	4	6	dBm
Gain control range				30		dB
Power control step		2 to 8	3	5	7	dB
Adjacent channel power |M−N| = 2		≤ −20 dBm		-40	-30	dBm

Adjacent channel power |M−N| > 2		≤ −40 dBm		-47	-45	dBm

7.4.2.2 Synthesizer

Table 7 Transmitter Characteristics – Synthesizer

CHARACTERISTICS	CONDITION	BLUETOOTH SPECIFICATIONS	Min	Typ	Max	Unit
Operation frequency range		2402 to 2483.5	2402		2480	MHz
−20 dB BW		≤ 1000		900	1000	kHz

7.4.2.3 Modulation (GFSKTB=0.5)

Table 8 Transmitter Characteristics – Modulation

CHARACTERISTICS	CONDITION	BLUETOOTH SPECIFICATIONS	MIN	TYP	MAX	UNIT
Bit rate				1		Mbps
Average deviation Detector bandwidth–10 MHz	Mod Data = 4−1, 4−0 1111000011110000…	140 to 175	140	160	175	kHz
Instantaneous deviation	Mod data = 1010101…	> 115	115	130		kHz
dF2/dF1		> 80	80	90		%
Carrier frequency drift	DH1	< ±25	-20	±10	20	kHz
	DH3	< ±40	-35	±15	35	
	DH5	< ±40	-35	±15	35	
Drift rate		< 20		5	15	kHz/ 50 µs
Initial carrier frequency tolerance†		±75			±25	kHz

† For 0 ppm fast clock

7.4.3 Transceiver

Table 9 Transceiver Characteristics

CHARACTERISTICS	CONDITION	BLUETOOTH Specifications	MIN	TYP	MAX	UNIT
Out-of-band emission for TX and RX	869–960 MHz (CDMA, GSM)			-133	-124	dBm/Hz
	925–960 MHz (GSM)			-136	-129	
	1570–1580 MHz (GPS)			-149	-144	
	1805–1990 MHz (GSM,DCS)			-144	-141	
	1930–1990 MHz (GSM,PCS,CDMA,WCDMA)			-147	-139	
	2010–2170 MHz (WCDMA)			-149	-145	
Spurious emission during operation†	30 MHz – 1 GHz			-74	-71	dBm
	1 GHz – 12.75 GHz			-44	-29	
	1.8 GHz – 1.9 GHz			-73	-71	
	5.15 GHz – 5.3 GHz			-74	-69	
LO leakage‡	Frf/4			-90	-72	dBm
	Frf×3/8			-90	-78	
	Frf/2			-77	-71	
	Frf×3/4			-84	-76	
	Frf			-85	-67	
	Frf×5/4			-80	-71	
	2×Frf			-64	-45	

† As defined in Bluetooth spec

‡ Frf is the received RF frequency

8 Power Supply

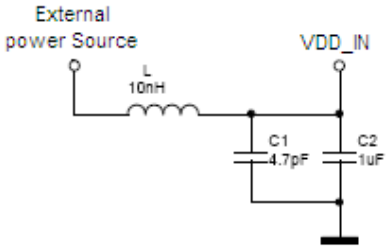
Proper power supplies must be chosen for the BT module. The Bluetooth module requires three power supplies for its operation:

a) VDD_IN: The main power supply for the core
   Range: 1.9V to 3.6V

a) VDD_IO: Supply for the I/O ring
   Range: 1.65V to 3.6V

a) VDD: Supply for the on-board MSP430 processor
   Range: 1.8V to 3.6V

It is recommended to use the LC circuit at the VDD_IN Supply point as shown below for RF noise filtering:



9 General Purpose IO

The following table describes all the available IO pins and the signals that can be multiplexed on these pins

Table 10 Description of GPIOs from MSP430

IO Pin	Default Function	Alternate Functionality	Description
MSP_IO0	GPIO	TACLK, CAOUT	General-purpose digital I/O pin/Timer_A, clock signal TACLK input / Comparator_A output
MSP_IO1	GPIO	TA0	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output
MSP_IO2	GPIO	TA1	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
MSP_IO3	GPIO	TA2	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2
MSP_IO4	GPIO	SMCLK	General-purpose digital I/O pin/SMCLK signal output
MSP_IO5	GPIO	TA0	General-purpose digital I/O pin/Timer_A, compare: Out0 output
MSP_IO6	GPIO	TA1	General-purpose digital I/O pin/Timer_A, compare: Out1 output
MSP_IO7	GPIO	TA2	General-purpose digital I/O pin/Timer_A, compare: Out2 output
MSP_IO8	GPIO	A3	General-purpose digital I/O pin/analog input a3 – 12-bit ADC
MSP_IO9	GPIO	A4	General-purpose digital I/O pin/analog input a4 – 12-bit ADC
MSP_IO10	GPIO	A1	General-purpose digital I/O pin/analog input a1 – 12-bit ADC
MSP_IO11	GPIO	A2	General-purpose digital I/O pin/analog input a2 – 12-bit ADC

IO Pin	Default Function	Alternate Functionality	Description
MSP_IO12	GPIO	SMCLK	General-purpose digital I/O pin/sub-main system clock SMCLK output
MSP_IO13	GPIO	MCLK	General-purpose digital I/O pin/main system clock MCLK output
MSP_IO14	GPIO	TB1	General-purpose digital I/O pin/Timer_B, capture: CCI1A/B input, compare: Out1 output
MSP_IO15	GPIO	TB2	General-purpose digital I/O pin/Timer_B, capture: CCI2A/B input, compare: Out2 output

In addition to these GPIOs, the K2BMMSP16150 BT module provides several configurable general purpose I/O pins from HPABT6150 device. These pins can be configured by using a Vendor Specific Commands. Each GPIO has a default function and value.

These pins are multiplexed with other peripheral pins (I2C, WLAN).

Table 11 Description of GPIOs from HPABT6150

IO Pin	Default Function	Alternate Functionality	Description	Default Reset Value
IO_1	-	GPIO, RF_SD	General purpose I/O or WLAN control signal	PD
IO_2	GPIO	SCL	General purpose I/O or I2C clock	PD
IO_3	GPIO	SDA	General purpose I/O or I2C Data	PU
IO_7	GPIO		General purpose I/O	PD
IO_14	GPIO	BT_PA_ON_OR_RX	WLAN control	PD
IO_15	GPIO	BT_PRI_DATA	WLAN control	PD

Note: Required to use a HCI vendor specific command for enabling alternate functionality

10 Audio Codec Interface

10.1 PCM Codec Interface

This interface consists of four signals: a clock AUD_CLK, a data input AUD_IN, a data output AUD_OUT, and a frame-synchronization signal AUD_FSYNC.

This interface offers a wide flexibility by providing the following parameters configurable by a vendor-specific HCI command:

- PCM highway master/slave role selection
- PCM highway clock frequency
- Frame-synchronization format (short frame, long frame, frame polarity)
- Data position in the Frame

10.1.1 PCM Master/Slave Configuration:

The Bluetooth module can act as PCM master or slave, configured via HCI Vendor specific command. When set to slave mode, PCMSYNC and PCMCLK pins act as inputs. When set to master mode, PCMSYNC and PCMCLK pins act as outputs. After reset the PCM interface is set to slave.

10.1.2 Bluetooth module as PCM Master:

PCM clock frequency: Capable of generating the clock between 64 kHz and 3.072 MHz (with 100Hz resolution).

PCM Sync: PCM frame Sync period configurable from 1 to 2048 in 1 clock increments

Frame sync duty-cycle (frame sync length) is fully configurable as well (from 1 to the Frame Sync period).

10.1.3 Bluetooth module as PCM Slave:

PCM clock frequency: Accepts any clock frequencies between 64 kHz and 10 MHz.

PCM Sync: frame-sync periods from 1 to 2048 times the audio clock period in one-clock increments, and duty cycles from 1 to 2047 times the audio-clock period

10.1.4 Two channel PCM codec Operation

In the following figure, a 2-channel PCM bus is shown where the two channels have different word sizes and arbitrary positions in the bus' frame. (FT stands for Frame Timer)

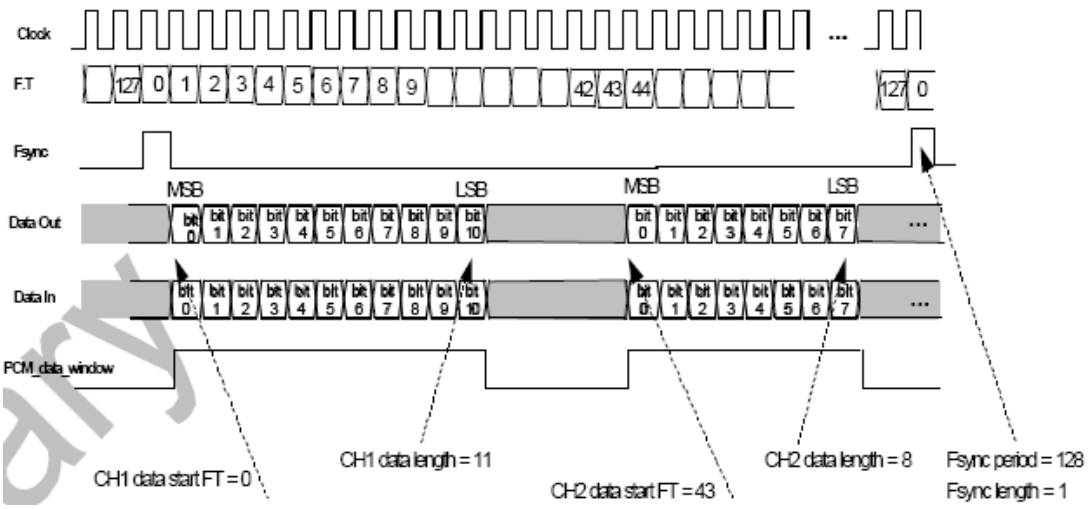


Figure 3 Two Channel PCM Bus Timing

10.1.5 Audio Encoding

- A-law (8-bit)
- u-Law (8-bit)
- Linear (8 or 16-bit)
- Transparent (for VoHCI)

10.2 I2S Codec Interface

1. In Inter-IC Sound (I2S) mode, the CODEC port interface can be configured as an I2S link serial interface to the I2S CODEC device.
2. The I2S Link serial interface is a time division multiplexed (TDM) slot based serial interface, which is used to transfer both audio data and command/status to the CODEC device.
3. In I2S mode, the CODEC port interface is configured as a bi-directional full duplex interface with two time slots per frame:
    - Time slot 0 is used for the left channel audio data and
    - Time slot 1 for the right channel audio data.
4. Each time slot is configurable up to 40 serial clock cycles in length and the frame is configurable up to 80 serial clock cycles in length.

11 Host Interface

The K2-MSP6150 module facilitates additional standard interfaces for communicating with host system.

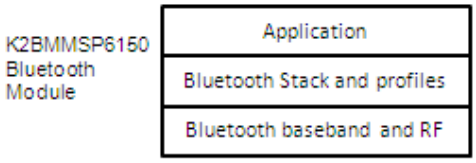
The interfaces listed below provide alternatives for the communication means between the K2-MSP6150 and the host processor:

- SPI interface
- I2C interface
- UART interface

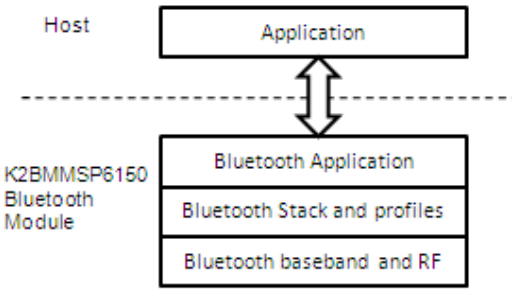
12 Firmware

The K2-MSP6150 Bluetooth module has an on-board MSP430 micro-controller with 56kB flash and 4kB RAM. The K2-MSP6150 Bluetooth module can be used with two types of configurations:

1. Standalone Bluetooth application embedded on the module.



2. Bluetooth application controlled by host application.



Detailed information on Bluetooth Protocol stack structure is available in the following Documents:

1. Driver Protocol Information.pdf
2. K2BMMSP6150 SPP Software User Guide.pdf

13 Application Information

13.1 Soldering recommendations

Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus the following recommendation should be taken as a starting point guide.

a) The K2-MSP6150 module uses bottom pads. The modules are optimized for soldering on both automatic and manual assembly line. For manual soldering, solder pads on the target board may, in some situation, be made slightly larger to allow easier heating process.

b) K2-MSP6150 module is compatible with industrial standard reflow profile for lead-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

c) Refer technical documentations of particular solder paste for profile configurations

d) Avoid using multiple flows

e) Reliability of the solder joint and self-alignment of the component are dependent on the solder volume. Minimum of 150mm stencil thickness is recommended

f) Aperture size of the stencil should be 1:1 with the pad size

g) A low residue, “no clean” solder paste should be used due to low mounted height of the component

13.2 Layout Guidelines

It is strongly recommended to use good layout practices to ensure proper operation of the module.

a) Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module.

b) To achieve good RF performance it is recommended to place ground plane(s) beneath the module but not under the antenna.

c) Except from the ground plane, it is preferable to mount as few components and other material as possible nearby the antenna. Free air is the best surrounding for the antenna.

d) All GND pins, including RF_GND must be connected directly to a flooded ground-plane. If more than one ground layer is used, then make a good connection between them using many via holes.

e) There shall be no copper around and under the antenna as shown in the figure 3:

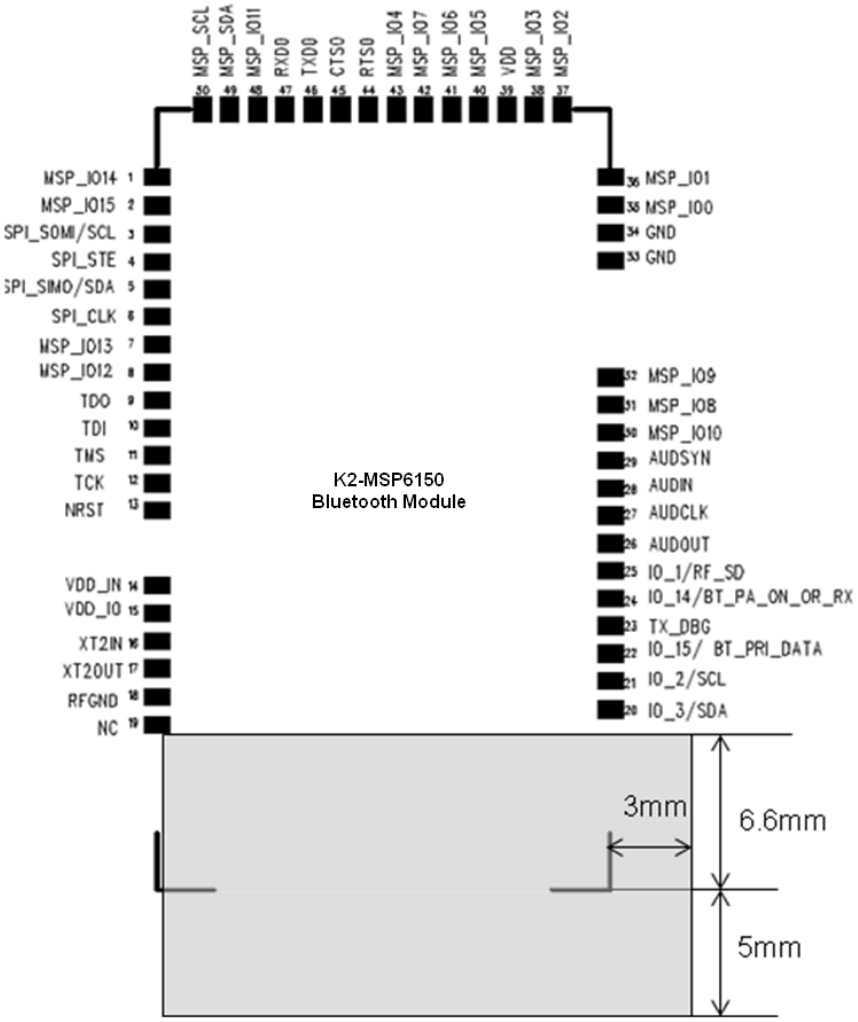


Figure 4 No-Metal Area

13.3 Typical Application Block Diagram

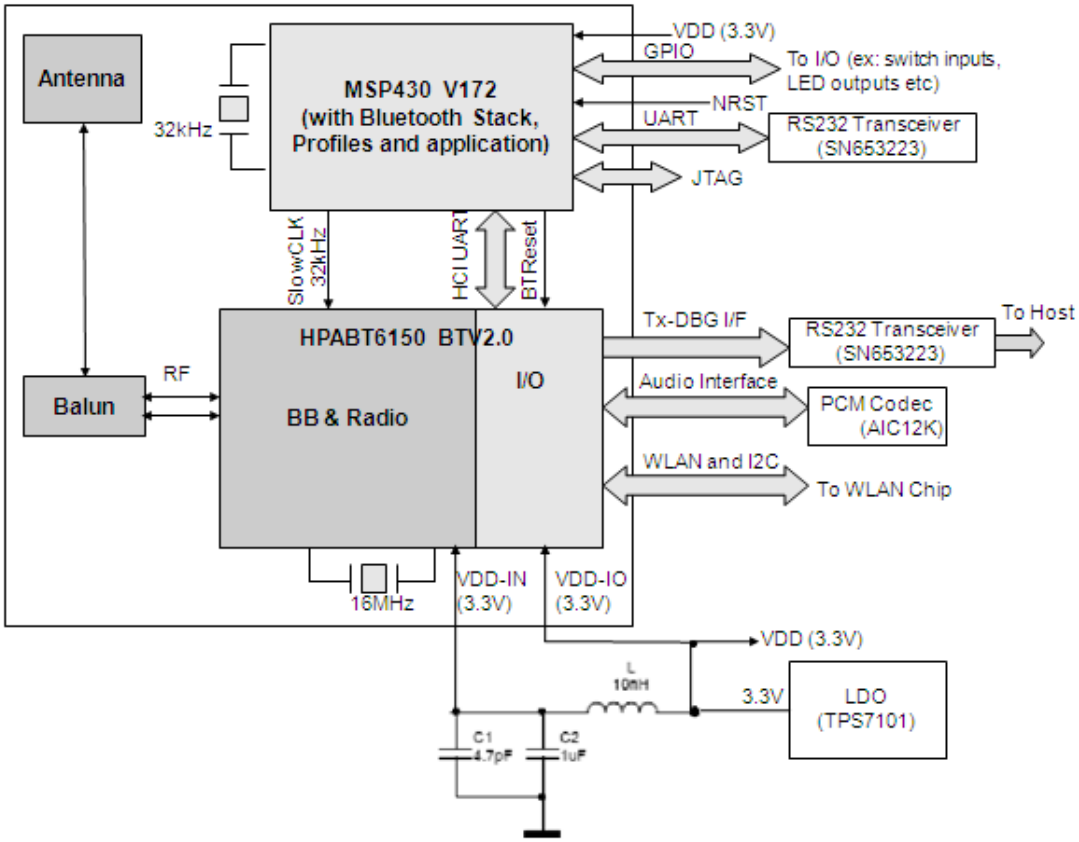


Figure 5 Typical Application Block Diagram

14 Packing Information

Physical Size:

Length : 18mm

Width : 31.5mm

Height :

Weight: TBD

15 Footprint and Dimensions

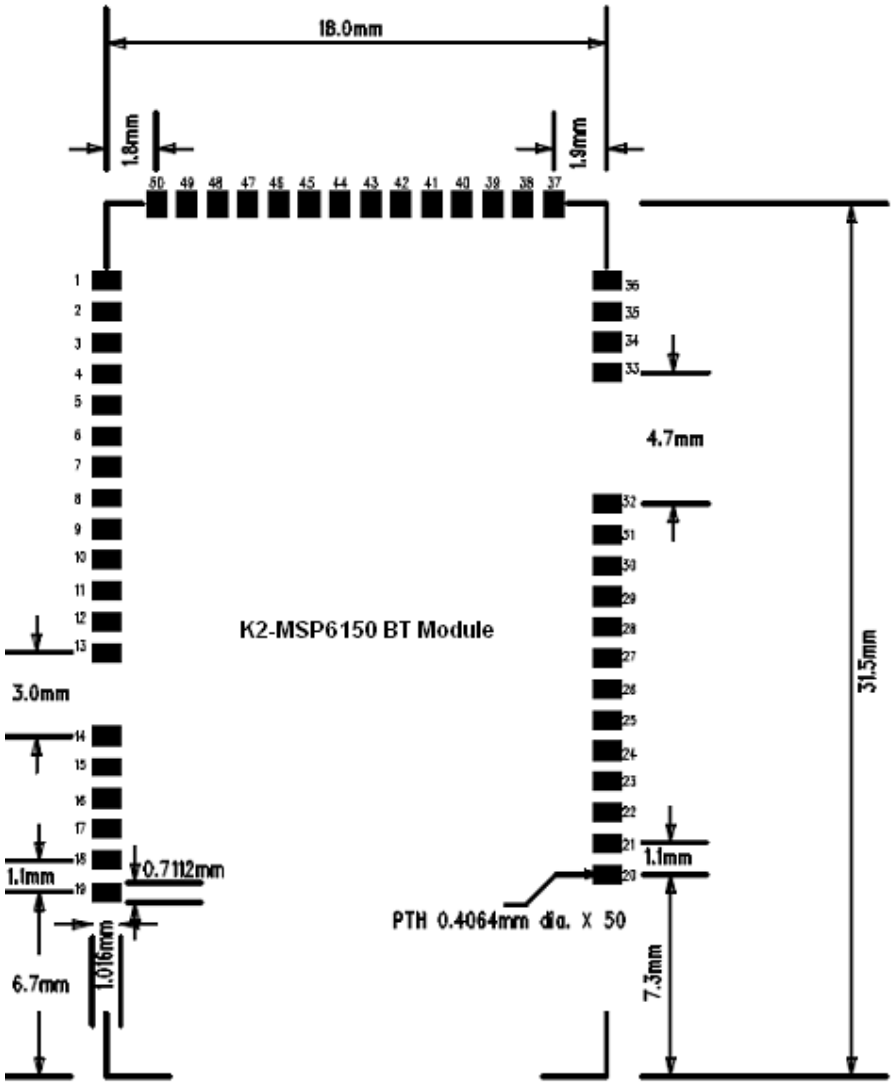


Figure 6 Footprint and Dimensions

16 U.S. Regulatory Wireless Notice

FEDERAL COMMUNICATION COMMISSION INTERFERENCE STATEMENT

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE:

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

This device is intended only for OEM integrators under the following conditions:

The transmitter module may not be co-located with any other transmitter or antenna,

As long as above conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

The final end product must be labeled in a visible area with the following: "Contains FCC ID:WH8K2MSP6150".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.