AS3993

UHF RFID Single Chip Reader EPC Class1 Gen2 Compatible

General Description

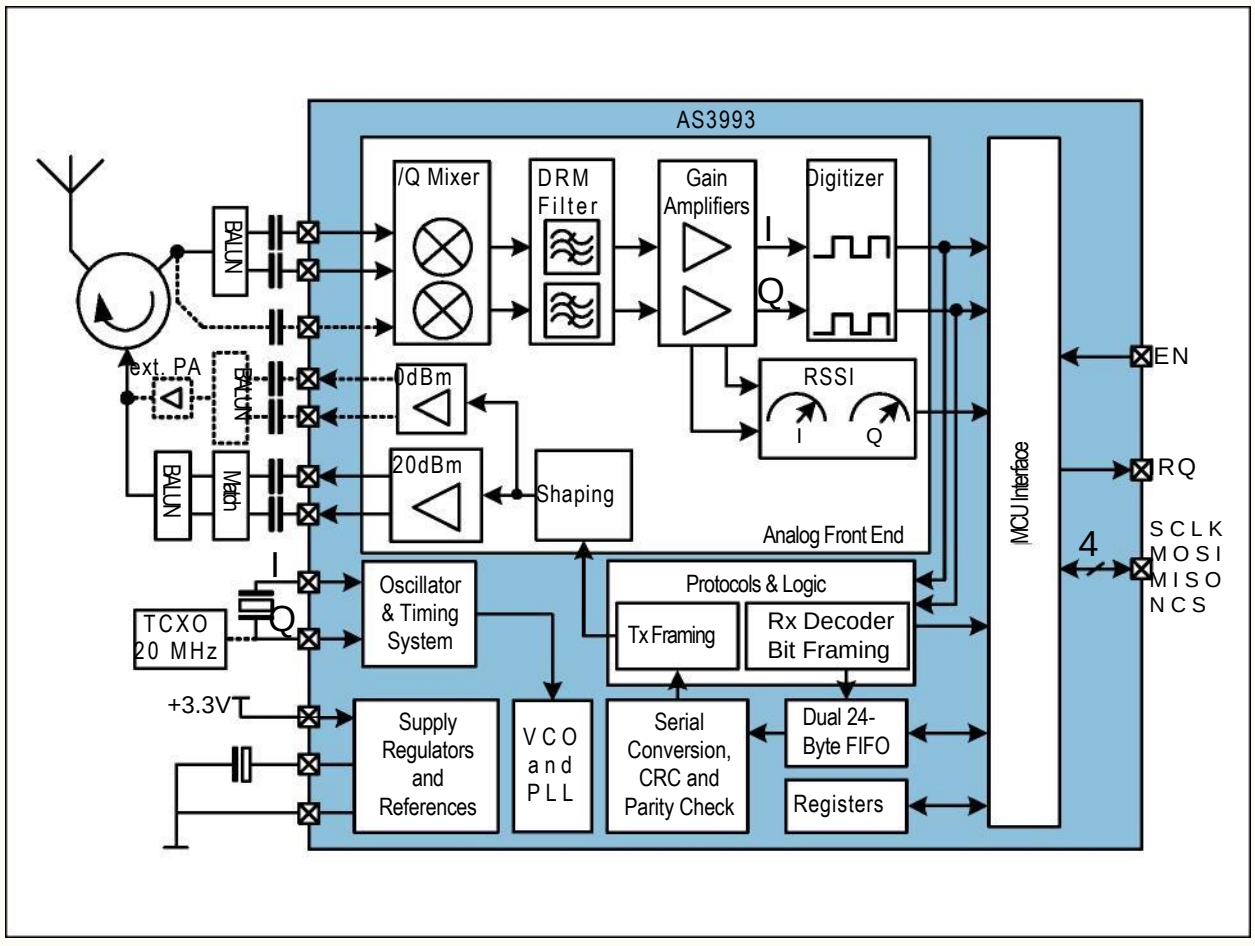
The AS3993 is an EPC Class 1 Gen 2 RFID reader IC which implements all the relevant protocols, including ISO 18000-6C, the ISO 29143 air-interface protocol for mobile RFID interrogators, and ISO 18000-6A/B (for operation in direct mode).

Benefit	Feature
Optimized for battery operation	Supply voltage range: 3.0V to 3.6V: • Limited operation possible down to 2.7V • Maximum PA supply voltage: 4.3V • Peripheral I/O supply range: 1.65V to 5.5
High Sensitivity	DRM: 250 kHz and 320 kHz filters for M4 and M8
World-wide shippable product	Frequency Hopping Support
Flexible modulation method	ASK or PR-ASK modulation
Small package footprint – saving PCB area	48-pin QFN (7x7x0.9 mm) package
Wide temperature range	-40°C to 85°C

- Battery-powered stationary readers.

Figure AS3993 – 2:
Block Diagram

AS3993 Block Diagram: Basic block diagram of AS3993 reader device



Pin Assignment

The AS3993 pin assignments are described below.

Figure AS3993 – 3: Pin Diagram

AS3993 Pin Assignment: This figure shows the pin assignment and location viewed from top.

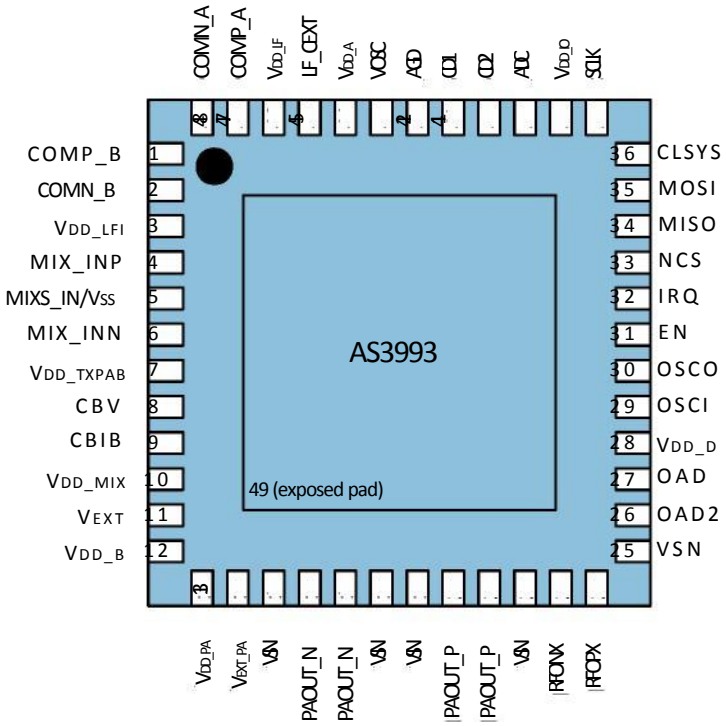


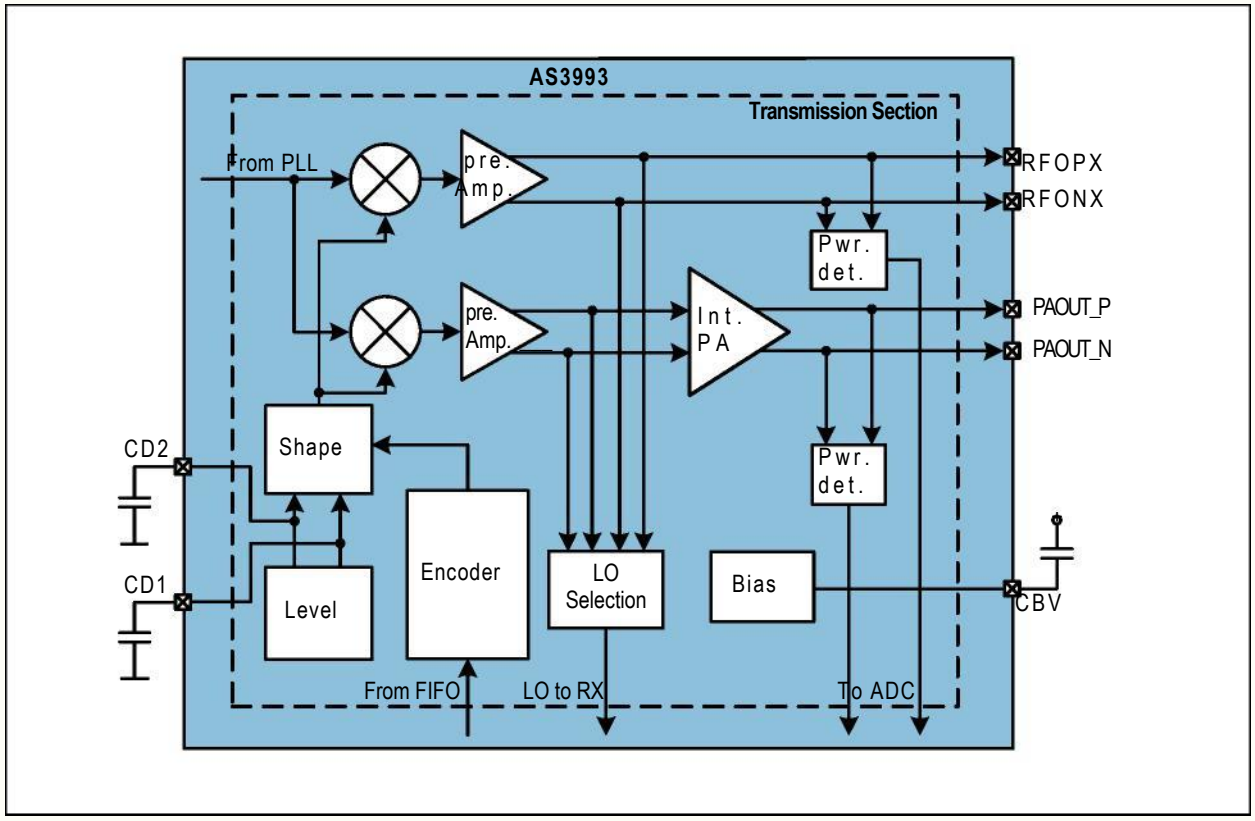
Figure AS3993 – 4: Pin Description

Pin Number 48-pin QFN	Pin Name	Pin Type	Description
1	COMP_B	Analog I/O	Internal node, connect de-coupling capacitor to VDD_LFI
2	COMN_B	Analog I/O	Internal node, connect de-coupling capacitor to VDD_LFI
3	VDD_LFI	Supply pad	Positive supply for LF input stage, connect to VDD_MIX
4	MIX_INP	Analog input	Positive differential mixer input
5	MIXS_IN/VSS	Analog input	Single ended mixer input
6	MIX_INN	Analog input	Negative differential mixer input
7	VDD_TXPAB	Supply pad	Bias positive supply. Connect to VDD_MIX
8	CBV	Analog I/O	Internal node, connect de-coupling capacitor to VDD_MIX
9	CBIB	Analog I/O	Internal node, connect de-coupling capacitor to ground
10	VDD_MIX	Analog I/O	Mixer positive supply, internally regulated

Transmission Section

The transmitter section comprises of a data handling, an encoding part, a shaping circuitry, a modulator and amplifier circuitry.

Figure AS3993 – 24:
Transmission Section



Block Diagram Transmission Section: This figure shows a detailed block diagram of the transmission section of the AS3993 device.

The RF carrier is modulated with a shaped representation of the transmit data and (pre-) amplified for transmission.

Tx Data Handling and Coding

The data handling part takes the baseband data from the FIFO and encodes it according to the Gen2 protocol (PIE). It adds a preamble or a frame-sync and calculates the CRC. The digital modulation signals are feed to the shape circuitry.

Tx Shape Circuitry

The modulation shape is controlled by a double D/A converter. The first 5-bit logarithmic converter forms two voltages, which define minimum and maximum $_{(Vpp)}$ modulation signal level. The two voltages are filtered by two external capacitors connected to the CD1 and CD2 pins to minimize the noise level and are used as a reference for the shaping circuitry. The second 9-bit linear converter transforms the digital modulation signal into a sinusoidal or linear shaped analog modulation signal. The output of the shaping circuit is interpolated and connected to the modulator input.

Local Oscillator (LO) Path

To improve the phase noise rejection, the local oscillator signal is derived from the output of the pre-amplifier stages. For optimal operation, the pre-amplifier levels should be close to nominal (set by **TX_lev<4:0>** in register 15h). In case lower levels are used, the LO signal can be increased by approximately 6 dB using option bit **eTX<7>**. The drawback is increased received noise.

Modulator

The modulator modulates the RF carrier with the shaped representation of the digital modulation signal. The internal modulator is capable of ASK and PR-ASK modulation.

Tx Level and Shape Adjustments

The output level and modulation shape properties are controlled by the Modulator Control Registers 1 - 4 (13h-16h). The level of the output signal is adjusted by option bits **TX_lev<4:0>** in Modulator Control Register 3 (15h). For good performance, it is advised to design the exterior circuit of the reader device as such that the reader output power is set close to the AS3993 nominal output power. In case temporarily operation at decreased power is need the **TX_lev<4:0>** option bits should be used. Sinusoidal or linear shape is defined by the option bit **lin_mod** in register *(15h)*. PR-ASK modulation is selected by setting the **pr_ask** option bit to high. In case PR-ASK is selected, the **del_len<5:0>** option bits are used to adjust the delimiter length in the range from 9.6 µs to 15.9 µs. For Tari = 25 µs PR-ASK and ASK delimiter shapes are available. The ASK transient which gives more accurate timing can be selected by the **ook_ask** option bit in register 15h. For Tari = 12.5 µs and 6.25 µs only the ASK delimiter shape is available. ASK modulation is selected by setting the **pr_ask** option bit to low. In ASK modulation it is possible to adjust the delimiter length by setting the option bit **ook_ask**. In this case, **ook_ask** defines 100% ASK modulation and the **del_len<5:0>** bits are used for delimiter length setting as in the PR-ASK mode described above. The rate of the modulation transient is automatically adjusted to the selected Tari setting and can be re-adjusted by the **ask_rate<1:0>** option bits (register 13h). For smoother transitions of the modulation signal an optional low pas filter can be activated by the **e_lpf** option bit in the Modulator Control Register 1 (13h). Bits **aux_mod** and **main_mod** define whether the modulation signal will be connected to the low power output or to the internal PA output path. In case one of the outputs is enabled by the **eTX<3:0>** bits in RF Output and LO Control Register (0Ch) and corresponding **aux_mod** or **main_mod** bit is low, the output is enabled but not modulated. With other words the device would output only a continuous wave signal.