# D350 THEORY OF OPERATION

# 1 INTRODUCTION

The VHF and UHF radios comprise of two PCBs, the RF and the digital PCB, connected via an 18-pin female and male connector. The digital board, which controls the radio functions and data inputs/outputs, is interfaced with external data equipment through the 15-pin d-type sub female (DB-15) connector.

# 2 DIGITAL CIRCUITS

The Digital circuit contains the CPU, the channel select switch, and associated digital circuits.

## 2.1 TX-SIGNAL CIRCUIT

There are different signal paths for the TX signal depending on user requirements

### Data Filter (pin 1)

The data signal from Pin 1 of DB-15 connector (CON401) goes through IC406-C. The signal is amplified by IC404-C and then its amplitude is limited by IC404-D. It is filtered by an 8th order low pass filter (IC405) to reduce the bandwidth. The first two stages of the 8th order LPF consist of a Gaussian filter for the improvement of ramp function response and the last two stages use a Butterworth filter for attenuation at higher frequencies. The output of the LPF is then fed to the RF board for TX modulation

### External modulation path with no data filter (pin 1)

This route is programmable and bypasses the data filter. It routed via an ac-coupled buffer, then directly to the RF.

### POCSAG route (pin 1)

This route uses the same circuitry as 2.1.2, but with modifications to make it compatible with TTL levels for POCSAG signals (TTL levels)

### DC coupled signal with no filtering (pin 1)

Link(LK430) changes route the signal directly to a voltage limiting circuit (diode and resistor added) then directly to the RF stage

### Voice (pin 7)

The audio signal, from Pin 7 is switched by IC409, through the 300Hz High pass filter, IC408, (removal of voice components below 300Hz allows SAT to added) to the audio filter with pre-emphasis. The signal is then fed to the data filter, IC405 as described in 1.1.1 above. The output of the LPF is fed to the RF board for modulation.

### Module option board route (pin 10)

From pin 10 the signal (RS232) is routed directly to the module option board, for processing, then to the MOD input of the RF.

## 2.2 RX-SIGNAL CIRCUIT

The Rx-signal circuit is split into several routes

### Data output (pin 2)

Data signals are switched through IC407-C by a 'busy' signal, which is activated when the radio receives a valid RF signal. It passes through a filter and amplitude level adjustment (IC416 A and B) to pin 2 of the DB-15 connector (CON401). The data route can be altered uses the available links in the data decoder

### Option Board Module Data Route (pin 11)

The option board module signal is routed via IC407C and the level shifter IC416C, to the option board.

For GMSK the dc level needs to be within specified limits for the GMSK chip to demodulate the signal. The decoded signal from the option board is routed directly to pin 11 of the DB-15 connector.

For FFSK or AFSK (Bell 202/V23) the signals can include SAT tones, so the signal is also routed via IC409 to the decode circuit as described below.

### Speech (pin 9)

Audio voice signals are switched through the analogue switch (IC409) to the 300Hz High pass filter (IC408) to eliminate the sub-audible tones (CTCSS/DCS). The output of the HPF is switched through IC418 (disabled if data is enabled) and IC406-A. The voice signal is then de-emphasized by R471 and C452 and amplified by IC412 (LM386 – Audio Amplifier), with the level adjusted by RV401. The amplified signal goes to pin 9 of CON401 (DB-15).

## 2.3 ANALOGUE SWITCH

IC409 (74HC4053B) is a digitally controlled analogue switch, which consists of three single pole double throw switches. Placing a high (5V) or low (0V) on the control lines switches the ports. A controls the X ports, B controls the Y ports and C controls the Z ports. This switch ensures the same filtering can be used for both TX and RX signals were appropriate.

## 2.4 HIGH PASS FILTER

The 300Hz high pass filter is an 8-pole 1dB Chebeyshev active filter that comprises of IC410 and associated components. Received audio is passed to IC408 from Pin 4 of IC409 where sub-audible tones below 300Hz are removed. TX (Mic) audio is also fed into IC408 via IC 409 (Pin 4) where sub-audible voice products below 300Hz are also removed.

## 2.5 Sub Audible Tone Circuits *

### 2.5.1 CTCSS/DCS DECODE CIRCUITS

Discriminated audio from Pin 9 of IC6 (on RF board) is fed into a 6th order Chebeyshev 250Hz low pass filter (IC411-B and associated components form the first 2 poles). The output is fed through the analogue switch, IC409, to IC410 (pin 8), which is a 6th order low pass Butterworth switched capacitor filter. The output from the Butterworth filter (Pin 3 of IC410) is then fed to the remaining second 4

poles part of the 6th order Chebeyshev filter (IC411-D, one of IC410's internal operational amps and associated components. The combination of filters gives a 4dB ripple low pass filter when programmed for 250 Hz. The remaining internal operational amplifier of IC410 forms the squaring circuit. This signal is compared the pre-programmed CTCSS/DCS of the MPU (via pin 32). If matched then valid data is decoded and the audio enable lines go high (pin 48 of microcontroller), along with LED401, lighting the green LED. Audio is released through pin 9 of DB-15 Connector. If unmatched, the busy L.E.D. (orange) is lit.

### 2.5.2 CTCSS/DCS ENCODE CIRCUITS

The SAT squelch signal is produced as a 3-bit parallel word at Pins 19, 20, and 21 of the micro controller (IC401). This is converted to an analogue signal by resistors R481, R482 and R483 and fed through the analogue switch (IC409) into the 6th order Butterworth clock tuned low pass filter (pin 8 of IC410)). The filtered encode output (Pin 3 of IC410) is fed to the sub-audible gain control circuit (IC411-A and RV402) and then fed to the audio mixer circuit of the RF board.

## 2.6 TWO TONE DECODE CIRCUITS

Two tone uses frequency with audio. Discriminated audio from the RF board is inputted to the comparator (two tone decoder: IC403-B) which forms the squaring circuit for the decode signal. The signal is output from Pin 7 of IC403-B and fed into IC401 (MCU) where it is compared whether it is matched with pre-programmed data or not. If matched valid data is decoded, which is shown by a green L.E.D. on the top panel of the radio and audio is released through pin 9 of the DB-15 Connector. If unmatched, the busy L.E.D. (Orange) is shown.

## 2.7 RSSI DETECTOR

From the RF board, the RSSI (Received Signal Strength Indicator) signal is input on Pin 16 of IC401 (MCU) through R513. The microcontroller unit (IC401) detects received signal level using the inner 8-bit ADC (Analogue to Digital Converter). The output of ADC is compared with the programmed RSSI level. If the MCU detects existence of a received signal from this comparison the orange L.E.D (busy).

## 2.8 EEPROM

RX / TX channel data and RSSI detection level as well as other data from the programmer are stored in the EEPROM. The stored data is non-volatile and is re-programmable. IC402 is an EEPROM with 4096 (8 x 512) capacity with the data being written and read serially.

## 2.9 CHANNEL SELECTOR

One of 16 channels may be selected either using the Dip Switch (SW401) or by using the appropriate serial command. It is also possible, using links LK440-LK443 for TTL inputs to select the channels (pins 15, 13,12,11 of the DB-15 connector), though the number channels available would be limited if using an internal option board. The same pins are used for the GPS module and for option board, serial out and busy are used.

The hardware selector, SW401 encodes the channel number, selected into 4-bit binary code. The binary code plus one equals the channel number. The binary code is decoded by the microcontroller, which enables the appropriate RX or TX frequency and associated data to be selected from the EEPROM. External serial

commands which are routed via Pin 8 of the DB-15 Connector (CON401) are fed into Pin 31 of IC401 (the MCU). The microcontroller uses UART for serial communication and decodes the serial commands in order to control the radio.

## 2.10 DC TO DC CONVERTER (STEP DOWN)

The main DC power is supplied to the switched mode DC-to-DC converter. The DC-to-DC converter regulates the varying input power supply voltage (9-18V) and outputs a constant voltage of 7.5 Volts. It is a source for all of the RF and digital circuits. The DC-to-DC converter is formed by IC801, IC802 and voltage divider (R802, R805). IC801 detects the voltage difference between the inner reference voltage and the divider output – the error amplifier. This error amplifier output is compared with the oscillator sawtooth to perform PWM control. The voltage output is feedback via the divider to the IC801 (and to IC802)

To save power when the modem is not in constant use, a serial command can be used to put the modem into a sleep mode. This involves the microprocessor deactivating IC802, so switching off most of the modem. The microprocessor itself needs to remain awake, so that it is able to receive a serial command to switch on IC802 and the rest of the circuitry.

# 3 RF CIRCUITS

## 3.1 PLL SYNTHESIZER

### 3.1.1 12.8 MHz TCXO

The VCTCXO contains the thermistor network compensation and crystal oscillator and modulation ports. The accuracy is ±5 PPM or less from -30c to +60c.

### 3.1.2 PLL IC DUAL MODULE PRESCALER

The PLL IC (IC2) is a MB15A02 for VHF and MB15A03SL for UHF. The input frequency of 12.8 MHz to the PLL frequency synthesizer (pin 1 of IC2) is divided into 6.25 kHz or 5 kHz by the reference counter and then supplied to the comparator. The RF signal input from the VCO is divided to 1/64 at the 64/65 modulus prescaler, then divided by the A and N counter to determine frequency steps. It is then supplied to the comparator, which compares the phase difference between reference and VCO signal. When the phase of the reference frequency is leading, ΦP is the output, but when the VCO frequency is leading, ΦR is the output. When ΦP= ΦR, phase detector out is a very small pulse.
The PLL comparison frequency is 6.25/5 kHz, so its minimum programmable frequency step is 6.25/5 kHz. The A and N counter is programmed to obtain the desired frequency by serial data in the CPU.
The lock detector produces a series of logic level pulses, when the loop is out of lock, at pin 7 of IC2 (VHF) and pin 14 of IC2 (UHF). The pulses are buffered by Q7 and integrated by R16 and C10 on the VHF circuit. The resultant voltage is fed to the micro controller.

### 3.1.3 EXTERNAL CHARGE PUMP

This is used to increase the dynamic range of VCO. The voltage range is dictated by the supply voltage of the charge pump, which is derived from the DC-to-DC converter, which, in turn, takes it supply from the regulated 7.5 volts from the control board. A voltage range of up to 12v is necessary for controlling the VCO. In addition the radio adopts a current mode charge pump to take direct control of such parameters as charge pump voltage swing, current magnitude, TRI-STATE leakage, and temperature compensation. ΦP, ΦR logic signals are converted into current pulses to enable either charging or discharging of the loop filter components to control the output frequency of the PLL.

### 3.1.4 REFERENCE FREQUENCY LPF

The Loop Filter contains R9, C1 and C2. The filter's settling time is 12mS with 1 kHz frequency. This filter also reduces the residual side-band noise for the best signal-to-noise ratio.

### 3.1.5 DC TO DC CONVERTER (STEP UP)

The DC-to-DC converter converts 7.5V to 14-16v to supply the necessary voltage for wide frequency range in the VCO.
Q901, Q902 and associated components form a 200kHz oscillator. The output of this oscillator is rectified (voltage doubled) by D901 and D902. C908 and C909 provide the filtering. The resultant voltage is passed through R12 to become the supply rail for the charge pump.

### 3.1.6 VCO

The radio adopts a two VCO system for TX and RX, both based on a similar theory of operation, but with additional circuitry for the TX VCO for the modulation path. The UHF VCOs are activated by control enable lines (originating from the microprocessor) switching power through Q20 (TX) and Q26 (RX). The VHF VCOs are switched by applying power Q8 (TX) and Q20 (RX). This power is derived from switching transistors Q1 and Q2 with the logic control lines, TX enable and Rx enable originating from the micro controller.
The UHF and VHF VCOs are configured as Colpitts oscillators using transistors Q202 (TX) / Q302 (Rx), varicap diodes D201(TX) / D301 (RX) and frequency setting inductors L203, L204 for TX and L302, L304 for RX with associated components. The varicap diodes are low-resistance elements, which have different capacitance depending on the reverse bias voltage. The required frequency is obtained by changing the reverse bias voltage (2 ~ 11V). C208 and C308 are used to change the control voltage by the tuning core. Cascade bias is provided by Q201 / Q301.
The modulation diode, D202, modulates the audio signal. C205 compensates the non-linearity of the VCO due to this modulation diode and maintains a constant modulation regardless of frequency.

## 3.2 TRANSMITTER

The transmitter consists of:
1. Buffer
2. P.A. Module
3. Low Pass Filter
4. Antenna Switch
5. A.P.C. Circuits

### 3.2.1 BUFFER

VCO output level is -4dBm and amplified to +10dBm. The buffer consists of Q9 and Q10 for reverse isolation and gain.

### 3.2.2 P.A. BLOCK

The P.A. Block uses a three-stage amplifier and contains Q701, Q702, and Q703. Q701 amplifies the TX signal from +10 dBm to 100mW and Q702 amplifies to 0.5W and Q703 amplifies to 6W and then matched to 50 Ohms using the L.C. network or strip line, thereby reducing the harmonics by -30 dB.

### 3.2.3 LOW PASS FILTER

L7, L8, L9, C36, C37, C38 and C39 form the 7th order Chebyshev low pass filter. Unwanted harmonics are reduced by -70 dBc.

### 3.2.4 ANTENNA SWITCH

When transmitting, the diodes D3 and D5 are forward biased to enable the RF path to be routed to the antenna. This results in D5 being shorted to ground to block the RF signal to the front-end. In receive, the diodes, D3 and D5, are reverse biased to pass the signal from the antenna through L10 and C61 to the front-end without signal loss.

### 3.2.5 AUTOMATIC POWER CONTROL (APC) CIRCUITS

The APC circuit consists of R63, variable resistor RV4, IC5, transistors Q15, Q11 and Q12 and associated components. The supplied current to the P.A. block is monitored by the voltage difference on R63 (0.1 Ohm). If the current varies due to RF power output variations or other reasons, it produces a voltage difference on R63 and then IC5A outputs a bias voltage to Q15 in proportion to that difference. The level is adjusted by RV4 (high power) and is compared with the reference voltage in IC5B. A differential voltage at the output of IC5B is passed to Q12 and Q11, which controls the bias voltage of the P.A. module, so ensuring a constant power output to the antenna. The power level (high/low) is selected via Q13, taking the control line from the micro controller. When the control line is high, Q13 is switched on, so adding parallel resistance to R54. This reduces overall resistance to ground, so reducing the voltage level at pin 5 of IC5-B. This reduces the differential voltage, so driving less current through Q12 and Q11 to the P.A.

## 3.3 RECEIVER

### 3.3.1 ANTENNA SWITCH

In receive, the diodes D3 and D5 are reverse biased. The signal is routed via L10 from the antenna to the front end.

### 3.3.2 FRONT-END

The front-end block consists of two band pass filters either side of a low noise amplifier (LNA), Q601. The band pass filter is used for elimination of image frequency and impedance matching. The LNA is used to amplify weak RF

signals without any increase of noise. Diode D601 serves as protection from static RF overload from nearby transmitters. The output of the front-end block is then coupled to the double balanced diode mixer D6. The Front-end block is pre-tuned at factory and no further adjustment is required

### 3.3.3 FIRST MIXER

The Double balanced diode mixer consists of D6, T1 and T2 and generates the 45.1 MHz intermediate frequency output from RF and local frequency oscillator. The filtered frequency from the front-end module is coupled to T1and the local frequency from RX VCO is coupled to T2. The 45.1 MHz IF output is matched with the input of the 2-pole monolithic filter by L12, L13, C65 and C66. The crystal filter provides a bandwidth of ±7.5 kHz at the operating frequency for a high degree of spurious and inter-modulation protection. The IF filter provides additional attenuation for the image frequency. The output impedance of the filter is matched with the base of the post amplifier, Q16 by C67 and C70.

### 3.3.4 SECOND OSCILLATOR MIXER LIMITER AND FM DETECTOR

The output of the post amplifier, Q16, is coupled via C71 to the input of the monolithic single conversion FM IF detector (IC6). The FM detector contains a mixer, the second local oscillator, a limiter and quadrature detector. The crystal X1, 44.645 MHz, is used to provide resultant 455kHz signal from the output of the second mixer. The mixer output is then routed to the ceramic filters CF1/CF3 (455KE1Y/FA) or CF2/CF4 (455KG1Y/FA), which provide adjacent channel selectivity of 25 kHz or 12.5 kHz bandwidth respectively. The filtered signal is fed back to IC6 at pin 5 into the limiter stage, with the audio being derived at the quadrature detector. AF output is on pin 9

### 3.3.5 RSSI (RECEIVER SIGNAL STRENGTH INDICATOR)

The RSSI signal is taken from the FM detector on pin 12 and is used in the programmable squelch system. It is an analogue DC voltage and varies in accordance with the received signal strength. The RSSI signal is filtered (LPF – IC4D) to eliminate unwanted noise and is compensated with a thermistor (TH4) at temperature.

### 3.3.6 Noise Squelch

The hardware squelch circuitry uses the output on pin 9 via RV5 and RV6 (adjustments dependant on channel spacing) to produce inputs on pins 7&8 of the FM detector. This enables an output on the noise detect on pin 13. This is routed via Q24 to the Digital board. The programmer dictates the form of squelch to be used, whether the hardware squelch circuitry (busy port) or the RSSI level check.