



FSC-BT1026x

(BT1026C/BT1026D) 5.0 Dual Mode Bluetooth Module Datasheet

(BT1026A/BT1026B) 5.1 Dual Mode Bluetooth Module Datasheet

Version 1.0

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Revision History

Version	Date	Notes	
1.0	2020/09/15	Initial Version	Fish

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1. INTRODUCTION

Overview

FSC-BT1026x it is a Bluetooth dual-mode module. It supports a Bluetooth Low Energy and compliant system for audio and data communication.

FSC-BT1026x integrates an ultra-low-power DSP and application processor with embedded flash memory, a high-performance stereo codec, a power management subsystem, I2S, LED drivers and ADC I/O in a SOC IC.

Both cores use external flash to execute code, making it easy for user to differentiate products from new features without delaying the development

By default, FSC-BT1026x module is equipped with powerful and easy-to-use Feasycom firmware. It's easy to use and completely encapsulated. Feasycom firmware enables users to access Bluetooth functionality with simple ASCII commands delivered to the module over serial interface - it's just like a Bluetooth modem.

Therefore, FSC-BT1026x provides an ideal solution for developers who want to integrate Bluetooth wireless technology into their design.

Features

- Qualified to Bluetooth® v5.1 specification (Support FSC-BT1026A、FSC-1026B)
- Qualified to Bluetooth® v5.0 specification (Support FSC-BT1026C、FSC-1026D)
- 120 MHz Qualcomm® Kalimba™ audio DSPs
- 32 MHz Developer Processor for applications
- Firmware Processor for system
- Flexible QSPI flash programmable platform
- Advanced audio algorithms
- High-performance 24-bit stereo audio interface
- Digital and analog microphone interfaces
- aptX, aptX HD, aptX Low Latency (Support

FSC-BT1026B、FSC-1026D)

- SBC and AAC audio codecs support
- Serial interfaces: UART, Bit Serializer (I²C/SPI),USB 2.0
- Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger

Application subsystem

- Dual core application subsystem 32 MHz operation
- 32-bit Firmware Processor:
 - Reserved for system use
 - Runs Bluetooth upper stack, profiles, house-keeping code
- 32-bit Developer Processor:
 - Runs developer applications
- Both cores execute code from external flash memory using QSPI clocked at 32MHz
- On-chip caches per core allow for optimized performance and power consumption

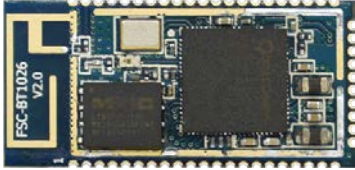
Bluetooth subsystem

- Qualified to Bluetooth v5.1/v5.0 specification including 2 Mbps Bluetooth low energy(Production parts)
- Single ended antenna connection with on-chip balun and Tx/Rx switch
- Bluetooth, Bluetooth low energy, and mixed topologies supported
- Class 1 support

Application

- Bluetooth speakers
- Bluetooth music box
- Wired/wireless stereo headsets/headphones
- USB audio/USB to Bluetooth dongle

1.1 Selection of version

Order Number	Descriptions	Module picture as below showing
FSC-BT1026A	Chip: QCC3021 Bluetooth: V5.1	
FSC-BT1026B	Chip: QCC3031 Bluetooth: V5.1 Support: aptX	
FSC-BT1026C	Chip: QCC3024 Bluetooth: V5.0	
FSC-BT1026D	Chip: QCC3034 Bluetooth: V5.0 Support: aptX	

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Chip	QCC3021 (FSC-BT1026A) QCC3031 (FSC-BT1026B) QCC3024 (FSC-BT1026C) QCC3031 (FSC-BT1026D)
	Bluetooth Version	V5.1 Dual-mode (FSC-BT1026A/FSC-BT1026B) V5.0 Dual-mode (FSC-BT1026C/FSC-BT1026D)
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+9 dBm (Maximum)
	Receive Sensitivity	-96.0 dBm (typ.) $\pi/4$ DQPSK receiver sensitivity -89.0 dBm (typ.) 8DPSK receiver sensitivity -100 dBm (typ.) BLE 1 Ms/s receiver sensitivity Real-time digitised RSSI available to application
	Raw Data Rates (Air)	3 Mbps(Classic BT - BR/EDR)
	Host Interface and Peripherals	TX, RX, CTS, RTS General Purpose I/O Default 115200,N,8,1

		Baudrate support from 1200 to 4000000
		5,6,7,8 data bit character
GPIO		17(maximum – configurable) lines
		O/P drive strength (2,4 ,8,or12mA)
		Pull-up resistor (33 KΩ) control
I ² C Interface		1 (hardware I ² C interface). Up to 400 kbps
		Master and slave I ² C interface
SPI Interface		SPI debug and programming interface with read access disable locking
ADC Interface		Analog input voltage range: 0~ 1.854V
		Supports single a 10-bit ADC
		1 channels (configured from GPIO total)
USB Interface		1 full-speed (12Mbps)
Audio CODEC		aptX, aptX HD, aptX Low Latency, SBC and AAC audio codecs
		Configurable Signal Detection to trigger events
		1 bank of up to 10-stage Speaker Parametric EQ
		6 banks of up to 5-stage User Parametric EQ for music enhancement
		Companer to compress or expand the dynamic range of the audio
		Post Mastering to improve DAC fidelity
		I ² S/PCM outputs with crossover
		USB audio
		Stereo audio ADC with line input, stereo audio DAC
		Supported sample rates of 8, 16, 32, 44.1, 48 and 96 kHz,192kHz(Input)
		MIC SNR: 92 dB
		MIC THD+N: 0.004%
		Headphone SNR: 101dBA typ
		Headphone THD+N: -90.5 typ
		Headphone Output Power: 30mW (0dBFS 32Ω load)
		Stereo separation (crosstalk): -80dB(Min)
Profiles	BR/EDR	SPP (Serial Port Profile) - Up to 600 Kbps
		A2DP/AVRCP/HFP/HSP/HOGP/PBAP/SPP Profiles support
	Bluetooth Low Energy	GATT Client & Peripheral -Any Custom Services
		Simultaneous BR/EDR and BLE support
Maximum Connections	BR/EDR	up to 7 active slaves
	Bluetooth Low Energy	1 connection as peripheral , up to 5 connections as central
FW upgrade		Via UART(TBD)
		USB(TBD)
		OTA
		SPI
Supply Voltage	Supply	VDD_IO: 1.7 ~ 3.3V; VBAT_IN: 2.8V~ 4.3V
Power Consumption		Max Peak Current(TX Power @ +8dBm TX): 78mA
		Standby Doze (Wait event) - 15mA (TBD)
		Deep Sleep - <1mA(TBD)
Physical	Dimensions	13mm(W) X 26.9mm(L) X 2.2mm(H); Pad Pitch 1mm

Environmental	Operating	-40°C to +85°C
	Storage	-40°C to +85°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity	10% ~ 90% non-condensing	
MSL grade:	MSL 3	
ESD grade:	Human Body Model: Class 2	2kV (all pins)
	Charged Device Model: Class III	500 V (all pins)

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

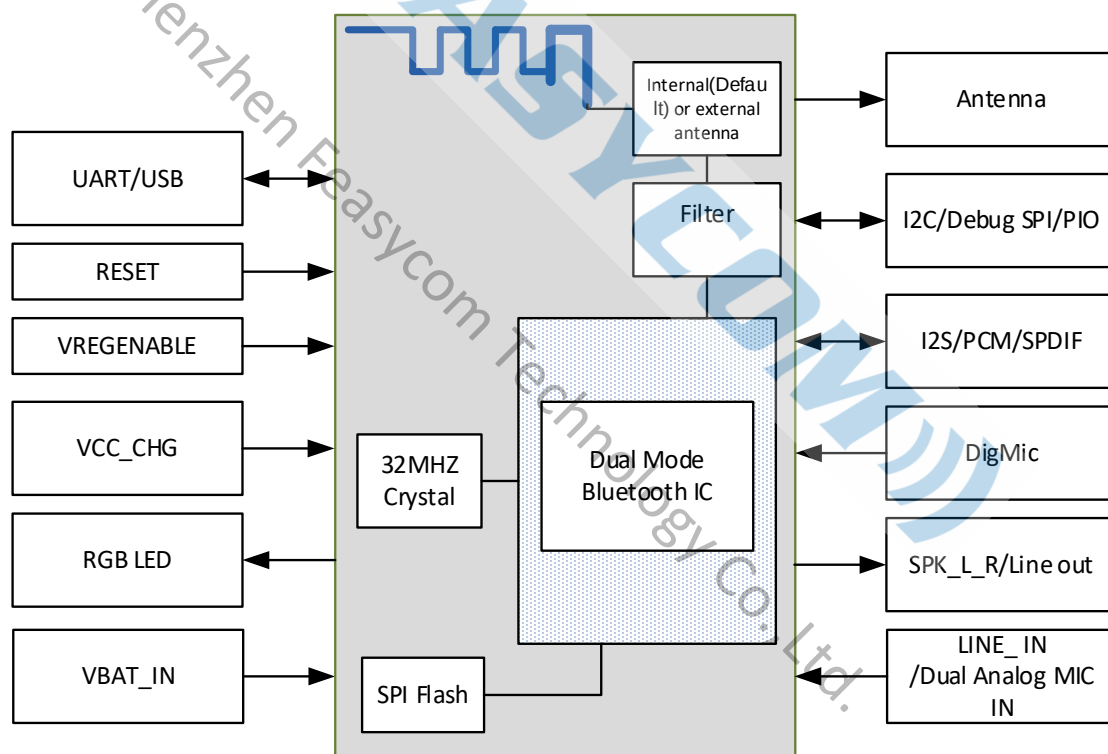


Figure 2: Block Diagram

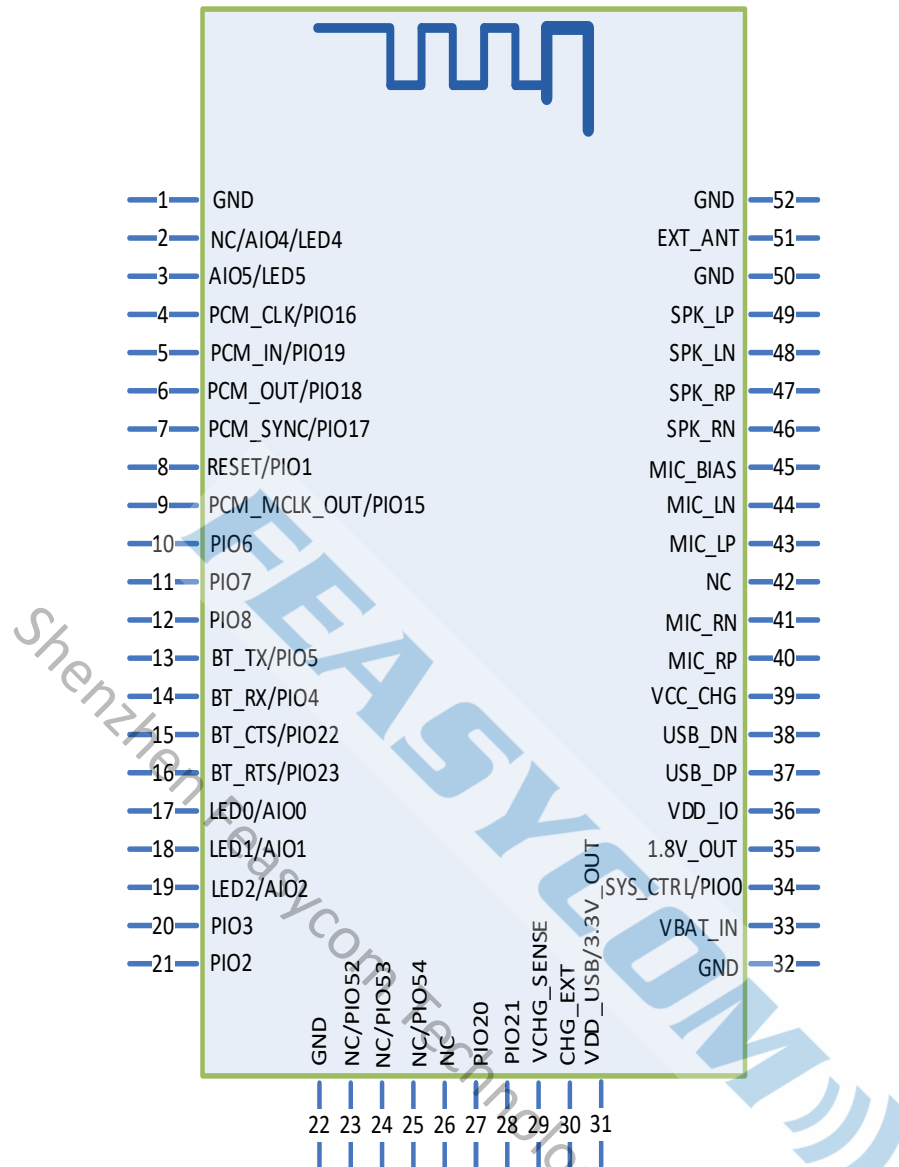


Figure 3: FSC-BT1026x PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	Vss	Power Ground	
2	NC/AIO4/LED4	A,I/O	NC (For FSC-BT1026A、FSC-BT1026B) General-purpose analog/digital input or open drain LED output. (For FSC-BT1026C、FSC-BT1026D)	
3	AIO5/LED5	A,I/O	General-purpose analog/digital input or open drain LED output.	Note 8
4	PCM_CLK/PIO16	I/O	Programmable I/O line 16. Alternative function: PCM_CLK	Note 6
5	PCM_IN/PIO19	I/O	Programmable I/O line 19. Alternative function: PCM_DIN[0]	Note 6

6	PCM_OUT/PIO18	I/O	Programmable I/O line 18. Alternative function: PCM_DOUT[0]	Note 6
7	PCM_SYNC/PIO17	I/O	Programmable I/O line 17. Alternative function: PCM_SYNC	Note 6
8	RESET/PIO1	I/O	Automatically defaults to RESET# mode when the device is unpowered, or in off modes. Reconfigurable as a PIO after boot. Alternative function: Programmable I/O line 1	
9	PCM_MCLK_OUT/PIO15	I/O	Programmable I/O line 15. Alternative function: MCLK_OUT	
10	PIO6	I/O	Programmable I/O line 6. Alternative function: TBR_MOSI[0]	
11	PIO7	I/O	Programmable I/O line 7. Alternative function: TBR_MISO[0]	
12	PIO8	I/O	Programmable I/O line 8. Alternative function: TBR_CLK	
13	BT_TX/PIO5	I/O	BT_TX /Programmable I/O line 5. Alternative function: TBR_MISO[1]	Note 6
14	BT_RX/PIO4	I/O	BT_RX/Programmable I/O line 4. Alternative function: TBR_MOSI[1]	Note 6
15	BT_CTS/PIO22	I/O	BT_CTS/Programmable I/O line 22.	Note 6
16	BT_RTS/PIO23	I/O	BT_RTS/Programmable I/O line 23.	Note 6
17	AIO0/LED0	A,I/O	General-purpose analog/digital input or open drain LED output.	Note 6,8
18	AIO1/LED1	A,I/O	General-purpose analog/digital input or open drain LED output.	Note 6,8
19	AIO2/LED2	A,I/O	General-purpose analog/digital input or open drain LED output.	Note 6,8
20	PIO3	I/O	Programmable I/O line 3. Alternative function: TBR_MISO[2]	
21	PIO2	I/O	Programmable I/O line 2. Alternative function: TBR_MISO[3]	
22	GND	Vss	Power Ground	
23	NC/PIO52	I/O	NC (For FSC-BT1026A、FSC-BT1026B) Programmable I/O line 52 (For FSC-BT1026C、FSC-BT1026D)	
24	NC/PIO53	I/O	NC (For FSC-BT1026A、FSC-BT1026B) Programmable I/O line 53 (For FSC-BT1026C、FSC-BT1026D)	
25	NC/PIO54	I/O	NC (For FSC-BT1026A、FSC-BT1026B) Programmable I/O line 54 (For FSC-BT1026C、FSC-BT1026D)	
26	NC			
27	PIO20	I/O	Programmable I/O line 20. Alternative function: PCM_DOUT[1]	Note 5
28	PIO21	I/O	Programmable I/O line 21. Alternative function: PCM_DOUT[2]	Note 5

29	VCHG_SENSE		Charger input sense pin after external mode sense-resistor. High impedance. NOTE: If using internal charger or no charger, connect VCHG_SENSE direct to VCHG.	
30	CHG_EXT		External charger transistor current control. Connect to base of external charger transistor as per application schematic.	
31	VDD_USB/3.3V_OUT		3.3V voltage INPUT/output(MAX. 50mA OUT)	Note 7
32	GND	Vss	Power Ground	
33	VBAT_IN	Vdd	Battery voltage input.	
34	SYS_CTRL/PIO0	I	Typically connected to an ON/OFF push button. Boots device in response to a button press when power is still present from battery and/or charger but software has placed the device in the OFF or DORMANT state. Additionally useable as a digital input in normal operation. No pull. Additional function: PIO[0] input only	Note 3
35	1.8V_OUT	Vdd	1.8V voltage output	Note 1
36	VDD_IO	I	PIO supply(1.8 V~3.3V)	Note 2
37	USB_DP		USB Full Speed device D+ I/O. IEC-61000-4-2 (device level) ESD Protection	Note 4
38	USB_DN		USB Full Speed device D- I/O. IEC-61000-4-2 (device level) ESD Protection	Note 4
39	VCC_CHG	Vdd	Charger input to Bypass regulator.	Note 4
40	MIC_RP	A	Microphone differential 2 input, positive. Alternative function: Differential audio line input right, positive	
41	MIC_RN	A	Microphone differential 2 input, negative. Alternative function: Differential audio line input right, negative	
42	NC			
43	MIC_LP	A	Microphone differential 1 input, positive. Alternative function: Differential audio line input left, positive	
44	MIC_LN	A	Microphone differential 1 input, negative. Alternative function: Differential audio line input left, negative	
45	MIC_BIAS	Vdd	Mic bias output.	
46	AUDIO_HPR_N/ SPK_RN	A	Headphone/speaker differential right output, negative. Alternative function: Differential right line output, negative	
47	AUDIO_HPR_P/ SPK_RP	A	Headphone/speaker differential right output, positive. Alternative function: Differential right line output, positive	
48	AUDIO_HPL_N/ SPK_LN	A	Headphone/speaker differential left output, negative. Alternative function: Differential left line output, negative	
49	AUDIO_HPL_P/ SPK_LP	A	Headphone/speaker differential left output, positive.	

Alternative function: Differential left line output, positive

50	GND	Vss	Power Ground	
51	RF_OUT	RF	Bluetooth transmit/receive.	Note 9
52	GND	Vss	Power Ground	

Module Pin Notes:

Note 1	The internal output of 1.8 V power supply provides maximum 30mA current, and the specific use method can see the application circuit diagram
Note 2	Provide voltage reference to I/O, such as: PIO, UART, SPI, I2S, PCM, etc
Note 3	Regulator enable input. Can also be sensed as an input. Regulator enable and multifunction button. A high input (tolerant to VBAT) enables the on-chip regulators, which can then be latched on internally and the button used as a multifunction input. * The PIN on electricity than VBAT_IN and VDD_IO foot 100 ms delay.
Note 4	Using USB function and Lithium battery charging function, the pin should connect 5V voltage
Note 5	1, Alternate I ² C function 2, I ² C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 6	For customized module, this pin can be work as I/O Interface.
Note 7	1, When you need to use the USB function, this pin needs to be connected to 3.3V (voltage range: 3.1V~3.6V) 2, when the No. 39 PIN (VCC_CHG) with a 5V input pin, this pin outputs 3.2V ~ 3.4V (maximum current: 50mA)
Note 8	Analog input voltage range: 0~ 1.8V
Note 9	By default, this PIN is an empty foot. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the OR resistance to block out the on-board antenna; Or contact Feasycom for modification.

4. PHYSICAL INTERFACE

4.1 Power Management

4.1.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.1.2 Battery Charger

4.1.2.1 Battery Charger Hardware Operating Modes

The default mode for the FSC-BT1026x battery charger is OFF.

The internal charger circuit can provide up to 200mA of charge current.

The battery charger hardware is controlled by the on-chip application. The battery charger has 5 modes:

- Disabled
- Trickle charge
- Fast charge
- Standby: fully charged or float charge
- Error: charging input voltage, VCHG, is too low

The battery charger operating mode is determined by the battery voltage and current, see the table below and the picture below.

Table 3: Battery Charger Operating Modes Determined by Battery Voltage and Current

Parameter	Battery Charger Enabled	VBAT_SENSE(internal)
Off	No	X
Trickle charge	Yes	>0 and $<V_{fast}$
Fast charge	Yes	$>V_{fast}$ and $<V_{float}$
Standby	Yes	$I_{term}^{(a)}$ and $>(V_{float} - V_{hyst})$
Error	Yes	$>(VCC_CHG - 50mV)$
(a) I_{term} is approximately 10% of I_{fast} for a given I_{fast} setting		

The picture below shows the mode-to-mode transition voltages. These voltages are fixed and calibrated. The transition between modes can occur at any time.

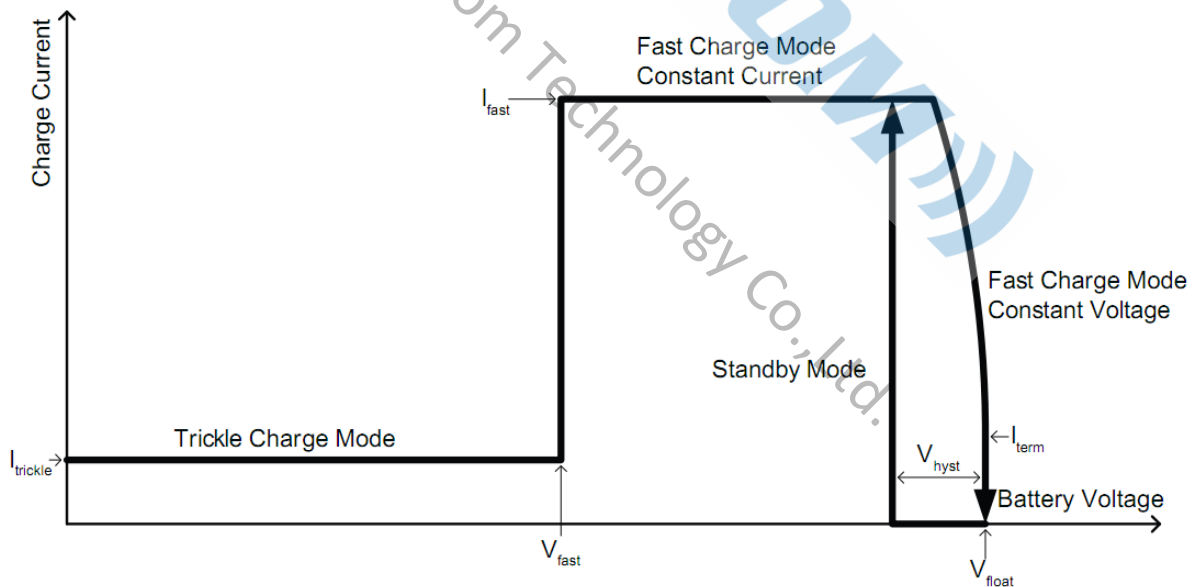


Figure 4: Battery Charger Mode-to-Mode Transition Diagram

Disabled Mode

In the disabled mode the battery charger is fully disabled and draws no active current on any of its terminals.

Trickle Charge Mode

In the trickle charge mode, when the voltage on VBAT_SENSE is lower than the V_{fast} threshold, a current of approximately 10% of the fast charge current, I_{fast} , is sourced from the VBAT_IN pin.

The V_{fast} threshold detection has hysteresis to prevent the charger from oscillating between modes.

Fast Charge Mode

When the voltage on VBAT_SENSE is greater than V_{fast} , the current sourced from the VBAT pin increases to I_{fast} . I_{fast} is between 10mA and 200mA set by PS Key or a VM trap. In addition, I_{fast} is calibrated in production test to correct for process variation in the charger circuit.

The current is held constant at I_{fast} until the voltage at VBAT_SENSE reaches V_{float} , then the charger reduces the current sourced to maintain a constant voltage on the VBAT_SENSE pin.

When the current sourced is below the termination current, I_{term} , the charging stops and the charger enters standby mode. I_{term} is typically 10% of the fast charge current.

Standby Mode

When the battery is fully charged, the charger enters standby mode, and battery charging stops. The battery voltage on the VBAT_SENSE pin is monitored, and when it drops below a threshold set at V_{hyst} below the final charging voltage, V_{float} , the charger re-enters fast charge mode.

Error Mode

The charger enters the error mode if the voltage on the VCC_CHG pin is too low to operate the charger correctly (VBAT_SENSE is greater than VCC_CHG - 50mV (typical)).

In this mode, charging is stopped. The battery charger does not require a reset to resume normal operation.

4.1.2.2 Battery Charger Trimming and Calibration

The battery charger default trim values are written by Feasycom into non-volatile memory when each IC is produced. Feasycom provides various PS Keys for overriding the default trims.

4.1.2.3 On-chip application Battery Charger Control

The on-chip application charger code has overall supervisory control of the battery charger and is responsible for:

- Responding to charger power connection/disconnection events
- Monitoring the temperature of the battery
- Monitoring the temperature of the die to protect against silicon damage
- Monitoring the time spent in the various charge states
- Enabling/disabling the charger circuitry based on the monitored information

- Driving the user visible charger status LED(s)

4.1.2.4 Battery Charger Firmware and PS Keys

The battery charger firmware sets up the charger hardware based on the PS Key settings and call traps from the VM charger code. It also performs the initial analogue trimming. Settings for the charger current depend on the battery capacity and type, which are set by the user in the PS Keys.

4.2 Reset

FSC-BT1026x is reset from several sources:

- Power-on reset
- USB charger attach reset
- Software configured watchdog timer

At reset, the digital I/O pins are set to inputs, bidirectional pins and outputs are set to tristate.

NOTE: Reset can also be triggered by a UART break symbol if:

- Host interface is any UART transport
And
- PSKEY_HOSTIO_UART_RESET_TIMEOUT is set to a value more than 1000
A reboot function is also available under software control.

4.3 General Purpose Analog IO

FSC-BT1026x has 1 general-purpose analogue interface pins, AIO0. Typically, this pin connects to a thermistor for battery pack temperature measurements during charging.

4.4 General Purpose Digital IO

FSC-BT1026x provides up to 20 lines of programmable bidirectional I/O.

4.5 RF Interface

For this module, the antenna must be connected to work properly.

The user can connect a 50ohm antenna directly to the RF port.

- 2402–2480 MHz Bluetooth 5.1 Dual Mode (BT and BLE); 1 Mbps to 3 Mbps over the air data rate.
- TX output power of +9dBm (MAX).
- Receiver to achieve best sensitivity -100dBm for BLE and -97dBm for Classic Bluetooth.

4.6 Serial Interfaces

4.6.1 UART Interface

FSC-BT1026x provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT1026x deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

Table 4: Possible UART Settings

Parameter	Possible Values
Baudrate	Minimum 2400 baud ($\leq 2\%$ Error)
	Standard 19200bps($\leq 1\%$ Error)
	Maximum 4Mbaud($\leq 1\%$ Error)
Flow control	RTS/CTS, or None
Parity	None, Odd or Even
Number of stop bits	1 / 2
Bits per channel	8

When connecting the module to a host, please make sure to follow .

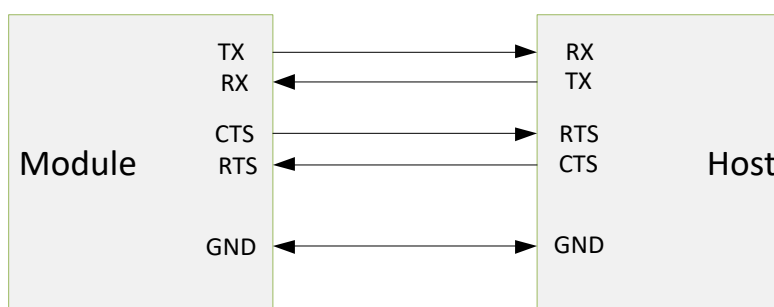


Figure 5: UART Connection

The UART interface resets FSC-BT1026x on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as below picture shows. If t_{BRK} is longer than the value defined by the PSKEY_HOSTIO_UART_RESET_TIMEOUT, a reset occurs. This feature enables a host to initialise the system to a known state. Also, FSC-BT1026x can issue a break character for waking the host.



Figure 6: Break Signal

The UART interface is tristate while FSC-BT1026x is being held in reset. This enables the user to connect other devices onto the physical UART bus. The restriction with this method is that any devices connected to this bus must tristate when FSC-BT1026x reset is de-asserted and the firmware begins to run.

4.6.2 I²C Interface

FSC-BT1026x includes a configurable I²C interface.

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I²C Bus Timing.

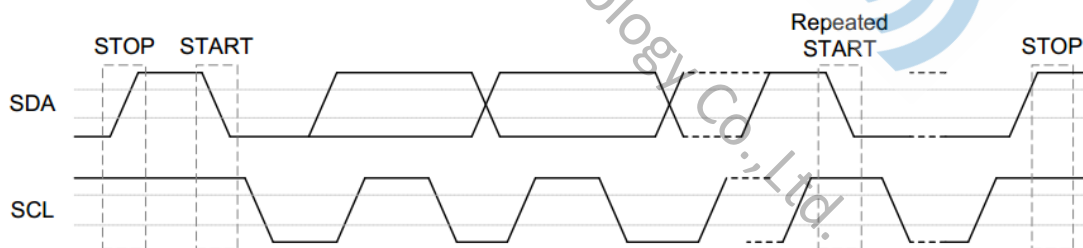


Figure 7: I2C Bus Timing

The device on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C H/W interfaces to the I²C bus via two pins: SDA and SCL. Pull up resistor is needed for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

4.6.3 USB Interface

FSC-BT1026x has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB interface on FSC-BT1026x acts as a USB peripheral, responding to requests from a master host controller.

FSC-BT1026x supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification) and USB Battery Charging Specification, available from <http://www.usb.org>. For more information on how to integrate the USB interface on FSC-BT1026x see the Bluetooth and USB Design Considerations Application Note.

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring (when VBUS is > 3.1)
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend support
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

4.7 LED Drivers

FSC-BT1026x includes a 3-pad synchronised PWM LED driver for driving RGB LEDs for producing a wide range of colors. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.

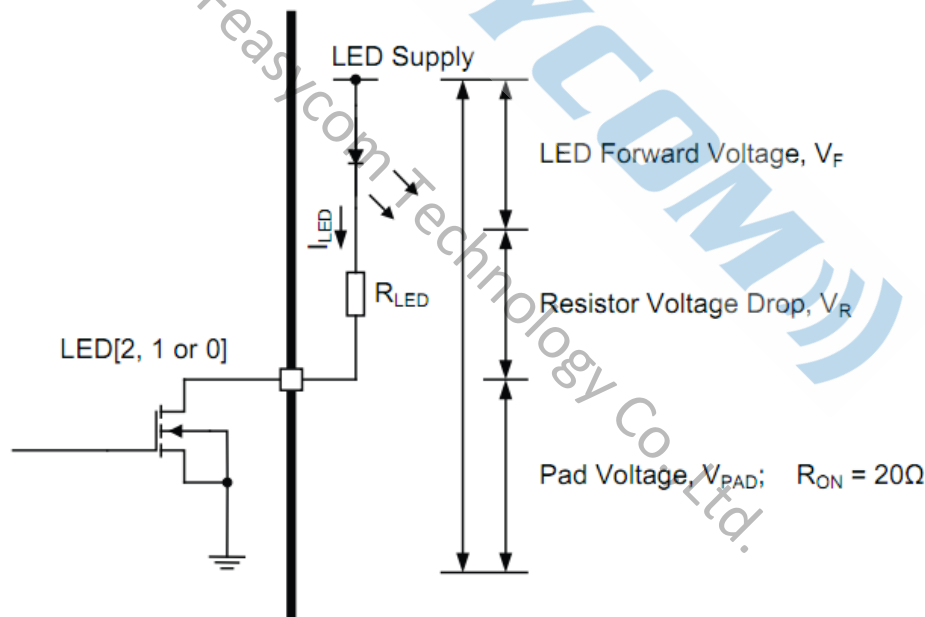


Figure 8: LED Equivalent Circuit

If a known value of current is required through the LED to give a specific luminous intensity, then the value of R_{LED} is calculated.

$$I_{LED} = \frac{V_{DD} - V_F}{R_{LED} + R_{ON}}$$

For the LED pads to act as resistance, the external series resistor, R_{LED} , needs to be such that the voltage drop across it, V_R , keeps V_{PAD} below 0.5V.

$$VDD = V_F + V_R + V_{PAD}$$

Note:

The LED current adds to the overall current. Conservative LED selection extends battery life.

4.8 Audio Interfaces

The audio interface circuit consists of:

- Single analog microphone input or dual analog line inputs
- Dual analogue audio outputs
- 1 digital microphone inputs
- 1 configurable I²S interface
- Configurable SPDIF input interface

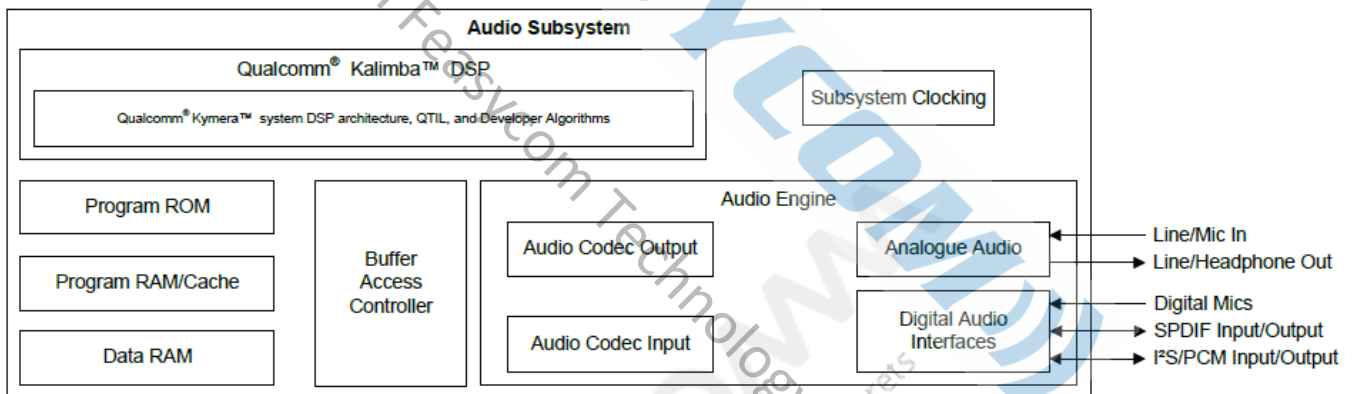


Figure 9: Audio Interface

4.8.1 Audio Input and Output

The audio input circuitry consists of 2 independent 24-bit high-quality ADC channels:

- Programmable as either stereo or dual-mono inputs.
- 1 input programmable as either microphone or line input, the other as line input only.
- Each channel can be connected as either single-ended or fully differential.
- Each channel has an analog and digital programmable gain stage.

The audio output circuitry consists of a dual differential class A-B output stage.

Note: FSC-BT1026x is designed for a differential audio output. If a single-ended audio output is required, use an external differential to single-ended converter.

4.8.2 Audio Codec Interface

The interface has the following features:

- Stereo and mono analog input for voice band and audio band
- Stereo and mono analog output for voice band and audio band

Note: To avoid any confusion regarding stereo operation, this data sheet explicitly states which is the left and right channel for audio output. Regarding audio input, software, and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel.

Audio Codec Block Diagram

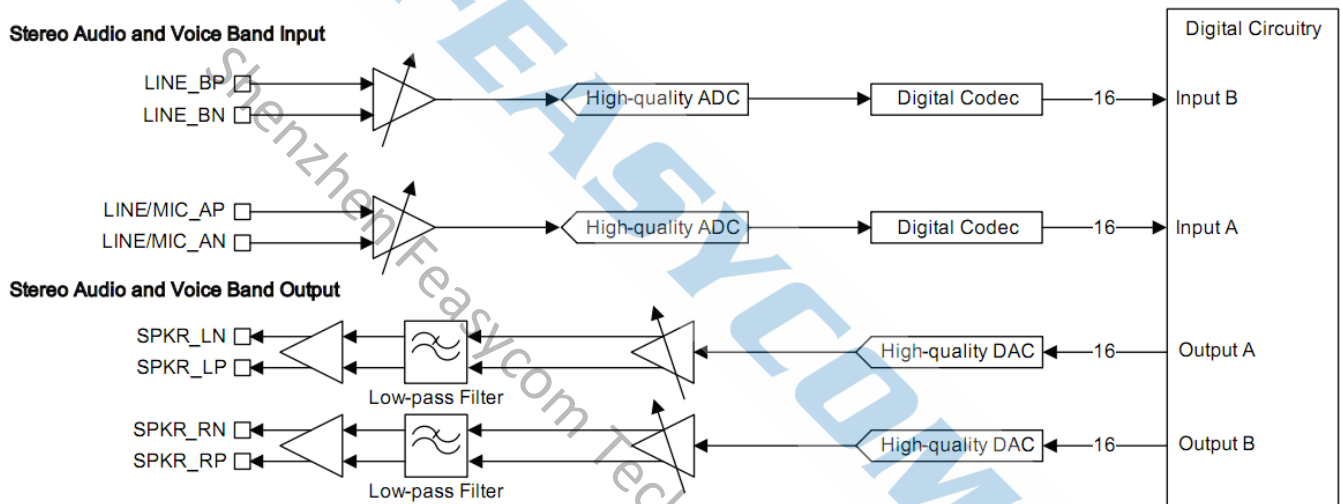


Figure 10: Audio Codec Input and Output Stages

FSC-BT1026x audio codec uses a fully differential architecture in the analog signal path. This architecture results in low common-mode-noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a dual power supply, VDD_AUDIO (internal) for the audio circuits and VDD_AUDIO_DRV (internal) for the audio driver circuits.

ADC

The FSC-BT1026x consists of 2 high-quality ADCs

- Each ADC has a second-order Sigma-Delta converter.
- Each ADC is a separate channel with identical functionality.
- Each channel has an analog and a digital gain stage.

ADC Sample Rate Selection

Each ADC supports the following pre-defined sample rates, although other rates are programmable, e.g. 40kHz:

- 8kHz
- 16kHz
- 32kHz
- 44.1kHz
- 48kHz
- 96kHz
- 192kHz

ADC Audio Input Gain

The picture below shows that the FSC-BT1026x audio input gain consists of:

- An analogue gain stage based on a pre-amplifier and an analogue gain amplifier
- A digital gain stage

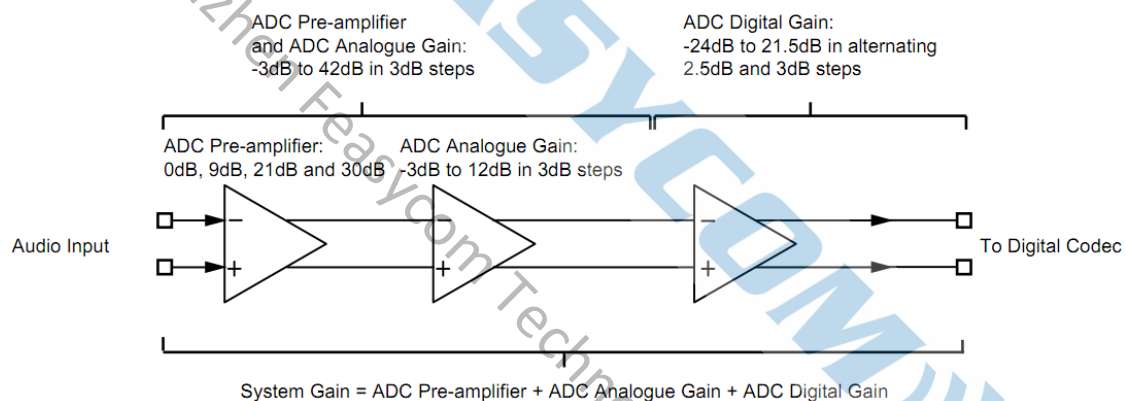


Figure 11: Audio Input Gain

ADC Pre-amplifier and analog/digital Gain

The gain of the ADC inputs can be configured in the range of -27 dB to 63.5 dB steps, making it suitable for line and microphone input levels. 0 dB is 1600 mV pk-pk input.

The ADC input impedance is nominal 6 kΩ except when 0 dB pre-amplifier gain is selected when it becomes 12 kΩ. If the input pre-amplifier is disabled, the input impedance varies between 6 kΩ and 34 kΩ, depending on gain selection. In normal operation, the input pre-amplifier is enabled.

Calls connected by the VM stream automatically select the distribution of gain within the ADC for best performance. Alternatively, the individual gain stages can be set.

ADC Digital Gain

A digital gain stage inside the ADC varies from -24dB to 21.5dB, see following table. There is also a fine gain interface with a 9-bit gain setting allowing gain changes in 1/32 steps, for more information contact Feasycom.

The firmware controls the audio input gain.

Table 5: ADC Audio Input Gain Rate

Digital Gain Selection Value	ADC Digital Gain Setting(dB)	Digital Gain Selection Value	ADC Digital Gain Setting(dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

ADC Digital IIR Filter

The ADC contains 2 integrated anti-aliasing filters:

- A long IIR filter suitable for music (>44.1kHz)
- G.722 filter is a digital IIR filter that improves the stop-band attenuation required for G.722 compliance (which is the best selection for 8kHz / 16kHz / voice)

For more information contact Feasycom.

DAC

The DAC consists of:

- Each DAC has a fourth-order Sigma-Delta converter.
- Each DAC is a separate channel with identical functionality.
- Each channel has an analog and a digital gain stage.

DAC Sample Rate Selection

Each DAC supports the following sample rates:

- 8kHz
- 11.025kHz
- 16kHz
- 22.050kHz
- 32kHz
- 40kHz
- 44.1kHz
- 48kHz
- 96kHz

DAC Gain

The DAC outputs have two gain stages, a digital stage followed by an analog stage. The digital gain varies between -24 dB and 21.5 dB and the analog gain between 0 dB and -21 dB, giving a total range of -45 dB to 21.5 dB.

Calls connected by the VM stream automatically select the distribution of gain within the DAC for best performance.

Alternatively, the individual gain stages can be set.

Table 6: DAC Digital Gain Rate Selection

Digital Gain Selection Value	DAC Digital Gain Setting(dB)	Digital Gain Selection Value	DAC Digital Gain Setting(dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 7: DAC Analogue Gain Rate Selection

Analogue Gain Selection Value	DAC Analogue Gain Setting(dB)	Analogue Gain Selection Value	DAC Analogue Gain Setting(dB)
7	0	3	-12
6	-3	2	-15
5	-6	1	-18
4	-9	0	-21

DAC Digital FIR Filter

The DAC contains an integrated digital FIR filter with the following modes:

- A default long FIR filter for best performance at $\geq 44.1\text{kHz}$.
- A short FIR to reduce latency.
- A narrow FIR (a sharp roll-off at Nyquist) for G.722 compliance. Best for 8kHz/16kHz.

4.8.3 Microphone bias generator

FSC-BT1026x contains an independent low-noise microphone bias generator. The microphone bias generator is recommended for biasing electret condensor microphones.

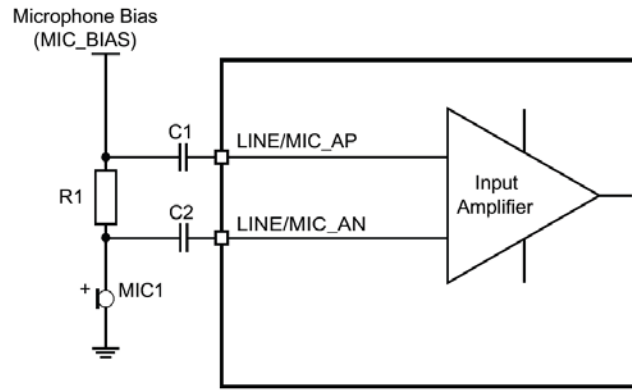


Figure 12: Microphone Biasing

The microphone bias generator provides a selectable output voltage of 1.8 V or 2.6 V nominal and derives its power from VBAT or VOUT_3V3. No output capacitor is required.

The bias resistor R1 should match the microphone load impedance, and typically is 2.2 k Ω . C1 and C2 are typically 100/150 nF to give a bass roll-off to limit wind noise on the microphone.

The mic bias generator has a maximum drop out of 300 mV, if VBAT drops below (selected output voltage – drop out voltage), the output voltage will fall below specification. The generator will continue to operate but noise performance will be impaired.

4.8.4 Line input

The picture below show 2 circuits for line input operation and show connections for either differential or single-ended inputs.

In line input mode, the input impedance of the pins to ground varies from 6k Ω to 34k Ω depending on input gain setting.

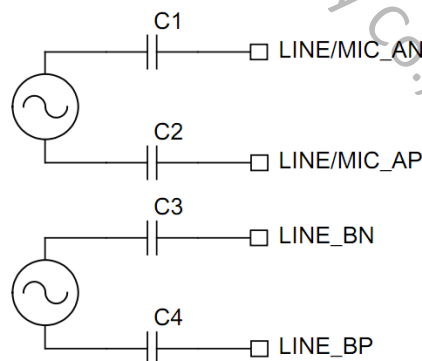


Figure 13: Differential Input

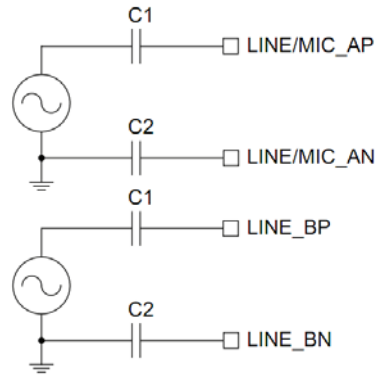


Figure 14: Single-ended Input

4.8.5 Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The analogue output circuit comprises a DAC, a buffer with gain-setting, a low-pass filter and a class AB output stage amplifier.

The picture below shows that the output is available as a differential signal between SPKR_LN and SPKR_LP for the left channel, and between SPKR_RN and SPKR_RP for the right channel.

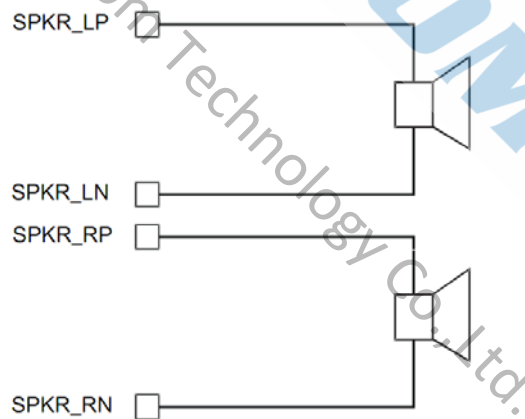


Figure 15: Speaker Output

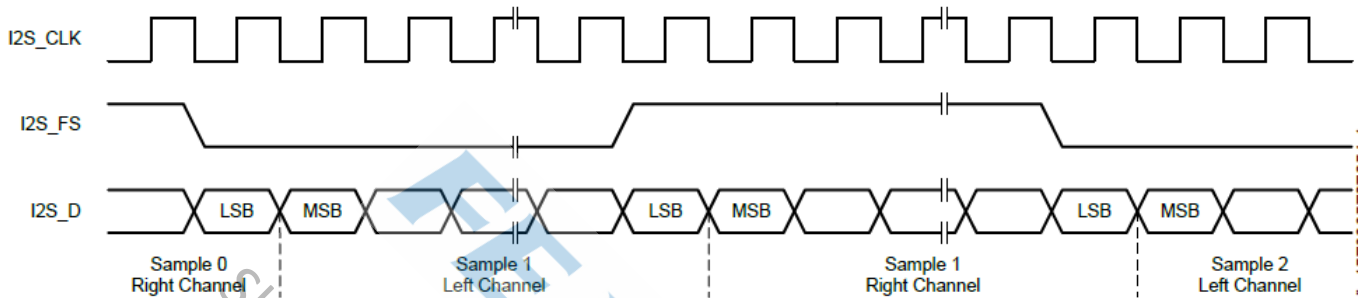
4.8.6 I2S interface

FSC-BT1026x supports I2S input and output via its one industry-standard I2S digital audio interfaces, left-justified or right-justified.

FSC-BT1026x supports several alternative PCM data formats. For further details, contact QTIL. When in PCM mode, the following pin name to function mappings apply.

Table 8: Alternative functions of the digital audio bus interface on the PCM interface

I2S Pin	PCM function
I2S_SD_OUT	PCM_OUT
I2S_SD_IN	PCM_IN
I2S_WS	PCM_SYNC
I2S_SCK	PCM_CLK

**Figure 16:** Digital audio interface modes**Table 9:** Digital audio interface slave timing

Parameter	Min	Type	Max	Unit
SCK Frequency	-	-	6.2	MHz
WS Frequency	-	-	96	KHz
t_{ch} - SCK high time	80	-	-	ns
t_{cl} - SCK low time	80	-	-	ns

Table 10: I2S/PCM slave mode timing

Parameter	Min	Type	Max	Unit
t_{ssu} - WS valid to SCK high set-up time	5	-	-	ns
t_{sh} - SCK high to WS invalid hold time	15	-	-	ns
t_{opd} - SCK low to SD_OUT valid delay time	-	-	20	ns
t_{isu} - SD_IN valid to SCK high set-up time	15	-	-	ns
t_{ih} - SCK high to SD_IN invalid hold time	5	-	-	ns

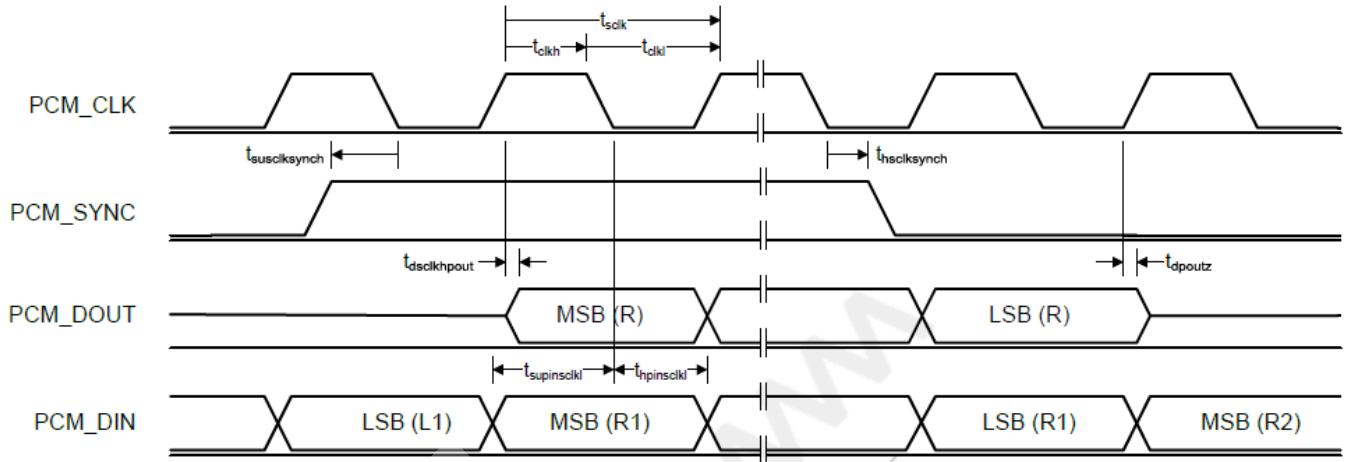


Figure 17: Digital audio interface slave timing

Table 11: Digital audio interface master timing

Parameter	Min	Type	Max	Unit
SCK Frequency	-	-	6.2	MHz
WS Frequency	-	-	96	KHz

Table 12: I2SPCM master mode timing parameters, WS and SCK as outputs

Parameter	Min	Type	Max	Unit
t_{spd} - SCK low to WS valid delay time	-	-	20	ns
t_{opd} - SCK low to WS valid delay time	-	-	20	ns
t_{isu} - SD_IN valid to SCK high set-up time	-	-	20	ns
t_{ih} - SCK high to SD_IN invalid hold time	0	-	-	ns

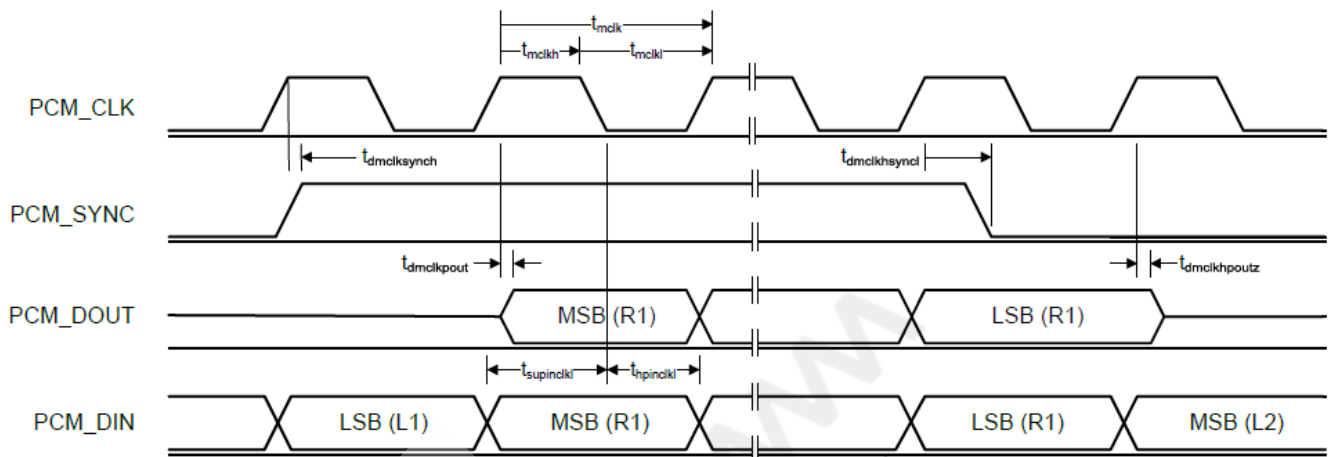


Figure 18: Digital audio interface master timing

4.9 Programming and Debug Interface

Important Note:

FSC-BT1026x provides a debug SPI interface for programming, configuring, and debugging the FSC-BT1026x.

Access to this interface is required in production. Ensure the 4 SPI signals and the SPI/I2S_SEL line are brought out to either test points or a header. The SPI/I2S_SEL line needs to be pulled high externally to use the SPI interface.

Feasycom provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from Feasycom.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 13: Absolute Maximum Rating

Parameter	Min	Max	Unit
5V (VCC_CHG)	-0.4	+5.75 / 6.50 ^(a)	V
BATTERY (LED 0,1,2)	-0.4	+4.4	V
BATTERY (VBAT_IN)	-0.4	+4.4	V
BATTERY (VREGENABLE)	-0.4	+4.4	V
VDD_USB/3.3V_OUT	-0.4	+3.6	V
VDD_IO	-0.4	+3.6	V

Other terminal voltages	VSS-0.4	VDD+0.4 ≤ 3.60 ^(b)	V
T _{ST} - Storage Temperature	-40	+85	°C

(a) Standard maximum input voltage is 5.75V, a 6.50V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact Feasycom.

(b) VDD is the VDD_IO supply domain for this I/O. Voltage must not exceed 3.6 V on any I/O.

5.2 Recommended Operating Conditions

Table 14: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
5V (VCC_CHG)	4.75 / 3.10 (a)	5	5.75 / 6.50 (b)	V
BATTERY (LED 0,1,2)	1.10	3.70	4.30	V
BATTERY (VBAT_IN)	2.8	3.3	4.30	V
BATTERY (VREGENABLE)	0	3.3	4.25	V
VDD_USB/3.3V_OUT	3.1	3.3	3.6	V
VDD_IO	1.7	1.8	3.3	V
T _A - Operating Temperature	-40	20	+85	°C

(a) Minimum input voltage of 4.75V is required for full specification, regulator operates at reduced load current from 3.1V

(b) Standard maximum input voltage is 5.75V, a 6.50V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact Feasycom.

5.3 Input/output Terminal Characteristics

5.3.1 Digital

Table 15: DC Characteristics (V_{DD} - V_{SS} = 3 ~ 3.6 V, T_A = 25°C)

Parameter	Min	Type	Max	Unit
Input Voltage				
V _{IL} - Standard IO Low level input voltage	-0.4	-	0.4	V
V _{IH} - Standard IO Low level input voltage	0.7 x VDD_IO	-	VDD_IO+0.4	V
Tr/Tf	-	-	25	nS

Output Voltage

V_{OL} - Low Level Output Voltage, $I_{OL}=4mA$	-	-	0.4	V
V_{OH} - High Level Output Voltage, $I_{OH}=-4mA$	$0.7 \times VDD_{IO}$	-	-	V
Tr/Tf	-	-	5	nS

Input and Tristate Currents

Strong pull-up	-150	-40	-10	uA
Strong pull-down	10	40	150	uA
Weak pull-up	-5	-1.0	-0.33	uA
Weak pull-down	0.33	1.0	5.0	uA
C_I Input Capacitance	1.0	-	5.0	pF

5.3.2 Battery Charger**Table 16:** Battery Charger

Parameter	Min	Type	Max	Unit	
Battery Charger					
Input voltage, VCHG	4.75 / 3.10(a)	5.00	5.75 / 6.50(b)	V	
(a) Reduced specification from 3.1V to 4.75V. Full specification >4.75V.					
(b) Standard maximum input voltage is 5.75V, a 6.50V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact Feasycom.					
Trickle Charge Mode					
Charge current I _{trickle} , as percentage of fast charge current	8	10	12	%	
V _{fast} rising threshold	-	2.9	-	V	
V _{fast} rising threshold trim step size	-	0.1	-	V	
V _{fast} falling threshold	-	2.8	-	V	
Fast Charge Mode					
Charge current during constant current mode, I _{fast}	Max,	194	200	mA	
	headroom >0.55V	-	10	mA	
	Min, headroom >0.55V				
Reduced headroom charge current, as a percentage of I _{fast}	Mid, headroom =0.15V	50	-	100	%
Charge current step size	-	10	-	mA	
V _{float} threshold, calibrated	4.16	4.20	4.24	V	
Charge termination current I _{term} , as percentage of I _{fast}	7	10	20	%	
Standby Mode					
Voltage hysteresis on VBAT_IN, V _{hyst}	100	-	150	mV	

Error Charge Mode

Headroom(a) error falling threshold	-	50	-	mV
-------------------------------------	---	----	---	----

(a) Headroom = VCC_CHG – VBAT_IN

5.3.3 USB**Table 17:USB**

Parameter	Min	Type	Max	Unit
3V3_USB for correct USB operation(internal)	3.10	3.30	3.60	V
Input Threshold				
V _{IL} - input logic level low	-	-	0.3 x 3V3_USB	V
V _{IH} - input logic level high	0.7 x 3V3_USB	-	-	V
Output Voltage Levels to Correctly Terminated USB Cable				
V _{OL} - output logic level low	0	-	0.2	V
V _{OH} - output logic level high	2.8	-	3V3_USB	V

5.3.4 LED Driver Pads**Table 18:LED Driver Pads**

Parameter	Min	Type	Max	Unit
Current, I _{PAD} - High impedance state	-	-	5	uA
Current, I _{PAD} -Current sink state	-	-	50	mA
LED pad voltage, V _{PAD} I _{PAD} = 10mA	-	-	0.55	V
V _{OL} output logic level low ^a	-	0	-	V
V _{OH} output logic level high ^a	-	0.8	-	V
V _{IL} input logic level low	-	-	0.4	V
V _{IH} input logic level high	1	-	-	V

a LED output port is open-drain and requires a pull-up

5.4 Stereo Codec**5.4.1 Analogue to Digital Converter****Table 19:Analogue to Digital Converter (single-ended/differential audio input)**

Parameter	Ccnditions	Min	Type	Max	Unit
Resolution	-	-	-	16	Bits
Output Sample Rate, F _{sample}	-	8	-	96	KHz
Input level	-	-	-	2.4	V _{pk-pk}

Input impedance	0 dB to 24 dB analog gain			20		KΩ
	27 dB to 39 dB analog gain			10		kΩ
SNR	f _{in} = 1kHz	Single	-	101	-	dBA
	48KHz	differential	-	100	-	dBA
	A-Weighted					
	THD+N < 0.1%					
	2.4V _{pk-pk} input (0dB gain)					
THD+N	f _{in} = 1kHz	Single	-	-85	-	dB
	48KHz	differential	-	-91	-	dB
	2.4V _{pk-pk} input (0dB gain)					
Digital gain	Digital gain resolution = 1/32			-24	-	21.5 dB
Analogue gain	3dB steps			-	-	39 dB
Stereo separation (crosstalk)			80	-	-	dB

5.4.1 Digital to Analogue Converter

Table 20: Digital to Analogue Converter

Parameter		Cconditions		Min	Type	Max	Unit
Resolution	-			-	-	16	Bits
Input Sample Rate, F _{sample}	-			8	-	96	KHz
SNR	f _{in} = 1kHz	F _{sample}	Load				
	B/W = 20Hz->20KHz	48kHz	32Ω	-	101	-	dBA
	A-Weighted 0dBFS input						
THD+N	f _{in} = 1kHz	F _{sample}	Load	-			
	B/W = 20Hz->20kHz	48kHz	32Ω	-	-90.5	-	dB
	0dBFS input						
Digital gain	Digital gain resolution = 1/32			-24	-	21.5	dB
Stereo separation (crosstalk)				80	-	-	dB

5.5 Auxiliary ADC

Table 21: Auxiliary ADC

Parameter		Min	Type	Max	Unit
Resolution		-	-	10	Bits
Input voltage range (a)		0	-	1.854	V
Accuracy	INL	-3	-	3	LSB
(Guaranteed monotonic)	DHL	-1	-	2	LSB
Offset		-1	-	1	LSB
Gain error		-1	-	1	%

Input bandwidth	-	100	-	KHz
Conversion time		10		uS

(a) LSB size = 1.854V/1023

5.6 Microphone bias generator

Table 22:Microphone bias generator

Parameter	Min	Type	Max	Unit
Output voltage (Tunable, step = 0.1 V)	1.5	-	2.1	V
Output current capability	0.07	-	3.0	mA
Output noise (B/W = 20 Hz → 20 kHz Unweighted)	4.5	5.1	7.3	uVrms
Crosstalk Between Microphones (Using recommended application circuit)	-	80	-	dB
Load capacitance (From parasitic PCB routing and package)	-	-	0.1	nF

5.7 Power consumptions(TBD)

Table 23: Power consumptions

Dut role	Connection		Packet type	Average current	Unit
N/A	Deep sleep	With UART host connection	-	63	uA
N/A	Page scan	Page = 1280 ms interval Window = 11.25 ms	-	243	uA
N/A	Inquiry and page scan	Inquiry = 1280 ms interval Page = 1280 ms interval Window = 11.25 ms	-	441	uA
Master	ACL	No traffic	DH1	4.89	mA
Master	ACL	File transfer	DH1	7.21	mA
Master	ACL	Sniff = 500 ms, 1 attempt, 0 timeout	DH1	150	uA
Master	ACL	Sniff = 1280 ms, 8 attempts, 1 timeout	DH1	126	uA
Master	SCO	Sniff = 100 ms, 1 attempt, PCM	HV3	9.37	mA
Master	SCO	Sniff = 100 ms, 1 attempt, mono audio codec	HV3	11.69	mA
Master	eSCO	Setting S3, sniff = 100 ms, PCM	2EV3	7.50	mA
Master	eSCO	Setting S3, sniff = 100 ms, PCM	3EV3	7.13	mA
Master	eSCO	Setting S3, sniff = 100 ms, codec	2EV3	9.81	mA
Master	eSCO	Setting S3, sniff = 100 ms, codec	3EV3	9.44	mA
Slave	ACL	No traffic	DH1	7.88	mA
Slave	ACL	File transfer	DH1	8.89	mA

Slave	ACL	Sniff = 500 ms, 1 attempt, 0 timeout	DH1	162	uA
Slave	ACL	Sniff = 1280 ms, 8 attempts, 1 timeout	DH1	169	uA
Slave	SCO	Sniff = 100 ms, 1 attempt, PCM	HV3	9.71	mA
Slave	SCO	Sniff = 100 ms, 1 attempt, mono audio codec	HV3	12.06	mA
Slave	eSCO	Setting S3, sniff = 100 ms, PCM	2EV3	7.98	mA
Slave	eSCO	Setting S3, sniff = 100 ms, PCM	3EV3	7.62	mA
Slave	eSCO	Setting S3, sniff = 100 ms, codec	2EV3	10.30	mA
Slave	eSCO	Setting S3, sniff = 100 ms, codec	3EV3	9.94	mA
Master	Bluetooth low energy	Connected, 500 ms interval	-	176	uA
Slave	Bluetooth low energy	Connected, 500 ms interval	-	163	uA
N/A	Bluetooth low energy	Non-connectable, 1.28 s, 15 octet, 3 channels	-	99	uA
N/A	Bluetooth low energy	Discoverable, 1.28 s, 15 octet, 3 channels	-	108	uA
N/A	Bluetooth low energy	Discoverable, 1.28 s, 15 octet, 3 channels	-	110	uA
N/A	Bluetooth low energy	Scanning 1.28 s, 11.25 ms, single frequency	-	255	uA

NOTE : Current consumption values are taken in the following configuration:

- VBAT pin = 3.7 V
- RF TX power set to 0 dBm
- No RF retransmissions in case of eSCO
- Microphones and speakers disconnected
- Audio gateway transmits silence when SCO or eSCO channel is open
- LEDs disconnected
- AFH classification master disabled

These values exclude SPI flash device current.

6. MSL &ESD Protection

Table 24: MSL and ESD

Parameter	Class	Max Rating
MSL grade(with JEDEC J-STD-020)		MSL 3
Human Body Model Contact Discharge per ANSI/ESDA/JEDEC JS-001	2	2kV(all pins)
Charged Device Model Contact Discharge per JEDEC/EIA JESD22-C101	III	500V (all pins)

6.1 USB Electrostatic Discharge Immunity

FSC-BT1026x has integrated ESD protection on the USB_DP and USB_DN pins as detailed in IEC 61000-4-2.

Table 25: USB Electrostatic Discharge Protection Level

IEC 61000-4-2 Level	ESD Test Voltage (Positive and Negative)	IEC 61000-4-2 Classification	Comments
1	2kV contact / 2kV air	Class 1	Normal performance within specification limits
2	4kV contact / 4kV air	Class 1	Normal performance within specification limits
3	6kV contact / 8kV air	Class 2 or class 3	Temporary degradation or operator intervention required
4	8kV contact / 15kV air	Class 2 or class 3	Temporary degradation or operator intervention required

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below **Table 27** and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below **Table 27**, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 26: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @	Floor Life Limit	Saturated @	Floor Life Limit	Saturated@	Floor Life Limit
	30°C/85%	+ 72 hours @ 30°C/60%	30°C/85%	+ 72 hours @ 30°C/60%	30°C/85%	+ 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

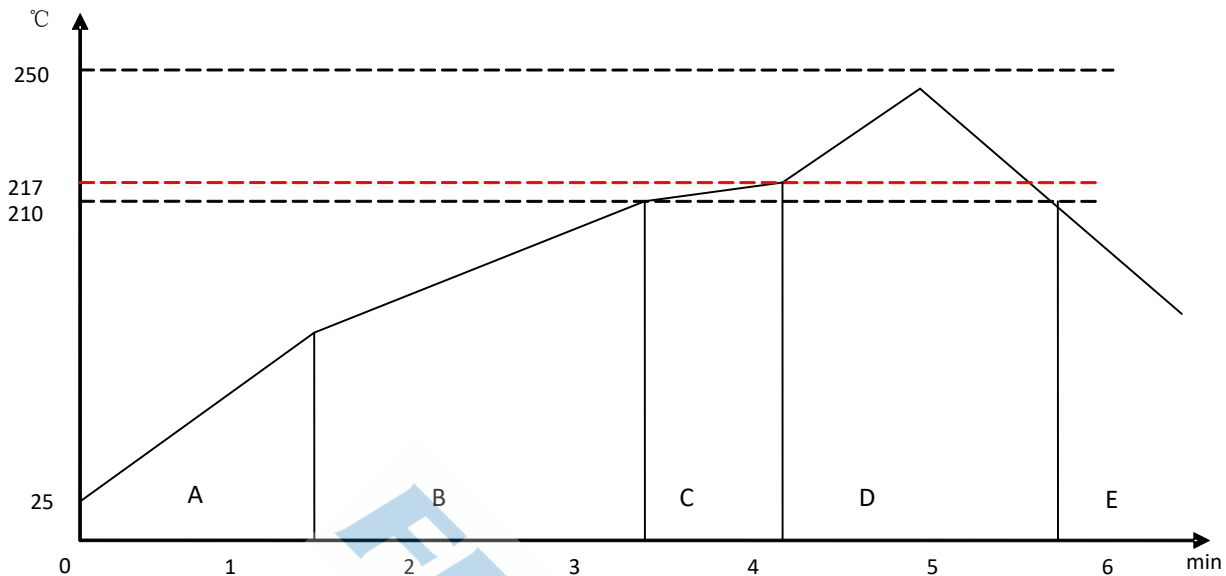


Figure 19: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (T_p) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling rate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.2mm(H) Tolerance: $\pm 0.1\text{mm}$
- Module size: 13mm X 26.9mm Tolerance: $\pm 0.2\text{mm}$

- Pad size: 1.6mmX0.6mm Tolerance: $\pm 0.2\text{mm}$
- Pad pitch: 1.0mm Tolerance: $\pm 0.1\text{mm}$

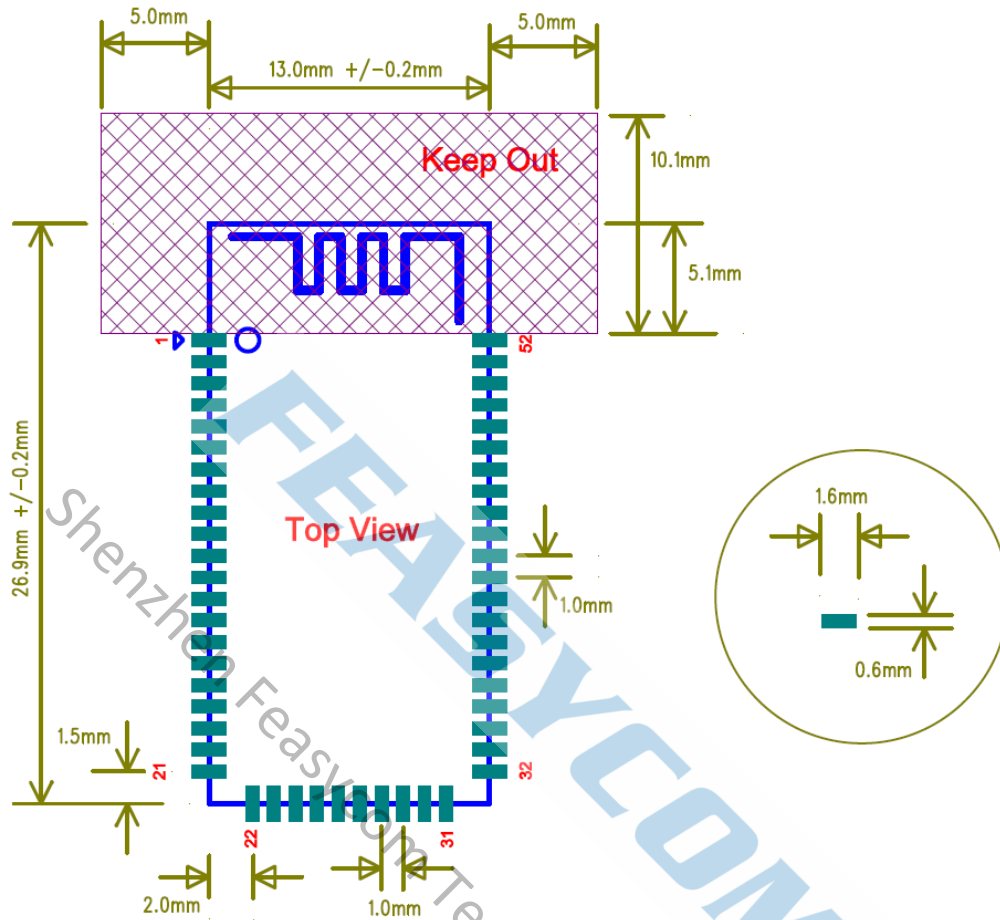


Figure 20: FSC-BT1026x footprint

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT1026x is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines (Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional

resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

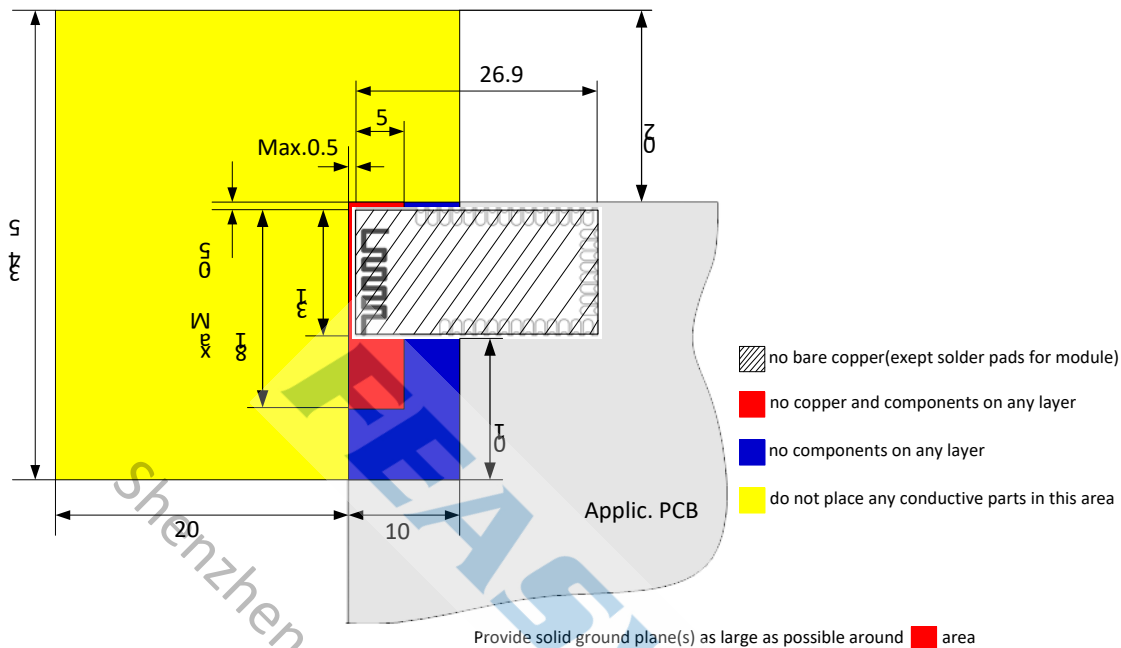


Figure 21:FSC-BT1026x Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in **Figure** below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

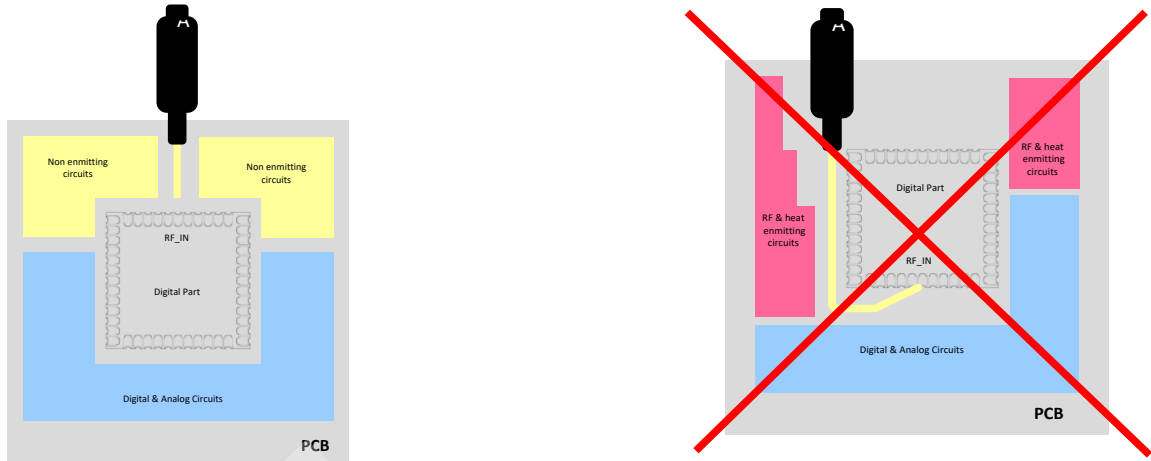


Figure 22: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

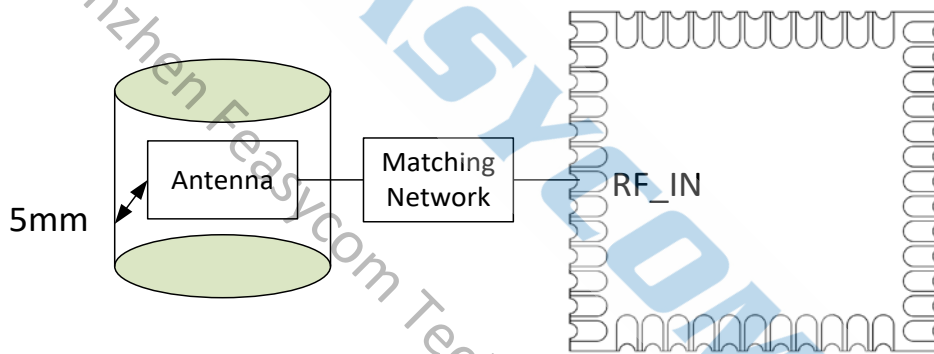


Figure 23: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

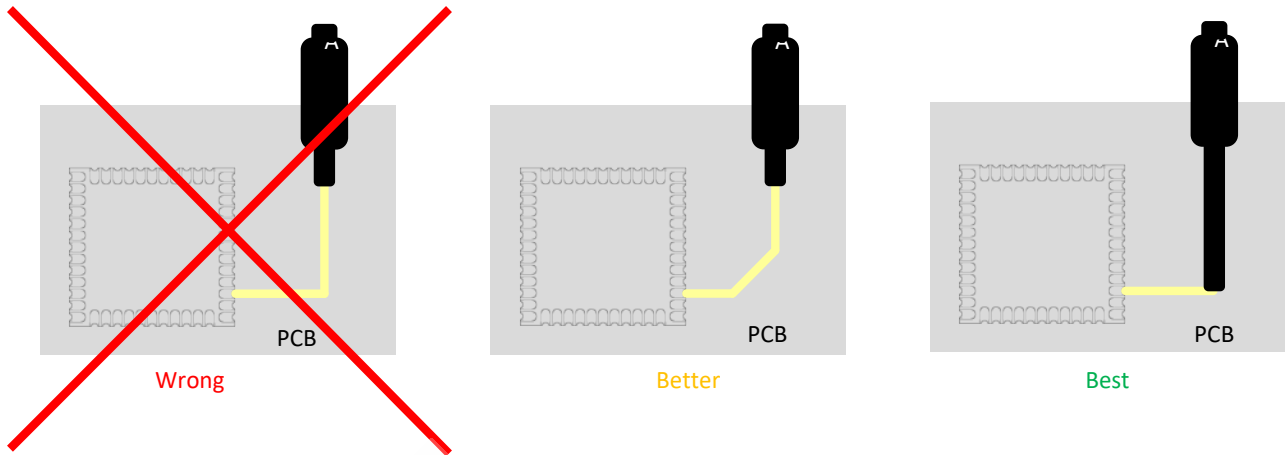


Figure 24: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

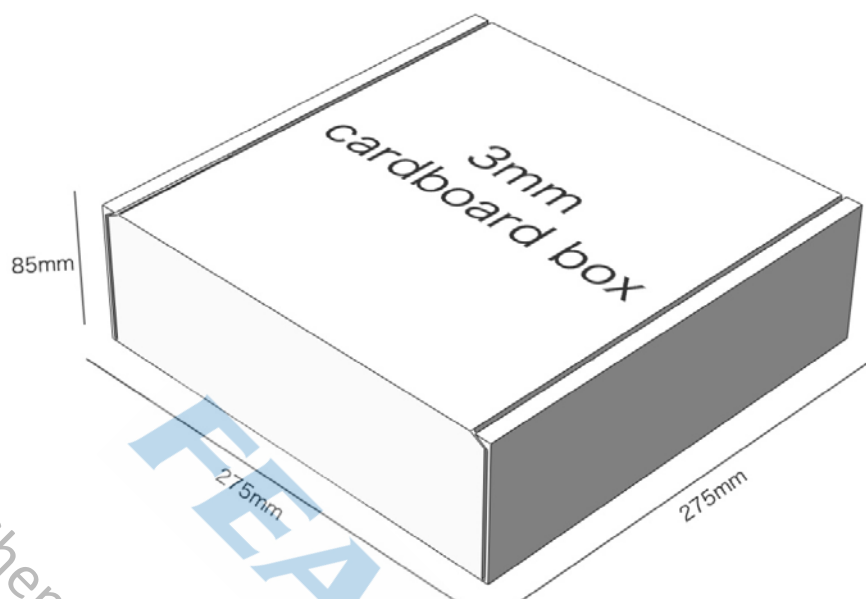
10.1 DefaultPacking

- Tray vacuum
- Tray Dimension: 180mm * 195mm



Figure 25: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 2000PCS Per Carton (Min Carton Package)

Figure 26: Packing Box

11. APPLICATION SCHEMATIC

