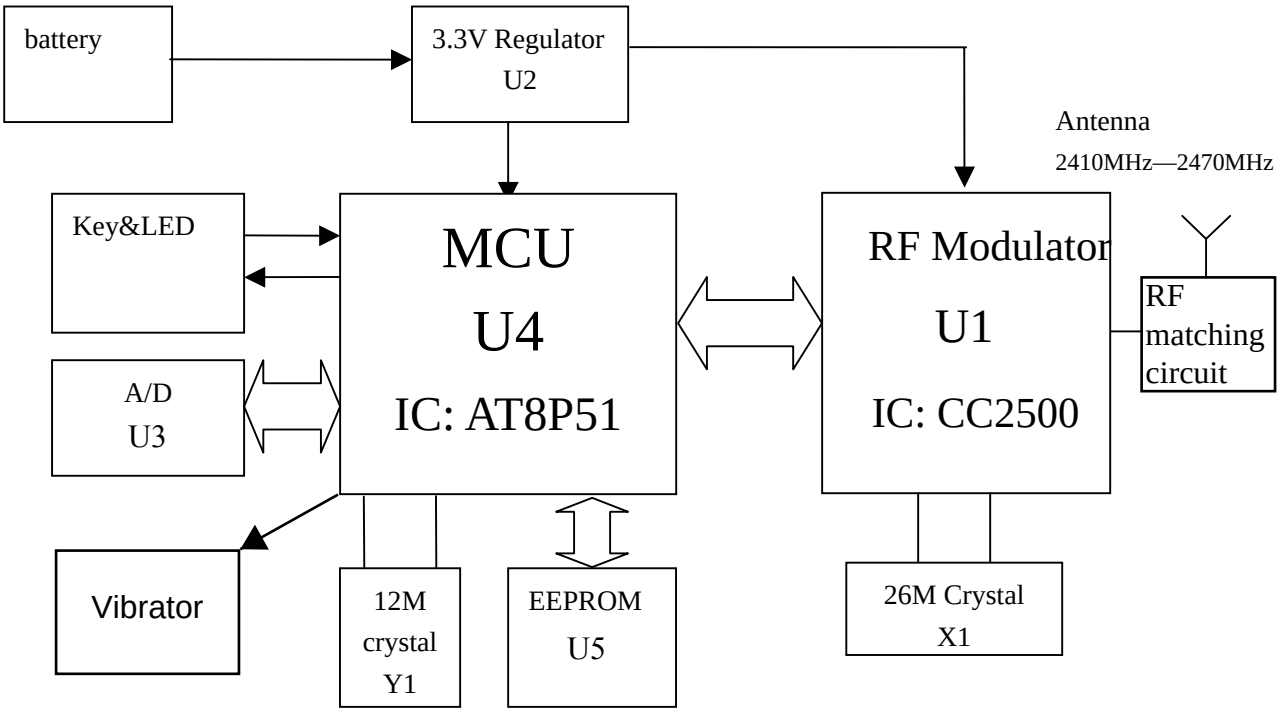
controller block diagram



Circuit Description

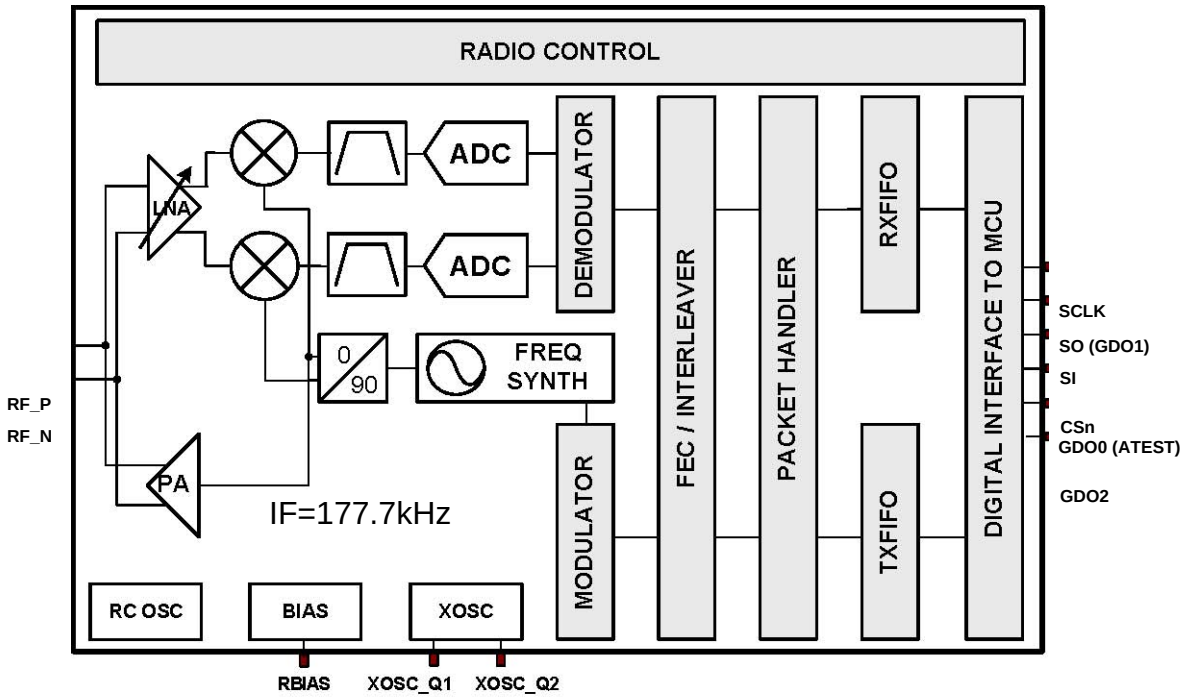


Figure 2: *CC2500* Simplified Block Diagram

A simplified block diagram is shown in Figure 2.

CC2500 RF module features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitised by the ADCs. Automatic gain control (AGC), fine channel filtering demodulation bit/packet synchronization is performed digitally.

The transmitter part of RF Module **CC2500** is based on direct synthesis of the RF frequency. The frequency synthesizer includes a completely on-chip LC VCO and a 90 degrees phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode.

A crystal is to be connected to XOSC_Q1 and XOSC_Q2. The crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part.

A 4-wire SPI serial interface is used for configuration and data buffer access.

The digital baseband includes support for channel configuration, packet handling and data buffering.

Application Circuit

Application circuit is shown in Figure 3. The external components are described in Table 1.

Bias resistor

The bias resistor R171 is used to set an accurate bias current.

Balun and RF matching

C122, C132, L121 and L131 form a balun that converts the differential RF port on **CC2500** to a single-ended RF signal (C121 and C131 are also needed for DC blocking). Together with an appropriate LC network, the balun components also transform the impedance to match a 50Ω antenna (or cable).