PS2 Wireless Gamepad Operation Principle

1. Controller Side Radio

The radio system is mainly composed of two parts: frequency synthesizer (U1, CC2500) and baseband microprocessor (U4, AT8P51). The antenna is an embedded PCB antenna matching is done by using lumped inductors and capacitors (L122, C121, C131, C132).

The microcontroller U4 scans keystrokes on the joypad, then packs the data by adding preambles, frame information, and error checking bytes to the frequency synthesizer U1 for transmission. It uses one of 75 channels (frequency range is 2.410-2.470GHz) to send signal in random to the dongle, and the channels change frequency is 62.5Hz (i.e. 0.016s). There are 4 synchronous channels (distribute in the 75 channels uniformity) that are used for connect with the dongle. These synchronous channels will scan with channels changing frequency, 62.5Hz (i.e. 0.016s), before connected with dongle. The system will change the channel frequency randomly after connected with the dongle.

The joypad is powered by batteries and regulated to 3.3V by regulator U2. And, the microcontroller U4 is used to control the vibrator (motor left and right) for motion action to the user. The power consumption of RF module is about 4mA, the total power consumption of the joypad side radio system is about 8mA in normal working mode. It will enter sleep mode if no key be pressed after 5 minutes, in this mode the total power consumption of joypad is only about 40uA*.

CC2500
Single Chip Low Cost Low Power RF Transceiver

Applications

- *2400-2483.5 MHz ISM/SRD band systems*
- *Consumer Electronics*
- *Wireless game controllers*
- *Wireless audio*
- *Wireless keyboard and mouse*

Product Description

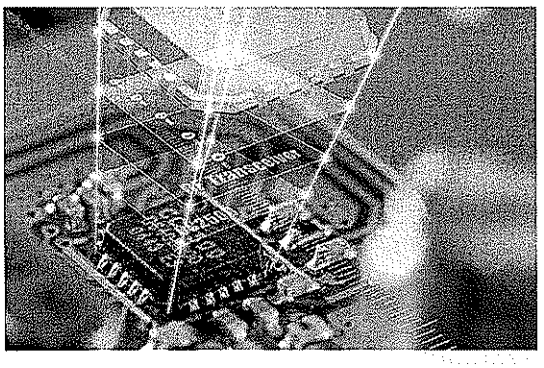
The **CC2500** is a low cost true single chip 2.4 GHz transceiver designed for very low power wireless applications. The circuit is intended for the ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency band at 2400-2483.5 MHz.

The RF transceiver is integrated with a highly configurable baseband modem. The modem supports various modulation formats and has a configurable data rate up to 500 kbps. The communication range can be increased by enabling a Forward Error Correction option, which is integrated in the modem.

CC2500 provides extensive hardware support for packet handling, data buffering, burst transmissions, clear channel assessment, link quality indication and wake-on-radio.

The main operating parameters and the 64-byte transmit/receive FIFOs of **CC2500** can be controlled via an SPI interface. In a typical system, the **CC2500** will be used together with a microcontroller and a few additional passive components.

CC2500 is based on Chipcon's SmartRF®04 technology in 0.18 µm CMOS.



Key Features

- Small size (QLP 4x4 mm package, 20 pins)
- True single chip 2.4 GHz RF transceiver
- Frequency range: *2400-2483.5 MHz*
- High sensitivity (–101 dBm at 10 kbps, 1% packet error rate)
- Programmable data rate up to 500 kbps
- Low current consumption (13.3 mA in RX, 250 kbps, input 30 dB above sensitivity limit)
- Programmable output power up to +1 dBm
- Excellent receiver selectivity and blocking performance
- Very few external components: Completely on-chip frequency synthesizer, no external filters or RF switch needed
- Programmable baseband modem
- Ideal for multi-channel operation
- Configurable packet handling hardware
- Suitable for frequency hopping systems due to a fast settling frequency synthesizer
- Optional Forward Error Correction with interleaving
- Separate 64-byte RX and TX data FIFOs
- Efficient SPI interface: All registers can be programmed with one "burst" transfer
- Digital RSSI output
- Suited for systems compliant with EN 300 328 and EN 300 440 class 2 (Europe), CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
- Wake-on-radio functionality for automatic low-power RX polling
- Many powerful digital features allow a high-performance RF system to be made using an inexpensive microcontroller
- Integrated analog temperature sensor
- Lead-free "green" package

Features (continued from front page)

- Flexible support for packet oriented systems: On chip support for sync word detection, address check, flexible packet length and automatic CRC handling.
- Programmable channel filter bandwidth
- 2-FSK, GFSK and MSK supported
- OOK supported
- Automatic Frequency Compensation can be used to align the frequency synthesizer to received centre frequency
- Optional automatic whitening and de-whitening of data
- Support for asynchronous transparent receive/transmit mode for backwards compatibility with existing radio communication protocols
- Programmable Carrier Sense indicator
- Programmable Preamble Quality Indicator for detecting preambles and improved protection against sync word detection in random noise
- Support for automatic Clear Channel Assessment (CCA) before transmitting (for listen-before-talk systems)
- Support for per-package Link Quality Indication

Abbreviations

Abbreviations used in this data sheet are described below.

2-FSK	Binary Frequency Shift Keying
ADC	Analog to Digital Converter
AFC	Automatic Frequency Offset Compensation
AGC	Automatic Gain Control
AMR	Automatic Meter Reading
ASK	Amplitude Shift Keying
BER	Bit Error Rate
CCA	Clear Channel Assessment
CRC	Cyclic Redundancy Check
CS	Carrier Sense
DC	Direct Current
EIRP	Equivalent Isotropic Radiated Power
ESR	Equivalent Series Resistance
FEC	Forward Error Correction
FIFO	First-In-First-Out
FHSS	Frequency Hopping Spread Spectrum
FSK	Frequency Shift Keying
GFSK	Gaussian shaped Frequency Shift Keying
IF	Intermediate Frequency
LBT	Listen Before Transmit
LNA	Low Noise Amplifier
LO	Local Oscillator
LQI	Link Quality Indicator
MCU	Microcontroller Unit
MSK	Minimum Shift Keying
NA	Not Applicable
PA	Power Amplifier
PCB	Printed Circuit Board
PD	Power Down
PER	Packet Error Rate
PLL	Phase Locked Loop
POR	Power-on Reset
PQI	Preamble Quality Indicator
PQT	Preamble Quality Threshold
RCOSC	RC Oscillator
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
RX	Receive, Receive Mode
SAW	Surface Aqustic Wave
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
TBD	To Be Defined
TX	Transmit, Transmit Mode
VCO	Voltage Controlled Oscillator
WOR	Wake on Radio, Low power polling
XOSC	Crystal Oscillator
XTAL	Crystal

Table Of Contents

1 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings given in Table 1 be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

Parameter	Min	Max	Units	Condition
Supply voltage	–0.3	3.6	V	All supply pins must have the same voltage
Voltage on any digital pin	–0.3	VDD+0.3 max 3.6	V	
Voltage on the pins RF_P, RF_N and DCOUPL	–0.3	2.0	V	
Voltage ramp-up rate		120	kV/µs	
Input RF level		+10	dBm	
Storage temperature range	–50	150	°C	
Solder reflow temperature		260	°C	T = 10 s

Table 1: Absolute Maximum Ratings

2 Operating Conditions

The operating conditions for ***CC2500*** are listed Table 2 in below.

Parameter	Min	Max	Unit	Condition
Operating temperature	–40	85	°C	
Operating supply voltage	1.8	3.6	V	All supply pins must have the same voltage

Table 2: Operating Conditions

3 General Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
Frequency range	2400		2483.5	MHz	
Data rate	1.2		500	kbps	Modulation formats supported: (Shaped) MSK (also known as differential offset QPSK) up to 500 kbps 2-FSK up to 500 kbps GFSK and OOK (up to 250 kbps) Optional Manchester encoding (halves the data rate).

Table 3: General Characteristics

4 Electrical Specifications

4.1 Current Consumption

Tc = 25°C, VDD = 3.0 V if nothing else stated. All measurements were performed using the CC2500EM reference design.

Parameter	Min	Typ	Max	Unit	Condition
Current consumption in power down modes		400		nA	Voltage regulator to digital part off, register values retained (SLEEP state)
		900		nA	Voltage regulator to digital part off, register values retained, low-power RC oscillator running (SLEEP state with WOR enabled)
		92		µA	Voltage regulator to digital part off, register values retained, XOSC running (SLEEP state with MCSM0.OSC_FORCE_ON set)
		157		µA	Voltage regulator to digital part on, all other modules in power down (XOFF state)
Current consumption		1.4		µA	Automatic RX polling once each second, using low-power RC oscillator, with 460 kHz filter bandwidth and 250 kbps data rate, PLL calibration every 4th wakeup. Average current with signal in channel *below* carrier sense level.
		17		µA	Same as above, but with signal in channel *above* carrier sense level, 1.9 ms RX timeout, and no preamble/sync word found.
		0.9		µA	Automatic RX polling every 15th second, using low-power RC oscillator, with 460 kHz filter bandwidth and 250 kbps data rate, PLL calibration every 4th wakeup. Average current with signal in channel below carrier sense level.
		37		µA	Same as above, but with signal in channel *above* carrier sense level, 14 ms RX timeout, and no preamble/sync word found.
		1.5		mA	Only voltage regulator to digital part and crystal oscillator running (IDLE state)
		7.4		mA	Only the frequency synthesizer running (after going from IDLE until reaching RX or TX states, and frequency calibration states)
Current consumption, RX states		15.3		mA	Receive mode, 2.4 kbps, input at sensitivity limit, MDMCFG2.DEM_DCFILT_OFF = 1
		12.8		mA	Receive mode, 2.4 kbps, input 30 dB above sensitivity limit, MDMCFG2.DEM_DCFILT_OFF = 1
		15.4		mA	Receive mode, 10 kbps, input at sensitivity limit, MDMCFG2.DEM_DCFILT_OFF = 1
		12.9		mA	Receive mode, 10 kbps, input 30 dB above sensitivity limit, MDMCFG2.DEM_DCFILT_OFF = 1
		18.8		mA	Receive mode, 250 kbps, input at sensitivity limit, MDMCFG2.DEM_DCFILT_OFF = 0
		15.7		mA	Receive mode, 250 kbps, input 30 dB above sensitivity limit, MDMCFG2.DEM_DCFILT_OFF = 0
		16.6		mA	Receive mode, 250 kbps reduced current, input at sensitivity limit, MDMCFG2.DEM_DCFILT_OFF = 1
		13.3		mA	Receive mode, 250 kbps reduced current, input 30 dB above sensitivity limit, MDMCFG2.DEM_DCFILT_OFF = 1
		19.6		mA	Receive mode, 500 kbps, input at sensitivity limit, MDMCFG2.DEM_DCFILT_OFF = 0
		17.0		mA	Receive mode, 500 kbps, input 30 dB above sensitivity limit, MDMCFG2.DEM_DCFILT_OFF = 0
Current consumption, TX states		11.1		mA	Transmit mode, –12 dBm output power
		15.1		mA	Transmit mode, -6 dBm output power

Parameter	Min	Typ	Max	Unit	Condition
		21.2		mA	Transmit mode, 0 dBm output power
		21.5		mA	Transmit mode, 1.5 dBm output power

Table 4: Current Consumption

4.2 RF Receive Section

Tc = 25°C, VDD = 3.0 V if nothing else stated. All measurements were performed using the CC2500EM reference design.

Parameter	Min	Typ	Max	Unit	Condition/Note
Digital channel filter bandwidth	58		812	kHz	User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0 MHz crystal).
2.4 kbps data rate, reduced current, MDMCFG2.DEM_DCFILT_OFF = 1 (2-FSK, 1% packet error rate, 20 bytes packet length, 203 kHz digital channel filter bandwidth)					
Receiver sensitivity		–104		dBm	The sensitivity can be improved to typically –106 dBm by setting MDMCFG2.DEM_DCFILT_OFF = 0 . The typical current consumption is in this case 17.0 mA at sensitivity limit.
Saturation		–13		dBm	
Adjacent channel rejection		23		dB	Desired channel 3 dB above the sensitivity limit. 250 kHz channel spacing
Alternate channel rejection		31		dB	Desired channel 3 dB above the sensitivity limit. 250 kHz channel spacing
					See Figure 17 for plot of selectivity versus frequency offset
10 kbps data rate, reduced current, MDMCFG2.DEM_DCFILT_OFF = 1 (2-FSK, 1% packet error rate, 20 bytes packet length, 232 kHz digital channel filter bandwidth)					
Receiver sensitivity		–99		dBm	The sensitivity can be improved to typically –101 dBm by setting MDMCFG2.DEM_DCFILT_OFF = 0 . The typical current consumption is in this case 17.3 mA at sensitivity limit.
Saturation		–9		dBm	
Adjacent channel rejection		18		dB	Desired channel 3 dB above the sensitivity limit. 250 kHz channel spacing
Alternate channel rejection		25		dB	Desired channel 3 dB above the sensitivity limit. 250 kHz channel spacing
					See Figure 18 for plot of selectivity versus frequency offset
250 kbps data rate, MDMCFG2.DEM_DCFILT_OFF = 0 (MSK, 1% packet error rate, 20 bytes packet length, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		–89		dBm	
Saturation		–13		dBm	
Adjacent channel rejection		21		dB	Desired channel 3 dB above the sensitivity limit. 750 kHz channel spacing
Alternate channel rejection		30		dB	Desired channel 3 dB above the sensitivity limit. 750 kHz channel spacing
					See Figure 19 for plot of selectivity versus frequency offset

Parameter	Min	Typ	Max	Unit	Condition/Note
250 kbps data rate, reduced current, MDMCFG2.DEM_DCFILT_OFF = 1 (MSK, 1% packet error rate, 20 bytes packet length, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		–87		dBm	
Saturation		–13		dBm	
Adjacent channel rejection		21		dB	Desired channel 3 dB above the sensitivity limit. 750 kHz channel spacing
Alternate channel rejection		30		dB	Desired channel 3 dB above the sensitivity limit. 750 kHz channel spacing
					See Figure 20 for plot of selectivity versus frequency offset
500 kbps data rate, MDMCFG2.DEM_DCFILT_OFF = 0 (MSK, 1% packet error rate, 20 bytes packet length, 812 kHz digital channel filter bandwidth)					
Receiver sensitivity		–82		dBm	
Saturation		–18		dBm	
Adjacent channel rejection		14		dB	Desired channel 3 dB above the sensitivity limit. 1 MHz channel spacing
Alternate channel rejection		25		dB	Desired channel 3 dB above the sensitivity limit. 1 MHz channel spacing
					See Figure 21 for plot of selectivity versus frequency offset
General					
Selectivity at 10 MHz offset		47		dB	Desired channel at –80 dBm. Compliant with ETSI EN 300 440 class 2 receiver requirements.
Selectivity at 20 MHz offset		52		dB	Desired channel at –80 dBm. Compliant with ETSI EN 300 440 class 2 receiver requirements.
Selectivity at 50 MHz offset		54		dB	Desired channel at –80 dBm. Compliant with ETSI EN 300 440 class 2 receiver requirements.
Spurious emissions 25 MHz – 1 GHz Above 1 GHz			 –57 –47	 dBm dBm	

Table 5: RF Receive Parameters

4.3 RF Transmit Section

Tc = 25°C, VDD = 3.0 V, 0 dBm if nothing else stated. All measurements were performed using the CC2500EM reference design.

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential load impedance		80 + j74		Ω	Differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna. Follow the CC2500EM reference design available from Chipcon's website.
Output power, highest setting		+1		dBm	Output power is programmable and is available across the entire frequency band Delivered to a 50 Ω single-ended load via Chipcon reference design RF matching network.
Output power, lowest setting		–30		dBm	Output power is programmable and is available across the entire frequency band Delivered to a 50 Ω single-ended load via Chipcon reference design RF matching network.
Spurious emissions					
25 MHz – 1 GHz			–36	dBm	
47-74, 87.5-118, 174-230, 470-862 MHz			–54	dBm	
1800-1900 MHz			–47	dBm	Restricted band in Europe
At 2·RF and 3·RF			–41	dBm	Restricted bands in USA
Otherwise above 1 GHz			–30	dBm	

Table 6: RF Transmit Parameters

4.4 Crystal Oscillator

Tc = 25°C, VDD = 3.0 V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency	26	26	27	MHz	
Tolerance		±40		ppm	This is the total tolerance including a) initial tolerance, b) crystal loading, c) aging and d) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing / bandwidth.
ESR			100	Ω	
Start-up time		300		µs	Measured on Chipcon's CC2500EM reference design.

Table 7: Crystal Oscillator Parameters

4.5 Low Power RC Oscillator

Typical performance is for Tc = 25°C @ VDD = 3.0 V if nothing else is stated. The values in the table are simulated results and will be updated in later versions of the data sheet.

Parameter	Min	Typ	Max	Unit	Condition/Note
Calibrated frequency	34.6	34.7	36	kHz	Calibrated RC Oscillator frequency is XTAL frequency divided by 750
Frequency accuracy after calibration			+0.3 -10	%	
Temperature coefficient		+0.4		% / °C	Frequency drift when temperature changes after calibration
Supply voltage coefficient		+3		% / V	Frequency drift when supply voltage changes after calibration
Initial calibration time		2		ms	When the RC Oscillator is enabled, calibration is continuously done in the background as long as the crystal oscillator is running.
Wake-up period	58e-6		59650	Seconds	Programmable, dependent on XTAL frequency

Table 8: RC Oscillator Parameters

4.6 Frequency Synthesizer Characteristics

Tc = 25°C, VDD = 3.0 V if nothing else stated. All measurements were performed using the CC2500EM reference design.

Parameter	Min	Typ	Max	Unit	Condition/Note
Programmed frequency resolution	397	$F_{XOSC}/2^{16}$	412	Hz	26-27 MHz crystal.
Synthesizer frequency tolerance		±40		ppm	Given by crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing.
RF carrier phase noise		–78		dBc/Hz	@ 50 kHz offset from carrier
RF carrier phase noise		–78		dBc/Hz	@ 100 kHz offset from carrier
RF carrier phase noise		–81		dBc/Hz	@ 200 kHz offset from carrier
RF carrier phase noise		–90		dBc/Hz	@ 500 kHz offset from carrier
RF carrier phase noise		–100		dBc/Hz	@ 1 MHz offset from carrier
RF carrier phase noise		–108		dBc/Hz	@ 2 MHz offset from carrier
RF carrier phase noise		–116		dBc/Hz	@ 5 MHz offset from carrier
RF carrier phase noise		–127		dBc/Hz	@ 10 MHz offset from carrier
PLL turn-on / hop time		90		µs	Time from leaving the IDLE state until arriving in the RX, FSTXON or TX state, when not performing calibration. Crystal oscillator running.
PLL RX/TX and TX/RX settling time		10		µs	Settling time for the 1xIF frequency step from RX to TX, and vice versa.
PLL calibration time		18739		XOSC cycles	Calibration can be initiated manually, or automatically before entering or after leaving RX/TX.
	0.69	0.72	0.72	ms	Min/typ/max time is for 27/26/26 MHz crystal frequency.

Table 9: Frequency Synthesizer Parameters

4.7 Analog Temperature Sensor

The characteristics of the analog temperature sensor are listed in Table 10 below. Note that it is necessary to write 0xBF to the PTEST register to use the analog temperature sensor in the IDLE state.

Parameter	Min	Typ	Max	Unit	Condition/Note
Output voltage at –40°C		0.660		V	
Output voltage at 0°C		0.755		V	
Output voltage at +40°C		0.859		V	
Output voltage at +80°C		0.958		V	
Output voltage at +120°C		1.056		V	
Temperature coefficient		2.54		mV/°C	Fitted from –20°C to +80°C
Error in calculated temperature, calibrated		0		°C	From –20°C to +80°C when using 2.54 mV / °C, after 1-point calibration at room temperature
Current consumption increase when enabled		0.3		mA	

Table 10: Analog Temperature Sensor Parameters

4.8 DC Characteristics

The DC Characteristics of ***CC2500*** are listed in Table 11 below.

Tc = 25°C if nothing else stated.

Digital Inputs/Outputs	Min	Max	Unit	Condition
Logic "0" input voltage	0	0.7	V	
Logic "1" input voltage	VDD-0.7	VDD	V	
Logic "0" output voltage	0	0.5	V	For up to 4 mA output current
Logic "1" output voltage	VDD-0.3	VDD	V	For up to 4 mA output current
Logic "0" input current	NA	–1	µA	Input equals 0V
Logic "1" input current	NA	1	µA	Input equals VDD

Table 11: DC Characteristics

4.9 Power-On Reset

When the power supply complies with the requirements in Table 12 below, proper Power-On-Reset functionality is guaranteed. Otherwise, the chip should be assumed to have unknown state until transmitting an SRES strobe over the SPI interface. See Section 19.1 on page 35 for further details.

Parameter	Min	Typ	Max	Unit	Condition/Note
Power ramp-up time			5	ms	From 0 V until reaching 1.8 V
Power off time	1			ms	Minimum time between power-on and power-off.

Table 12: Power-On Reset Requirements

5 Pin Configuration

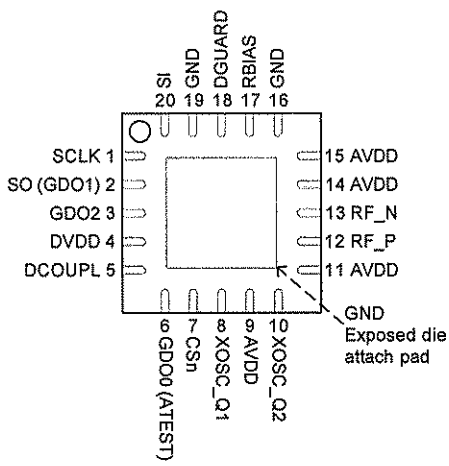


Figure 1: Pinout top view

Note: The exposed die attach pad **must** be connected to a solid ground plane as this is the main ground connection for the chip.

Pin #	Pin name	Pin type	Description
1	SCLK	Digital Input	Serial configuration interface, clock input
2	SO (GDO1)	Digital Output	Serial configuration interface, data output. Optional general output pin when CSn is high
3	GDO2	Digital Output	Digital output pin for general use: • Test signals • FIFO status signals • Clear Channel Indicator • Clock output, down-divided from XOSC • Serial output RX data
4	DVDD	Power (Digital)	1.8 - 3.6 V digital power supply for digital I/O's and for the digital core voltage regulator
5	DCOUPL	Power (Digital)	1.6 - 2.0 V digital power supply output for decoupling. NOTE: This pin is intended for use with the CC2500 only. It can not be used to provide supply voltage to other devices.
6	GDO0 (ATEST)	Digital I/O	Digital output pin for general use: • Test signals • FIFO status signals • Clear Channel Indicator • Clock output, down-divided from XOSC • Serial output RX data • Serial input TX data Also used as analog test I/O for prototype/production testing
7	CSn	Digital Input	Serial configuration interface, chip select
8	XOSC_Q1	Analog I/O	Crystal oscillator pin 1, or external clock input
9	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
10	XOSC_Q2	Analog I/O	Crystal oscillator pin 2
11	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
12	RF_P	RF I/O	Positive RF input signal to LNA in receive mode Positive RF output signal from PA in transmit mode
13	RF_N	RF I/O	Negative RF input signal to LNA in receive mode Negative RF output signal from PA in transmit mode
14	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
15	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
16	GND	Ground (Analog)	Analog ground connection
17	RBIAS	Analog I/O	External bias resistor for reference current
18	DGUARD	Power (Digital)	Power supply connection for digital noise isolation
19	GND	Ground (Digital)	Ground connection for digital noise isolation
20	SI	Digital Input	Serial configuration interface, data input

Table 13: Pinout overview

6 Circuit Description

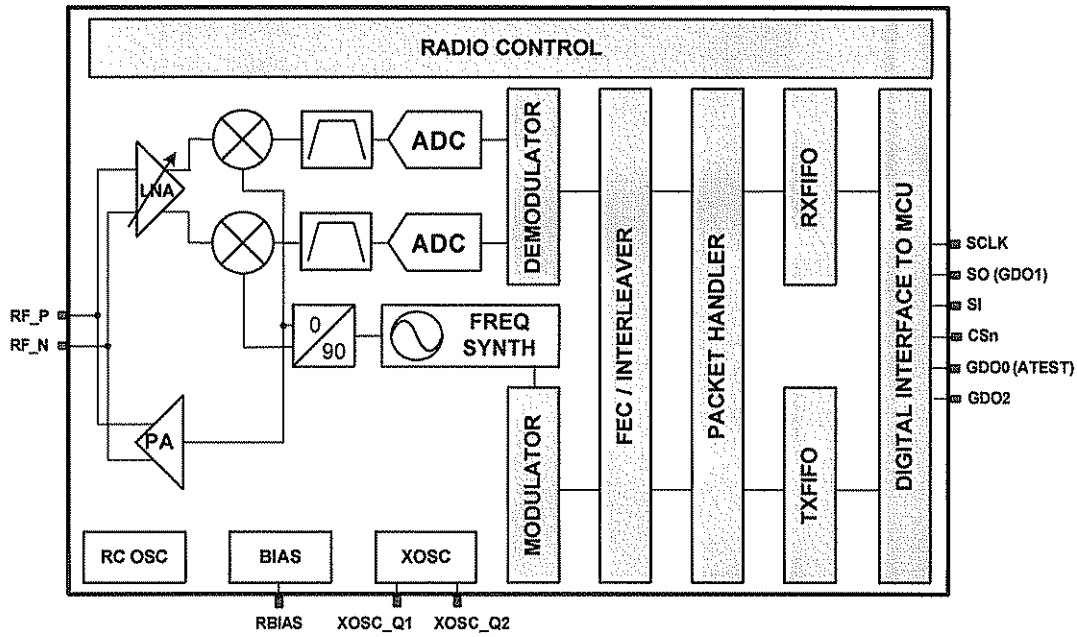


Figure 2: CC2500 simplified block diagram

A simplified block diagram of CC2500 is shown in Figure 2.

CC2500 features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitised by the ADCs. Automatic gain control (AGC), fine channel filtering, demodulation bit/packet synchronization is performed digitally.

The transmitter part of CC2500 is based on direct synthesis of the RF frequency.

The frequency synthesizer includes a completely on-chip LC VCO and a 90 degrees phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode.

A crystal is to be connected to XOSC_Q1 and XOSC_Q2. The crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part.

A 4-wire SPI serial interface is used for configuration and data buffer access.

The digital baseband includes support for channel configuration, packet handling and data buffering.

7 Application Circuit

Only a few external components are required for using the CC2500. The recommended application circuit is shown in Figure 3. The external components are described in Table 14, and typical values are given in Table 15. Note that the PCB antenna alternative indicated in Figure 3 is preliminary and subject to changes. Performance for the PCB antenna alternative will be included in future revisions of this data sheet.

Bias resistor

The bias resistor R171 is used to set an accurate bias current.

Balun and RF matching

C122, C132, L121 and L131 form a balun that converts the differential RF signal on CC2500 to a single-ended RF signal (C121 and C131 are also needed for DC blocking). Together

with an appropriate LC network, the balun components also transform the impedance to match a 50 Ω antenna (or cable). Component values for the RF balun and LC network are easily found using the SmartRF® Studio software. Suggested values are listed in Table 15.

Crystal

The crystal oscillator uses an external crystal with two loading capacitors (C81 and C101). See Section 26 on page 44 for details.

Power supply decoupling

The power supply must be properly decoupled close to the supply pins. Note that decoupling capacitors are not shown in the application circuit. The placement and the size of the decoupling capacitors are very important to achieve the optimum performance. Chipcon provides a reference design that should be followed closely.

Component	Description
C51	Decoupling capacitor for on-chip voltage regulator to digital part
C81/C101	Crystal loading capacitors, see Section 26 on page 44 for details
C121/C131	RF balun DC blocking capacitors
C122/C132	RF balun/matching capacitors
C123/C124	RF LC filter/matching capacitors
L121/L131	RF balun/matching inductors (inexpensive multi-layer type)
L122	RF LC filter inductor (inexpensive multi-layer type)
R171	Resistor for internal bias current reference
XTAL	26-27 MHz crystal, see Section 26 on page 44 for details

Table 14: Overview of external components (excluding supply decoupling capacitors)

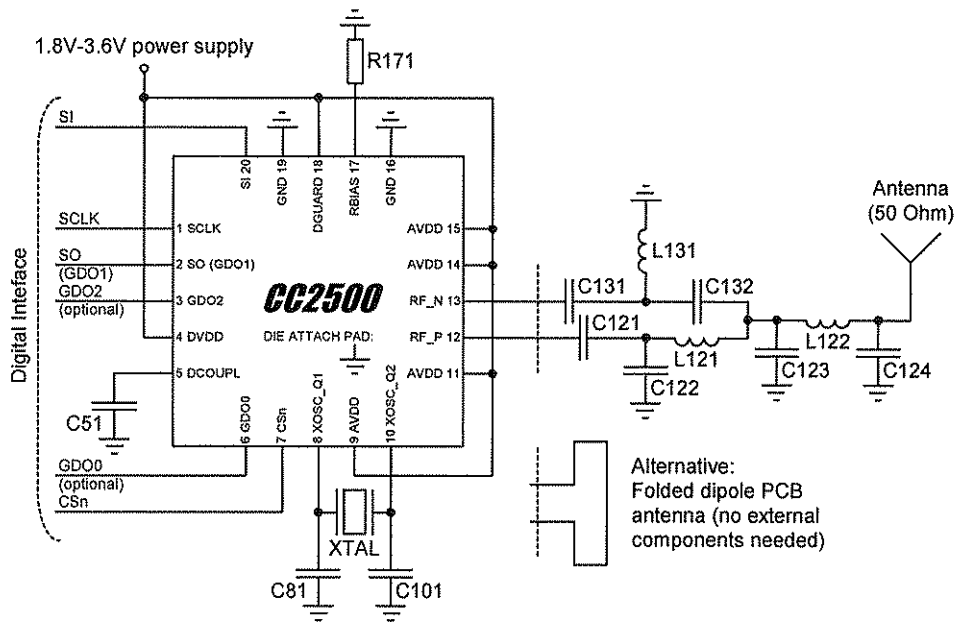


Figure 3: Typical application and evaluation circuit (excluding supply decoupling capacitors)

Component	Value
C51	100 nF ±10%, 0402 X5R
C81	27 pF ±5%, 0402 NP0
C101	27 pF ±5%, 0402 NP0
C121	100 pF ±5%, 0402 NP0
C122	1.0 pF ±0.25 pF, 0402 NP0
C123	1.8 pF ±0.25 pF, 0402 NP0
C124	1.5 pF ±0.25 pF, 0402 NP0
C131	100 pF ±5%, 0402 NP0
C132	1.0 pF ±0.25 pF, 0402 NP0
L121	1.2 nH ±0.3 nH, 0402 monolithic, Murata LQG-15 series
L122	1.2 nH ±0.3 nH, 0402 monolithic, Murata LQG-15 series
L131	1.2 nH ±0.3 nH, 0402 monolithic, Murata LQG-15 series
R171	56 kΩ ±1%, 0402
XTAL	26.0 MHz surface mount crystal

Table 15: Bill Of Materials for the application circuit

In the CC2500EM reference design LQG-15 series inductors from Murata have been used. Measurements have been performed with multi-layer inductors from other manufacturers (e.g. Würth) and the measurement results were the same as when using the Murata part.

8 Configuration Overview

CC2500 can be configured to achieve optimum performance for many different applications. Configuration is done using the SPI interface. The following key parameters can be programmed:

- Power-down / power up mode
- Crystal oscillator power-up / power-down
- Receive / transmit mode
- RF channel selection
- Data rate
- Modulation format
- RX channel filter bandwidth
- RF output power
- Data buffering with separate 64-byte receive and transmit FIFOs
- Packet radio hardware support
- Forward Error Correction with interleaving
- Data Whitening
- Wake-On-Radio (WOR)

Details of each configuration register can be found in Section 31, starting on page 49.

Figure 4 shows a simplified state diagram that explains the main *CC2500* states, together with typical usage and current consumption. For detailed information on controlling the *CC2500* state machine, and a complete state diagram, see Section 19, starting on page 34.

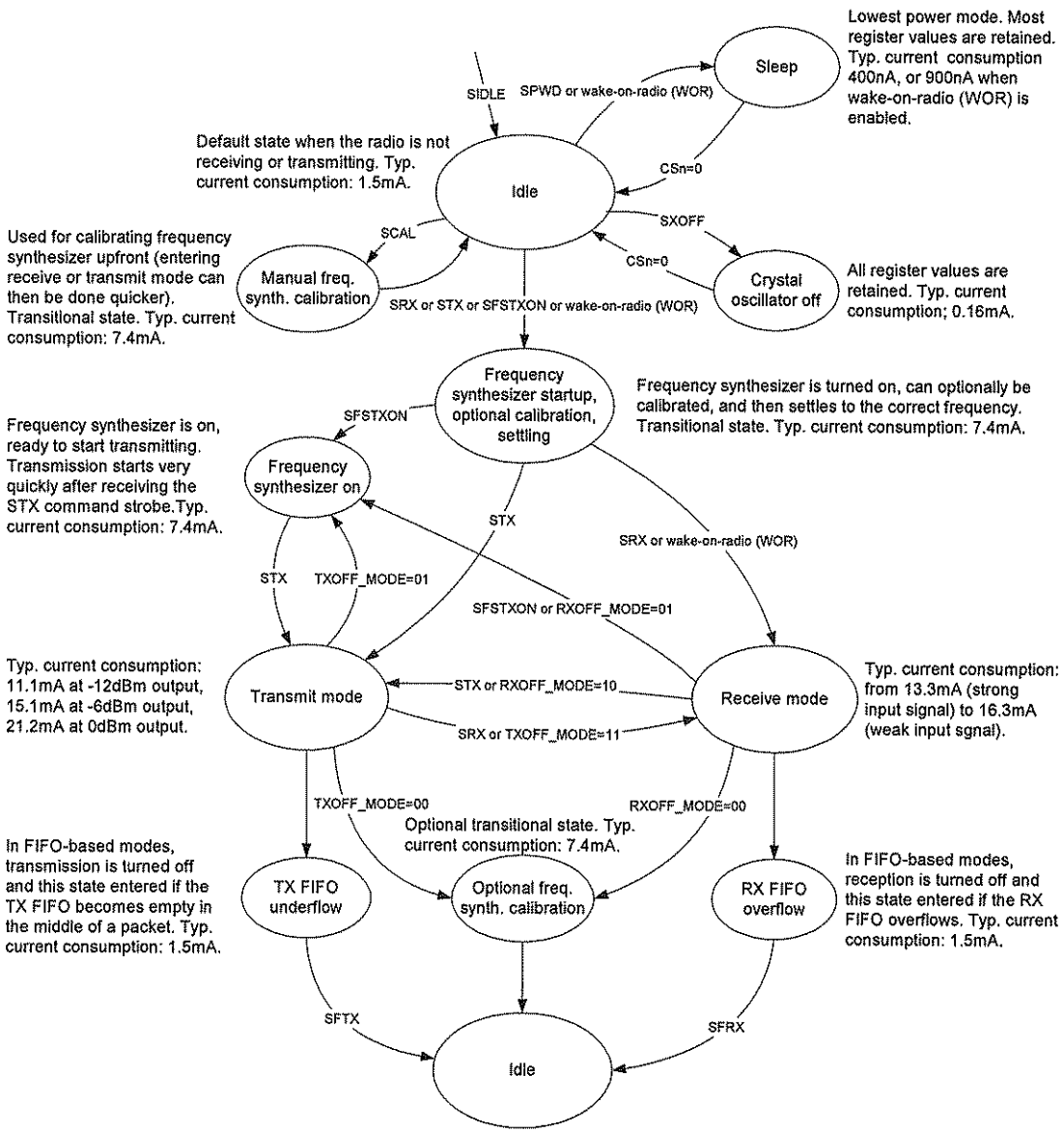


Figure 4: Simplified state diagram, with typical usage and current consumption at 250 kbps data rate and `MDMCFG2.DEM_DCFILT_OFF` = 1 (reduced current)

9 Configuration Software

CC2500 can be configured using the SmartRF® Studio software, available for download from http://www.chipcon.com. The SmartRF® Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality. A screenshot of the SmartRF® Studio user interface for ***CC2500*** is shown in Figure 5.

Channel No.	Frequency (MHz)
1	*2410.0000*
2	*2410.8109*
3	*2411.6218*
4	*2412.4327*
5	*2413.2436*
6	*2414.0545*
7	*2414.8654*
8	*2415.6763*
9	*2416.4872*
10	*2417.2981*
11	*2418.1090*
12	*2418.9199*
13	*2419.7308*
14	*2420.5417*
15	*2421.3526*
16	*2422.1635*
17	*2422.9744*
18	*2423.7853*
19	*2424.5962*
20	*2425.4071*
21	*2426.2180*
22	*2427.0289*
23	*2427.8398*
24	*2428.6507*
25	*2429.4616*
26	*2430.2725*
27	*2431.0834*
28	*2431.8943*
29	*2432.7052*
30	*2433.5161*
31	*2434.3270*
32	*2435.1379*
33	*2435.9488*
34	*2436.7597*
35	*2437.5706*
36	*2438.3815*
37	*2439.1924*
38	*2440.0033*
39	*2440.8142*
40	*2441.6251*
41	*2442.4360*
42	*2443.2469*
43	*2444.0578*
44	*2444.8687*
45	*2445.6796*

RF output power:*1dBm*

Frequency range of operation:*2440MHz~2470MHz*

Type of modulation:*MSK*

Type of antenna joint:*single-ended monopole PCB antenna*

Channel separation:*810.9KHz*

The channels in red color are the synchronous channels

46	*2446.4905*
47	*2447.3014*
48	*2448.1123*
49	***2448.9232***
50	*2449.7341*
51	*2450.5450*
52	*2451.3559*
53	*2452.1668*
54	*2452.9777*
55	*2453.7886*
56	*2454.5995*
57	*2455.4104*
58	*2456.2213*
59	*2457.0322*
60	*2457.8431*
61	*2458.6540*
62	*2459.4649*
63	*2460.2758*
64	*2461.0867*
65	*2461.8976*
66	*2462.7085*
67	*2463.5194*
68	*2464.3303*
69	*2465.1412*
70	*2465.9521*
71	*2466.7630*
72	*2467.5739*
73	*2468.3848*
74	*2469.1957*
75	*2470.0066*

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