System Overview

The revolutionary MT6219 is a leading edge single-chip solution for GSM/GPRS mobile phones targeting the emerging applications in digital audio and video. Based on 32-bit ARM7EJ-S™ RISC processor, MT6219 not only features high performance GPRS Class 12 MODEM, but also provides comprehensive and advanced solutions for handheld multi-media.

Typical application is shown in **Figure** 1.

Multi-media Subsystem

The MT6219 multi-media subsystem provides connection to CMOS image sensor and supports resolution up to 1.3M pixels. With its advanced image signal and data processing technology, MT6219 allows efficient processing of image and video data. It also has built-in JPEG CODEC and MPEG-4 CODEC, thus enabling real-time creation and playback of high-quality images and video. In addition to advanced image and video features, MT6219 also utilizes high resolution DAC, digital audio, and audio synthesis technology to provide superior audio features for all future multi-media needs.

In order to provide more flexibility and bandwidth for multi-media products, an additional 8-bit parallel interface is incorporated. This interface enables connection to LCD panels as well as connection to NAND flash devices to allow for multi-media data storage capabilities.

External Memory Interface

Providing the greatest capacity for expansion, MT6219 supports up to 8 state-of-the-art devices through its 16-bit host interface. Devices such as burst/page mode Flash, page mode SRAM, Pseudo SRAM, Color/Parallel LCD, and multi-media companion chip are all supported through this interface. To minimize power consumption and ensure low noise, this interface is designed for flexible I/O voltage and allows lowering of supply voltage down to 1.8V. The driving strength is configurable for signal integrity adjustment. The data bus also employs retention technology to prevent the bus from floating during turn over.

User Interface

To provide complete user interface, MT6219 brings together all the necessary peripheral blocks for multi-media GSM/GPRS phone. The peripheral blocks consists of the Keypad Scanner with the capability to detect multiple key presses, SIM Controller, Alerter, Real Time Clock, PWM, Serial LCD Controller, and General Purpose Programmable I/Os. For connectivity and data storage, the MT6219 supports UART, IrDA, USB 1.1 Slave and MMC/SD/MS/MS Pro. Furthermore, for large amount of data transfer, high performance DMA (Direct Memory Access) and hardware flow control are implemented, which greatly enhances the performance and reduces MCU processing load.

Audio Interface

Using a highly integrated mixed-signal Audio Front-End, the MT6219 architecture allows for easy audio interfacing with direct connection to the audio transducers. The audio interface integrates D/A and A/D Converters for Voice band, as well as high resolution Stereo D/A Converters for Audio band. In addition, MT6219 also provides Stereo Input and Analog Mux. Overall, MT6219's audio features provide a rich platform for multi-media applications.

Radio Interface

MT6219 integrates a mixed-signal Baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. It contains gain and offset calibration mechanisms, and filters with programmable coefficients for comprehensive compatibility control on RF modules. This approach also allows the usage of a high resolution D/A Converter for controlling VCXO or crystal, thus reducing the need for expensive TCVCXO. MT6219 achieves great MODEM performance by utilizing 14-bit high resolution A/D Converter in the RF downlink path. Furthermore, to reduce the need for extra external current-driving component, the driving strength of some BPI outputs is designed to be configurable.

Debug Function

The JTAG interface enables in-circuit debugging of software program with the ARM7EJ-S core. With this standardized debugging interface, the MT6219 provides developers with a wide set of options in choosing ARM development kits from different third party vendors.

Power Management

The MT6219 offers various low-power features to help reduce system power consumption. These features include Pause Mode of 32KHz clocking at Standby State, Power Down Mode for individual peripherals, and Processor Sleep Mode. In addition, MT6219 is also fabricated in advanced low leakage CMOS process, hence providing an overall ultra low leakage solution.

Package

The MT6219 device is offered in a 13mm×13mm, 293-ball, 0.65 mm pitch, TFBGA package.

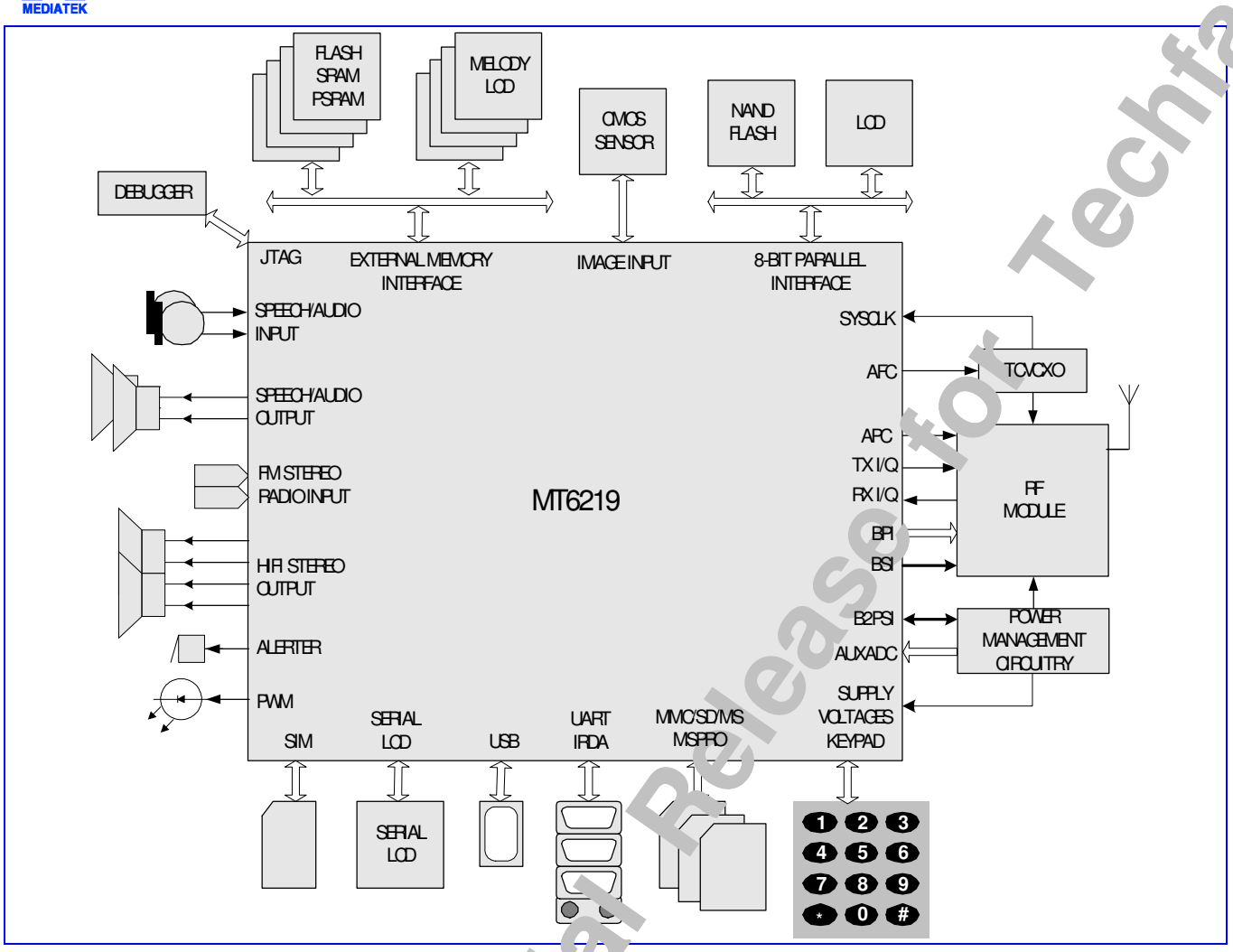

Figure 1 Typical application of MT6219

MODEM Features

- **General**
  - Integrated voice-band, audio-band and base-band analog front ends
  - TFBGA 13mm×13mm, 293-ball, 0.65 mm pitch package
- **MCU Subsystem**
  - ARM7EJ-S 32-bit RISC processor
  - High performance multi-layer AMBA bus
  - Java hardware acceleration for fast Java-based games and applets
  - Operating frequency: 26/52 MHz
  - Dedicated DMA bus
  - 14 DMA channels
  - 512K Bytes zero-wait-state on-chip SRAM
  - On-chip boot ROM for Factory Flash Programming
  - Watchdog timer for system crash recovery
  - 2 sets of General Purpose Timer
  - Circuit Switch Data coprocessor
  - Division coprocessor
- **External Memory Interface**
  - Supports up to 8 external devices
  - Supports 8-bit or 16-bit memory components with maximum size of up to 64M Bytes each
  - Supports Flash and SRAM with Page Mode or Burst Mode
  - Supports Pseudo SRAM
  - Industry standard Parallel LCD Interface
  - Supports multi-media companion chips with 8/16 bits data width
  - Flexible I/O voltage of 1.8V ~ 2.8V for memory interface
  - Configurable driving strength for memory interface
- **Audio and Modem CODEC**
  - Dial tone generation
  - Voice Memo
  - Noise Reduction
  - Echo Suppression
  - Advanced Sidetone Oscillation Reduction
  - Digital sidetone generator with programmable gain
  - Two programmable acoustic compensation filters
  - GSM/GPRS quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1 and A5/2 ciphering
  - GPRS GEA and GEA2 ciphering
  - Programmable GSM/GPRS Modem
  - Packet Switched Data with CS1/CS2/CS3/CS4 coding schemes
  - GSM Circuit Switch Data
  - GPRS Class 12
- **User Interfaces**
  - 6-row × 7-column keypad controller with hardware scanner
  - Supports multiple key presses for gaming
  - SIM/USIM Controller with hardware T=0/T=1 protocol control
  - 3 UARTs with hardware flow control and speed up to 921600 bps
  - IrDA modulator/demodulator with hardware framer

- Real Time Clock (RTC) operating with a separate power supply
- Serial LCD Interface with 8/9 bit format support
- General Purpose I/Os (GPIOs)
- 2 Sets of Pulse Width Modulation (PWM) Output
- Alerter Output with Enhanced PWM or PDM
- Six external interrupt lines

■ **Audio Interface and Audio Front End**

- Two microphone inputs sharing one low noise amplifier with programmable gain
- Two Voice power amplifiers with programmable gain
- 2nd order Sigma-Delta A/D Converter for voice uplink path
- D/A Converter for voice downlink path
- Supports half-duplex hands-free operation
- Compliant with GSM 03.50

■ **Radio Interface and Baseband Front End**

- GMSK modulator with analog I and Q channel outputs
- 10-bit D/A Converter for uplink baseband I and Q signals
- 14-bit high resolution A/D Converter for downlink baseband I and Q signals
- Calibration mechanism of offset and gain mismatch for baseband A/D Converter and D/A Converter
- 10-bit D/A Converter for Automatic Power Control
- 13-bit high resolution D/A Converter for Automatic Frequency Control
- Programmable Radio RX filter
- 2 Channels Baseband Serial Interface (BSI) with 3-wire control
- 10-Pin Baseband Parallel Interface (BPI) with programmable driving strength
- Multi-band support

■ **Power Management**

- Power Down Mode for analog and digital circuits
- Processor Sleep Mode
- Pause Mode of 32KHz clocking at Standby State
- 7-channel Auxiliary 10-bit A/D Converter for charger and battery monitoring and photo sensing

■ **Test and Debug**

- Built-in digital and analog loop back modes for both Audio and Baseband Front-End
- DAI port complying with GSM Rec.11.10
- JTAG port for debugging embedded MCU

Multi-Media Features

- **LCD/NAND Flash Interface**
  - Dedicated 8-bit Parallel Interface, supports up to 3 external devices
  - Hardware accelerated LCD Controller for display
  - Dedicated LCD bus
  - NAND Flash Controller for mass storages
- **LCD Controller**
  - Supports simultaneous connection to up to 2 parallel LCD and 1 serial LCD panels
  - Supports format: RGB332, RGB444, RGB565, RGB666, RGB888
  - Supports LCD panel maximum resolution up to 800x600 at 16bpp
  - Supports hardware display rotation
  - Capable of combining display memories with up to 4 blending layers
- **Image Signal Processor**
  - 8/10 bit Bayer format image input
  - Capable of processing image of size up to 1.3M pixels
  - Color Correction Matrix
  - Gamma Correction
  - Automatic Exposure Control
  - Automatic White Balance Control
  - Programmable AE/AWB windows
  - Edge Enhancement Support
  - Histogram Equalization Logic
  - Horizontal and Vertical Sync Information on Separate Pin
- **JPEG Decoder**
  - ISO/IEC 10918-1 JPEG Baseline and Progressive modes
  - Supports all possible YUV formats, including grayscale format
  - Supports all DC/AC Huffman table parsing
  - Supports all quantization table parsing
  - Supports restart interval
  - Supports SOS, DHT, DQT and DRI marker parsing
  - IEEE Std 1180-1990 IDCT Standard Compliant
  - Supports progressive image processing to minimize storage space requirement
  - Supports reload-able DMA for VLD stream
- **JPEG Encoder**
  - ISO/IEC 10918-1 JPEG baseline mode
  - ISO/IEC 10918-2 Compliance
  - Supports YUV422 and grayscale formats
  - Standard DC and AC Huffman tables
  - Provides 4 levels of encode quality
- **Image Data Processing**
  - High throughput hardware Resizer capable of tailoring image to arbitrary size
  - Horizontal scaling in averaging method
  - Vertical scaling in bilinear method
  - Simultaneous scaling for MPEG-4 encode and LCD display
  - YUV and RGB color space conversion
  - Pixel format transform
  - Boundary padding
  - Pixel processing: hue/saturation/intensity/color adjustment, Gamma correction and grayscale/invert/sepia-tone effects
  - Programmable Spatial Filtering: Linear filter, Non-linear filter and Multi-pass artistic effects

- Hardware accelerated image editing

MPEG-4/H.263 CODEC

- Hardware Video CODEC
- ISO/IEC 14496-2 simple profile:

  decode @ level 0/1/2/3

  encode @ level 0
- Supported visual tools for decoder: I-VOP, P-VOP, AC/DC prediction, 4-MV, Unrestricted MV, Error Resilience, Short Header
- Error Resilience for decoder: Slice Resynchronization, Data Partitioning, Reversible VLC
- Supported visual tools for encoder: I-VOP, P-VOP, Half-pel, DC prediction, Unrestricted MV, Reversible VLC, Short Header
- Supports encoding motion vector of range up to –64/+63.5 pixels
- ITU-T H.263 profile 0 @ level 10
- AAC/AMR/WB-AMR audio decode support
- AMR/WB-AMR audio encode support

2D Accelerator

- Rectangle fill
- BitBlt: multi-BitBlt without transform, 7 rotate, mirror (transparent) BitBlt
- Alpha blending
- Line drawing: normal line, dotted line
- Font caching: normal font, Italic font
- Supports 16-bpp RGB565 and 8-bpp index color modes
- Command queue with 32 levels

Audio CODEC

- Wavetable synthesis with up to 64 tones
- Advanced wavetable synthesizer capable of generating simulated stereo
- Wavetable including GM full set of 128 instruments and 47 sets of percussions
- PCM Playback and Record
- Digital Audio Playback
- High resolution D/A Converters for Stereo Audio playback
- Stereo analog input for stereo audio source
- Analog mixers for Stereo Audio
- Stereo to Mono Conversion

Connectivity

- Full-speed USB 1.1 Device
- Multi Media Card/Secure Digital Memory Card/Memory Stick/Memory Stick Pro host controller

General Description

Figure 2 details the block diagram of MT6219. Based on a dual-processor architecture, MT6219 integrates both an ARM7EJ-S core and a digital signal processor core. ARM7EJ-S is the main processor that is responsible for running high-level GSM/GPRS protocol software as well as multi-media applications. The digital signal processor handles the low-level MODEM as well as advanced audio functions. Except for some mixed-signal circuitries, the other building blocks in MT6219 are connected to either the microcontroller or the digital signal processor.

Specifically, MT6219 consists of the following subsystems:

- Microcontroller Unit (MCU) Subsystem - includes an ARM7EJ-S RISC processor and its accompanying memory management and interrupt handling logics.
- Digital Signal Processor (DSP) Subsystem - includes a DSP and its accompanying memory, memory controller, and interrupt controller.
- MCU/DSP Interface - where the MCU and the DSP exchange hardware and software information.
- Microcontroller Peripherals - includes all user interface modules and RF control interface modules.
- Microcontroller Coprocessors - runs computing-intensive processes in place of Microcontroller.
- DSP Peripherals - hardware accelerators for GSM/GPRS channel codec.
- Multi-media Subsystem - integrates several advanced accelerators to support multi-media applications.
- Voice Front End - the data path for converting analog speech from and to digital speech.
- Audio Front End - the data path for converting stereo audio from stereo audio source
- Baseband Front End - the data path for converting digital signal from and to analog signal of RF modules.
- Timing Generator - generates the control signals related to the TDMA frame timing.
- Power, Reset and Clock subsystem - manages the power, reset, and clock distribution inside MT6219.

Details of the individual subsystems and blocks are described in following Chapters.

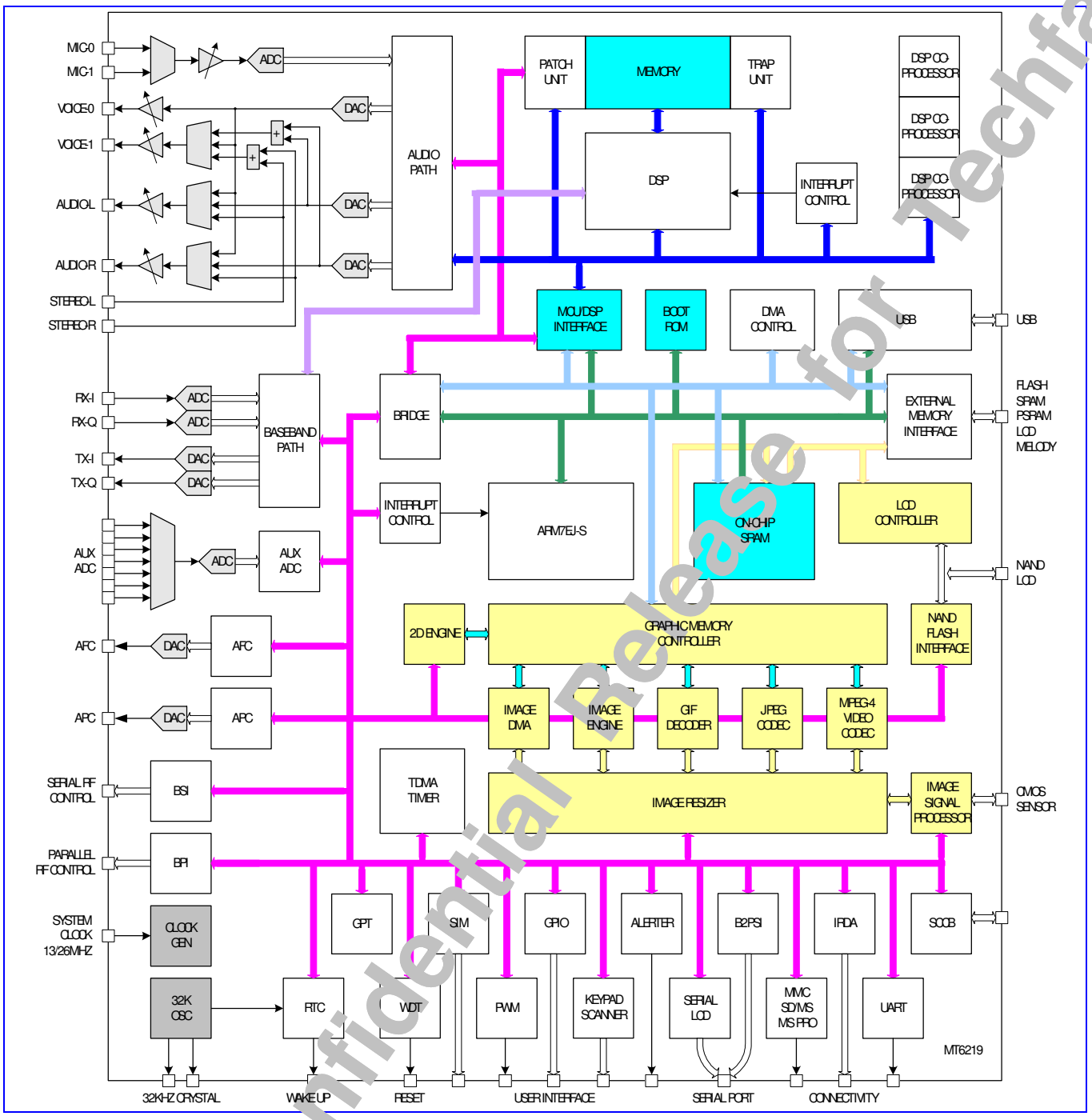

Figure 2 MT6219 block diagram.