The transmitter output power should meet 3GPP Specification.
The maximum output power should be setting PCL 0 for Power Class 1 device in PCS 1900 Band. The maximum output power of this device is 29.5dBm +/- 1 dB.
The device uses MTK chipset called MT6219, and all settings of RF parameter descript in this chapter.

Radio Interface Control

This chapter details the MT6219 interface control with the radio part of a GSM terminal. Providing a comprehensive control scheme, the MT6219 radio interface consists of Baseband Serial Interface (BSI), Baseband Parallel Interface (BPI), Automatic Power Control (APC) and Automatic Frequency Control (AFC) together with APC-DAC and AFC-DAC.

Base-band Serial Interface

The Base-band Serial Interface is used to control the external radio components. It utilizes a 3-wire serial bus to transfer data to RF circuitry for PLL frequency change, reception gain setting, and other radio control purposes. In this unit, BSI data registers are double-buffered in the same way as the TDMA event registers. The user writes data into the write buffer and the data is transferred from the write buffer to the active buffer when TDMA_EVTVAL signal from the TDMA timer is pulsed.

Each data register BSI_D*n*_DAT is associated with one data control register BSI_D*n*_CON, where *n* denotes the index. The data control register with index *n* used to identify which events (signaled by TDMA_BSISTR*n*) generated by the TDMA timer would trigger the download process of the word in register BSI_D*n*_DAT through the serial bus, as well as the length of the word in length of bits. A special event is defined. The event is triggered by the operation that the user writes 1 to the IMOD flag. It provides immediate download process without programming the TDMA timer.

If more than one data word is to be downloaded on the same BSI event, the word with the lowest address among them will be downloaded first, followed by the next lowest and so on.

The total time to download the words depends on the word length, the number of words to download, and the clock rates. The programmer should space the successive event to provide enough time. If the download process of the previous event isn't complete before the new events come, the later will be suppressed.

The unit supports 2 external components. There are four output pins. BSI_CLK is the output clock, BSI_DATA is the serial data port, and BSI_CS0 and BSI_CS1 are the select pins for the 2 components, respectively. BSI_CS1 is multiplexed with other function. Please refer to GPIO table for more detail.

The block diagram of the BSI unit is as depicted in **Figure 67**.

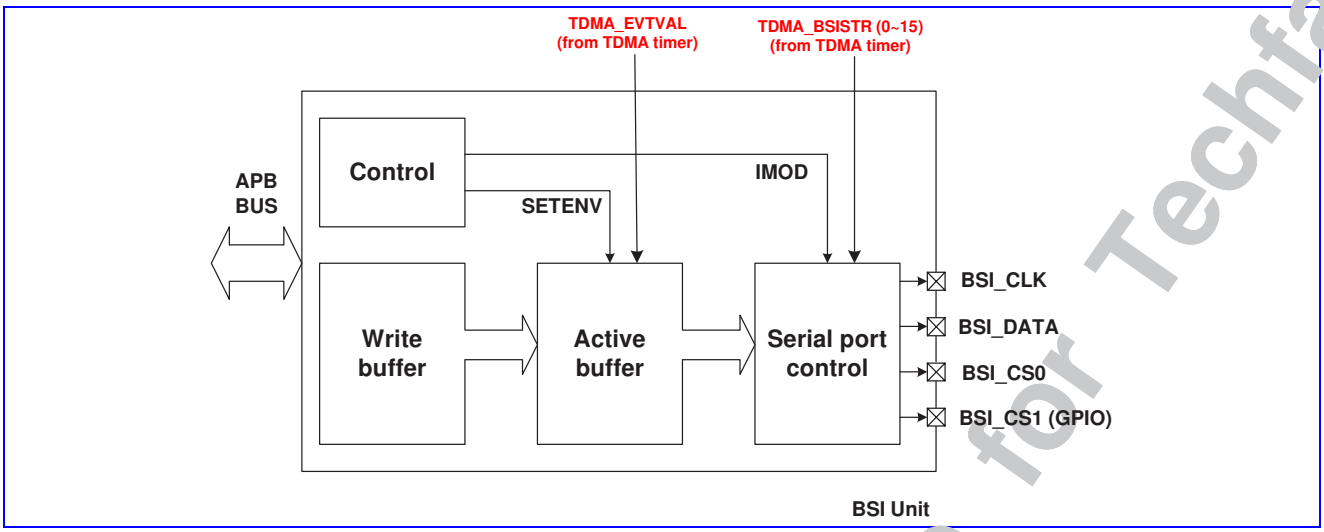

Figure 67 Block diagram of BSI unit.

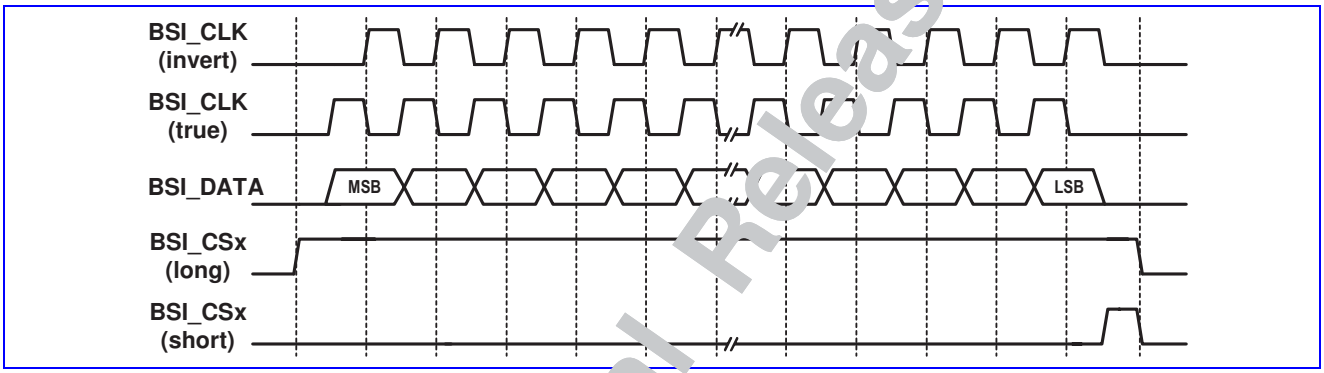

Figure 68 Timing characteristic of BSI interface

Register Definitions

BSI+0000h BSI control register BSI_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SETENV	EN1_POL	EN1_LEN	EN0_POL	EN0_LEN	IMOD	CLK_SPD		CLK_POL
Type								R/W	R/W	R/W	R/W	R/W	WO	R/W		R/W
Reset								0	0	0	0	0	N/A	0		0

This register is the control register of the BSI unit. It controls the signal type of the 3-wire interface.

CLK_POL The flag controls the polarity of BSI_CLK. Refer to **Figure 68**.

0 True clock polarity

1 Inverted clock polarity

CLK_SPD The field defines the clock rate of BSI_CLK. The 3-wire interface provides 4 choices of data bit rate. The default is 13/2 MHz.

00 13/2 MHz

01 13/4 MHz

10 13/6 MHz

11 13/8 MHz

IMOD The field enables the immediate mode. If the user writes 1 to the flag, the download will be triggered immediately without waiting for the timer events. The words in which the event ID equals to 1Fh will be downloaded following this signal. This flag is write-only. The immediate write can be exercised once. That means the programmer should write the flag again to start another immediate download. Setting the flag won't disable the other events from the timer. In case it's required to turn off all the events, the programmer can disable them by setting BSI_ENA to all zero.

ENX_LEN The field controls the type of the signal BSI_CS0 and BSI_CS1. Refer to **Figure 68**.

0 Long enable pulse

1 Short enable pulse

ENX_POL The field controls the polarity of the signal BSI_CS0 and BSI_CS1.

0 True enable pulse polarity

1 Inverted enable pulse polarity

SETENV The flag enables the write operation of the active buffer.

0 The user writes to the write buffer. The data is then latched in the active buffer after TDMA_EVTVAL is pulsed

1 The user directly write data to the active buffer.

BSI+0004h Control part of data register 0 BSI_D0_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISB			LEN								EVT_ID				
Type	R/W			R/W								R/W				

This register is the control part of the data register 0. It decides the required length of the download data word, the event to trigger the download process of the word, and which device it targets.

There are 26 data registers of this type as listed in **Table 41**.

EVT_ID This field stores the event ID that the data word is due to be downloaded.

00000~01111 Synchronously download of the word with the selected EVT_ID event. The match between this field and the event is listed as **Table 6**.

Event ID (in binary) – EVT_ID	Event name
00000	TDMA_BSISTR0
00001	TDMA_BSISTR1
00010	TDMA_BSISTR2
00011	TDMA_BSISTR3
00100	TDMA_BSISTR4
00101	TDMA_BSISTR5
00110	TDMA_BSISTR6
00111	TDMA_BSISTR7
01000	TDMA_BSISTR8
01001	TDMA_BSISTR9
01010	TDMA_BSISTR10

01011	TDMA_BSISTR11
01100	TDMA_BSISTR12
01101	TDMA_BSISTR13
01110	TDMA_BSISTR14
01111	TDMA_BSISTR15

Table 40 The match between the value of EVT_ID field in the BSI control registers and the TDMA_BSISTR events.

10000~11110 Reserved

11111 Immediate download

LEN The field stores the length of the data word. The actual length is defined as LEN + 1 in units of bits. The value ranges from 0 to 31, corresponding to 1 to 32 bits in length.

ISB The flag selects the target device.

0 Device 0 is selected.

1 Device 1 is selected.

BSI +0008h Data part of data register 0 BSI_D0_DAT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT [31:16]															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT [15:0]															
Type	R/W															

This register is the data part of the data register 0. The illegal length of the data is up to 32 bits. The actual number of bits to be transmitted is specified in LEN field in BSI_D0_CON register.

DAT The field signifies the data part of the data register.

There are in total 26 pairs of data registers. The address mapping and function is listed as

Register Address	Register Function	Acronym
BSI +0004h	Control part of data register 0	BSI_D0_CON
BSI +0008h	Data part of data register 0	BSI_D0_DAT
BSI +000Ch	Control part of data register 1	BSI_D1_CON
BSI +0010h	Data part of data register 1	BSI_D1_ DAT
BSI +0014h	Control part of data register 2	BSI_D2_CON
BSI +0018h	Data part of data register 2	BSI_D2_ DAT
BSI +001Ch	Control part of data register 3	BSI_D3_CON
BSI +0020h	Data part of data register 3	BSI_D3_ DAT
BSI +0024h	Control part of data register 4	BSI_D4_CON
BSI +0028h	Data part of data register 4	BSI_D4_ DAT
BSI +002Ch	Control part of data register 5	BSI_D5_CON
BSI +0030h	Data part of data register 5	BSI_D5_ DAT
BSI +0034h	Control part of data register 6	BSI_D6_CON
BSI +0038h	Data part of data register 6	BSI_D6_ DAT
BSI +003Ch	Control part of data register 7	BSI_D7_CON

BSI +0040h	Data part of data register 7	BSI_D7_ DAT
BSI +0044h	Control part of data register 8	BSI_D8_CON
BSI +0048h	Data part of data register 8	BSI_D8_ DAT
BSI +004Ch	Control part of data register 9	BSI_D9_CON
BSI +0050h	Data part of data register 9	BSI_D9_ DAT
BSI +0054h	Control part of data register 10	BSI_D10_CON
BSI +0058h	Data part of data register 10	BSI_D10_ DATA
BSI +005Ch	Control part of data register 11	BSI_D11_CON
BSI +0060h	Data part of data register 11	BSI_D11_ DAT
BSI +0064h	Control part of data register 12	BSI_D12_CON
BSI +0068h	Data part of data register 12	BSI_D12_ DAT
BSI +006Ch	Control part of data register 13	BSI_D13_CON
BSI +0070h	Data part of data register 13	BSI_D13_ DAT
BSI +0074h	Control part of data register 14	BSI_D14_CON
BSI +0078h	Data part of data register 14	BSI_D14_ DAT
BSI +007Ch	Control part of data register 15	BSI_D15_CON
BSI +0080h	Data part of data register 15	BSI_D15_ DAT
BSI +0084h	Control part of data register 16	BSI_D16_CON
BSI +0088h	Data part of data register 16	BSI_D16_ DAT
BSI +008Ch	Control part of data register 17	BSI_D17_CON
BSI +0090h	Data part of data register 17	BSI_D17_ DAT
BSI +0094h	Control part of data register 18	BSI_D18_CON
BSI +0098h	Data part of data register 18	BSI_D18_ DAT
BSI +009Ch	Control part of data register 19	BSI_D19_CON
BSI +00A0h	Data part of data register 19	BSI_D19_ DAT
BSI +00A4h	Control part of data register 20	BSI_D20_CON
BSI +00A8h	Data part of data register 20	BSI_D20_ DAT
BSI +00ACh	Control part of data register 21	BSI_D21_CON
BSI +00B0h	Data part of data register 21	BSI_D21_ DAT
BSI +00B4h	Control part of data register 22	BSI_D22_CON
BSI +00B8h	Data part of data register 22	BSI_D22_ DAT
BSI +00BCh	Control part of data register 23	BSI_D23_CON
BSI +00C0h	Data part of data register 23	BSI_D23_ DAT
BSI +00C4h	Control part of data register 24	BSI_D24_CON
BSI +00C8h	Data part of data register 24	BSI_D24_ DAT
BSI +00CCh	Control part of data register 25	BSI_D25_CON
BSI +00D0h	Data part of data register 25	BSI_D25_ DAT

Table 41 BSI data registers

BSI +0190h BSI event enable register BSI_ENA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI15	BSI14	BSI13	BSI12	BSI11	BSI10	BSI9	BSI8	BSI7	BSI6	BSI5	BSI4	BSI3	BSI2	BSI1	BSI0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

This register could enable the event by setting the corresponding bit. After hardware reset, all bits are initialized as 1. These bits are set as 1 after TDMA_EVTVAL is pulsed.

BSIx The flag enables the downloading of the words that corresponds to the events signaled by TMDA_BSI.

0 The event is not enabled.

1 The event is enabled.

Base-band Parallel Interface

General description

The Base-band Parallel Interface features 10 control pins, which is used for timing-critical external circuits. These pins are typically used to control front-end components which should be turned on/off at the specified time along the GSM time-base, such as transmit-enable, band switching, TR-switch, and so on.

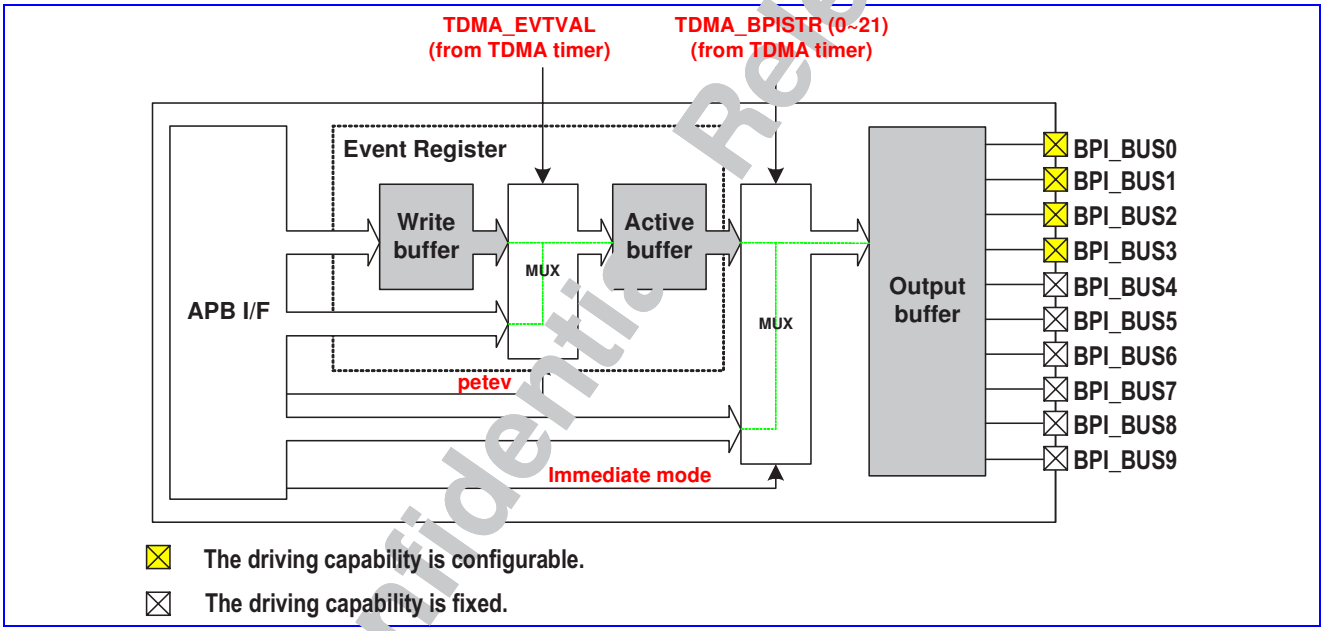

Figure 69 Block diagram of BPI interface

The user could program 22 sets of 10-bit register to set the output value of BPI_BUS0~BPI_BUS9. The data will be stored in the write buffers. Those are then forwarded to the active buffers when TDMA_EVTVAL signal, usually once in one frame, is pulsed. There are 22 corresponding write buffers and active buffer, as well as the TDMA events.

Each TDMA_BPISTR event triggers the transfer of the data in the corresponding active buffer to the output buffer, thus changing the value of the BPI bus. The user can disable the events by programming the enable registers in the TDMA timer.

If the TDMA_BPISTR event is disabled, the corresponding signal TDMA_BPISTR will not be pulsed, and the value on the BPI bus will remain unchanged.

For applications in which BPI signals serve as the switch, typically some current-driving components are added to enhance the driving capability. We provide 4 configurable output pins, which provide current up to 8mA. It's intended to reduce the number of the external components.

The output pins BPI_BUS6, BPI_BUS7, BPI_BUS8, and BPI_BUS9 are multiplexed with GPIO. Please refer to the GPIO table for more detailed information.

Register Definitions

BPI+0000h BPI control register BPI_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**PINM3**	**PINM2**	**PINM1**	**PINM0**	**PETEV**
Type												WO	WO	WO	WO	R/W
Reset												0	0	0	0	0

The register is the control register of the BPI unit. It controls the direct access mode of the active buffer and the current driving capability for the output pins.

The driving capability of BPI_BUS0, BPI_BUS1, BPI_BUS2, and BPI_BUS3 can be 2mA or 8mA, determined by the value of PINM0, PINM1, PINM2, and PINM3, respectively. This provides higher driving capability and can save some external current-driving components. Aside from those configurable pins, the driving capability of BPI_BUS4, BPI_BUS5, BPI_BUS6, and BPI_BUS7 is fixed as 2mA.

PETEV The flag is used to enable the direct access to the active buffer.

- **0** The user writes data to the write buffer. The data is latched in the active buffer after the TDMA_EVTVAL signal is pulsed.
- **1** The user directly writes data to the active buffer without waiting for the TDMA_EVTVAL signal.

PINM0 The field controls the driving capability of BPI_BUS0.

- **0** The output driving capability is 2mA.
- **1** The output driving capability is 8mA.

PINM1 The field controls the driving capability of BPI_BUS1.

- **0** The output driving capability is 2mA.
- **1** The output driving capability is 8mA.

PINM2 The field controls the driving capability of BPI_BUS2.

- **0** The output driving capability is 2mA.
- **1** The output driving capability is 8mA.

PINM3 The field controls the driving capability of BPI_BUS3.

- **0** The output driving capability is 2mA.
- **1** The output driving capability is 8mA.

BPI +0004h BPI data register 0 BPI_BUF0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**PO9**	**PO8**	**PO7**	**PO6**	**PO5**	**PO4**	**PO3**	**PO2**	**PO1**	**PO0**
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The register defines the BPI signals that are associated with the event TDMA_BPI0.

There are 22 registers of the same type as listed in **Table 42**. Each register is associated with one specific event signal from the TDMA timer. The data registers are all double-buffered. When PETEV is set to be 0, the data register links to the write buffer. When PETEV is set to be 1, the data register links to the active buffer.

There is one register BPI_BUFI dedicated to be used in immediate mode. Writing the value to that register change the BPI signals at once. The immediate mode provides an immediate operation on the programming of the BPI bus.

POx The flag defines the corresponding signals for BPIx after the TDMA event 0 takes place.

The overall data register definition is listed in **Table 42**.

Register Address	Register Function	Acronym
BPI +0004h	BPI pin data for event TDMA_BPI 0	BPI_BUF0
BPI +0008h	BPI pin data for event TDMA_BPI 1	BPI_BUF1
BPI +000Ch	BPI pin data for event TDMA_BPI 2	BPI_BUF2
BPI +0010h	BPI pin data for event TDMA_BPI 3	BPI_BUF3
BPI +0014h	BPI pin data for event TDMA_BPI 4	BPI_BUF4
BPI +0018h	BPI pin data for event TDMA_BPI 5	BPI_BUF5
BPI +001Ch	BPI pin data for event TDMA_BPI 6	BPI_BUF6
BPI +0020h	BPI pin data for event TDMA_BPI 7	BPI_BUF7
BPI +0024h	BPI pin data for event TDMA_BPI 8	BPI_BUF8
BPI +0028h	BPI pin data for event TDMA_BPI 9	BPI_BUF9
BPI +002Ch	BPI pin data for event TDMA_BPI 10	BPI_BUF10
BPI +0030h	BPI pin data for event TDMA_BPI 11	BPI_BUF11
BPI +0034h	BPI pin data for event TDMA_BPI 12	BPI_BUF12
BPI +0038h	BPI pin data for event TDMA_BPI 13	BPI_BUF13
BPI +003Ch	BPI pin data for event TDMA_BPI 14	BPI_BUF14
BPI +0040h	BPI pin data for event TDMA_BPI 15	BPI_BUF15
BPI +0044h	BPI pin data for event TDMA_BPI 16	BPI_BUF16
BPI +0048h	BPI pin data for event TDMA_BPI 17	BPI_BUF17
BPI +004Ch	BPI pin data for event TDMA_BPI 18	BPI_BUF18
BPI +0050h	BPI pin data for event TDMA_BPI 19	BPI_BUF19
BPI +0054h	BPI pin data for event TDMA_BPI 20	BPI_BUF20
BPI +0058h	BPI pin data for event TDMA_BPI 21	BPI_BUF21
BPI +005Ch	BPI pin data for immediate mode	BPI_BUFI

Table 42 BPI Data Registers

BPI +0060h BPI event enable register 0 BPI_ENA0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BEN15	BEN14	BEN13	BEN12	BEN11	BEN10	BEN9	BEN8	BEN7	BEN6	BEN5	BEN4	BEN3	BEN2	BEN1	BEN0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The register is used to enable the events that are signaled by the TDMA timer. After hardware reset, all the enable bits defaults to be 1 (enabled). Upon receiving the TDMA_EVTVAL pulse, those bits are also set to 1 (enabled).

BENn The flag controls the function of event n.

0 The event n is disabled.

1 The event n is enabled.

BPI+0064h BPI event enable register 1 BPI_ENA1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											BEN21	BEN20	BEN19	BEN18	BEN17	BEN16
Type											R/W	R/W	R/W	R/W	R/W	R/W
Reset											0	0	0	0	0	0

The register is used to enable the events that are signaled by the TDMA timing generator. After hardware reset, all the enable bits defaults to be 1 (enabled). Upon receiving the TDMA_EVTVAL pulse, those bits are also set to 1 (enabled).

BENn The flag controls the function of event n.

0 The event n is disabled.

1 The event n is enabled.

Automatic Power Control (APC) Unit

General description

Automatic Power Control unit is used to control the Power Amplifier (PA) module. Through APC unit, we can set the proper transmit power level of the handset and ensure that the burst power ramping requirements are met. In one TDMA frame, up to 7 TDMA events can be enabled to support multi-slot transmission. In practice, 5 banks of ramp profiles are used in one frame to make up 4 consecutive transmission slots.

The shape and magnitude of the ramp profiles are configurable to fit ramp-up (ramp up from zero), intermediate ramp (ramp between Transmission windows), and ramp-down (ramp down to zero) profiles. Each bank of the ramp profile consists of 16 8-bit unsigned values, which is adjustable for different conditions.

The entries from one bank of the ramp profile are partitioned into two parts, with 8 values in each part. In normal operation, the entries in the left half part are multiplied by a 10-bit left scaling factor, and the entries in the right half part are multiplied by a 10-bit right scaling factor. Those values are then truncated to form 16 10-bit intermediate values. Finally the intermediate ramp profile are linearly interpolated into 32 10-bit values and sequentially used to update the D/A converter. The block diagram of the APC unit is shown in **Figure 70**.

The APB bus interface is 32 bits wide. It takes 4 write accesses to program each bank of ramp profile. The detail register allocations are listed in **Table 43**.

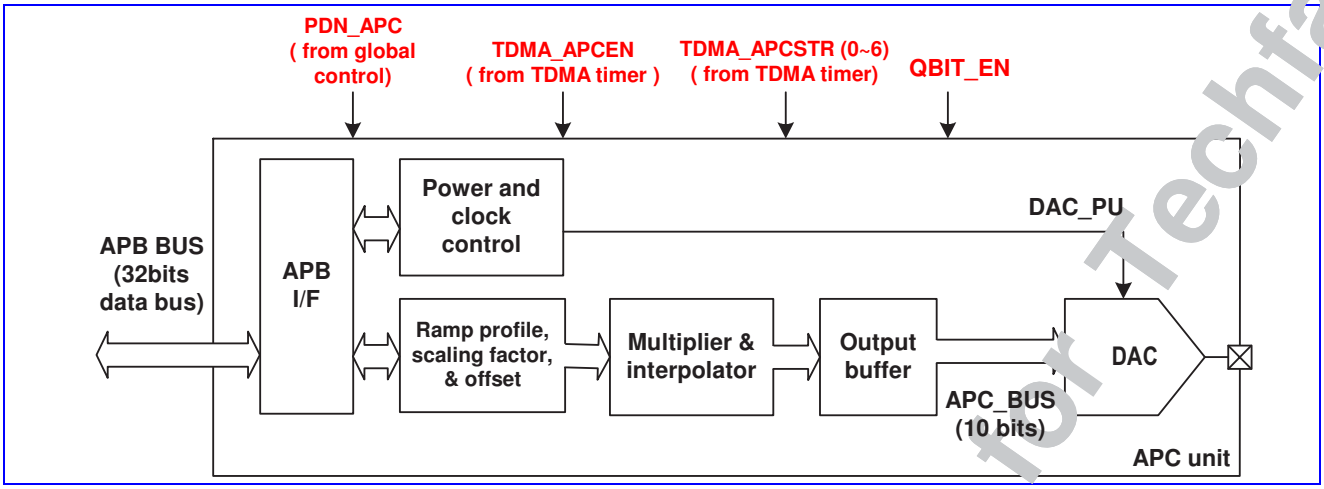

Figure 70 Block diagram of APC unit.

Register Definitions

APC+0000h APC 1st ramp profile #0 APC_PFA0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENT3								ENT2							
Type	R/W								R/W							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENT1								ENT0							
Type	R/W								R/W							

The register stores the first four entries of the first power ramp profile. The first entry resides in the least significant byte [7:0], the second in the second byte [15:8], the third in the third byte [23:16], and the forth in the most significant byte [31:24]. Since this register provides no hardware reset, the programmer should configure it before any APC event takes place.

ENT3 The field signifies the 4th entry of the 1st ramp profile.
ENT2 The field signifies the 3rd entry of the 1st ramp profile.
ENT1 The field signifies the 2nd entry of the 1st ramp profile.
ENT0 The field signifies the 1st entry of the 1st ramp profile.

The overall ramp profile register definition is listed in **Table 43**.

Register Address	Register Function	Acronym
APC +0000h	APC 1st ramp profile #0	APC_PFA0
APC +0004h	APC 1st ramp profile #1	APC_PFA1
APC +0008h	APC 1st ramp profile #2	APC_PFA2
APC +000Ch	APC 1st ramp profile #3	APC_PFA3
APC +0020h	APC 2nd ramp profile #0	APC_PFB0
APC +0024h	APC 2nd ramp profile #1	APC_PFB1
APC +0028h	APC 2nd ramp profile #2	APC_PFB2
APC +002Ch	APC 2nd ramp profile #3	APC_PFB3

APC +0040h	APC 3rd ramp profile #0	APC_PFC0
APC +0044h	APC 3rd ramp profile #1	APC_PFC1
APC +0048h	APC 3rd ramp profile #2	APC_PFC2
APC +004Ch	APC 3rd ramp profile #3	APC_PFC3
APC +0060h	APC 4th ramp profile #0	APC_PFD0
APC +0064h	APC 4th ramp profile #1	APC_PFD1
APC +0068h	APC 4th ramp profile #2	APC_PFD2
APC +006Ch	APC 4th ramp profile #3	APC_PFD3
APC +0080h	APC 5th ramp profile #0	APC_PFE0
APC +0084h	APC 5th ramp profile #1	APC_PFE1
APC +0088h	APC 5th ramp profile #2	APC_PFE2
APC +008Ch	APC 5th ramp profile #3	APC_PFE3
APC +00A0h	APC 6th ramp profile #0	APC_PFF0
APC +00A4h	APC 6th ramp profile #1	APC_PFF1
APC +00A8h	APC 6th ramp profile #2	APC_PFF2
APC +00ACh	APC 6th ramp profile #3	APC_PFF3
APC +00C0h	APC 7th ramp profile #0	APC_PFG0
APC +00C4h	APC 7th ramp profile #1	APC_PFG1
APC +00C8h	APC 7th ramp profile #2	APC_PFG2
APC +00CCh	APC 7th ramp profile #3	APC_PFG3

Table 43 APC ramp profile registers

APC +0010h APC 1st ramp profile left scaling factor APC_SCAL0L

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SCAL									
Type							R/W									
Reset							1_0000_0000									

The register stores the left scaling factor of the 1st ramp profile. This factor multiplies the first 8 entries of the 1st ramp profile to provide the scaled profile, which is then interpolated to control the D/A converter.

After hardware reset, the initial value of the register is 256. In that case, no scaling is done, that is, each entry of the ramp profile is multiplied by 1. That's because the 8 least significant bits will be truncated after multiplication.

The overall scaling factor register definition is listed in **Table 6**.

SF The field is the scaling factor. After hardware reset, the value is 256.

APC +0014h APC 1st ramp profile right scaling factor APC_SCAL0R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SF									
Type							R/W									
Reset							1_0000_0000									

The register stores the right scaling factor of the 1st ramp profile. This factor multiplies the last 8 entries of the 1st ramp profile to provide the scaled profile, which is then interpolated to control the D/A converter.

After hardware reset, the initial value of the register is 256. In that case, no scaling is done, that is, each entry of the ramp profile is multiplied by 1. That's because the 8 least significant bits will be truncated after multiplication.

The overall scaling factor register definition is listed in **Table 6**.

SF The field is the scaling factor. After hardware reset, the value is 256.

APC+0018h APC 1st ramp profile offset value APC_OFFSET0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							OFFSET									
Type							R/W									
Reset							0									

There are 7 offset values for the corresponding ramp profile.

The 1st offset value also serves as the pedestal value. It's used to power up the APC D/A converter before the RF signals start to transmit. The D/A converter is then biased on the value. It's intended to provide initial control voltage of the external control loop. The exact value depends on the characteristics of the external components. The timing to output the pedestal value is configurable through the TDMA_BULCON2 register of the timing generator. It can be set to 0~127 quarter bit time after the base-band D/A converter is powered up.

OFFSET The field stores the offset value for the corresponding ramp profile. After hardware reset, the default value is 0.

The overall offset register definition is listed in **Table 6**.

Register Address	Register Function	Acronym
APC +0010h	APC 1st ramp profile left scaling factor	APC_SCAL0L
APC +0014h	APC 1st ramp profile right scaling factor	APC_SCAL0R
APC +0018h	APC 1st ramp profile offset value	APC_OFFSET0
APC +0030h	APC 2nd ramp profile left scaling factor	APC_SCAL1L
APC +0034h	APC 2nd ramp profile right scaling factor	APC_SCAL1R
APC +0038h	APC 2nd ramp profile offset value	APC_OFFSET1
APC +0050h	APC 3rd ramp profile left scaling factor	APC_SCAL2L
APC +0054h	APC 3rd ramp profile right scaling factor	APC_SCAL2R
APC +0058h	APC 3rd ramp profile offset value	APC_OFFSET2
APC +0070h	APC 4th ramp profile left scaling factor	APC_SCAL3L
APC +0074h	APC 4th ramp profile right scaling factor	APC_SCAL3R
APC +0078h	APC 4th ramp profile offset value	APC_OFFSET3
APC +0090h	APC 5th ramp profile left scaling factor	APC_SCAL4L
APC +0094h	APC 5th ramp profile right scaling factor	APC_SCAL4R
APC +0098h	APC 5th ramp profile offset value	APC_OFFSET4
APC +00B0h	APC 6th ramp profile left scaling factor	APC_SCAL5L
APC +00B4h	APC 6th ramp profile right scaling factor	APC_SCAL5R
APC +00B8h	APC 6th ramp profile offset value	APC_OFFSET5
APC +00D0h	APC 7th ramp profile left scaling factor	APC_SCAL6L
APC +00D4h	APC 7th ramp profile right scaling factor	APC_SCAL6R
APC +00D8h	APC 7th ramp profile offset value	APC_OFFSET6

Table 44 APC scaling factor and offset value registers

APC+00E0h APC control register APC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															GSM	FPU
Type															R/W	R/W
Reset															1	0

GSM This field defines the operation mode of the APC module. In GSM mode, since there is only one slot in one frame, only one scaling factor and one offset value is required to be configured. If the bit is set, the programmer needs only to configure APC_SCAL0L and APC_OFFSET0. If the bit is not set, the APC module is operating in GPRS mode.

0 The APC module is operating in GPRS mode.

1 The APC module is operating in GSM mode. Default value.

FPU This field is used to force power on the APC D/A converter. Test only.

0 The APC D/A converter is not forced power up. It is only powered on when the transmission window is opened. Default value.

1 The APC D/A converter is forced power up.

Ramp profile programming

The first value of the first normalized ramp profile should be written in the least significant byte of the APC_PFA0 register. The second value should be written in the second least significant byte of the APC_PFA0, and so on.

Each ramp profile can be programmed to form arbitrary shape.

The start of ramping is triggered by one of the TDMA_APCSTR signals. The timing relationship of TDMA_APCSTR and TDMA slots is as depicted in **Figure 71** for 4 consecutive time slots case. The power ramping profile should comply with the timing mask defined in GSM SPEC 05.05. The timing offset values for 7 ramp profiles are stored in TDMA timer register from TDMA_APC0 to TDMA_APC6.

Since the APC unit provides more than 5 ramp profiles, it is able to accommodate up to 4 consecutive transmission slots. The additional 2 ramp profiles are used particularly when the timing relation between the last 2 transmission time slots and CTIRQ is uncertain. This provides the possibility to use some of them interchangeably in one and its succeeding frames.

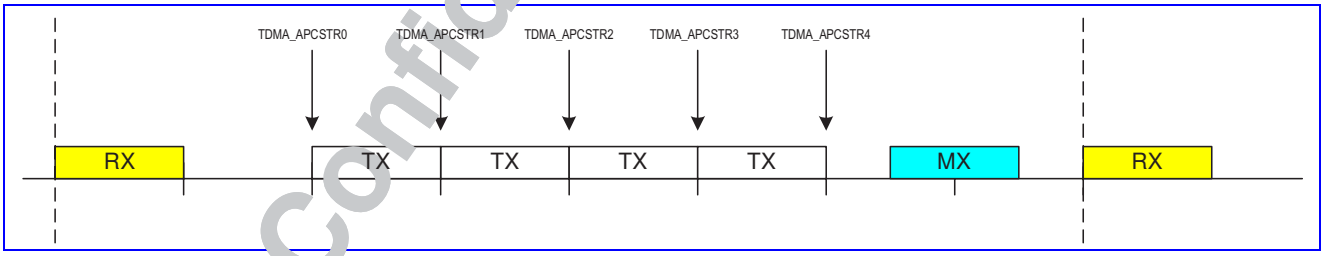

Figure 71 Timing diagram of TDMA_APCSTR.

In GPRS mode, in order to fit the intermediate ramp profile between different power levels, a simple scheme with scaling is used to synthesize the ramp profile. The equation is as follows:

$$DA_0 = OFF + S_0 \cdot \frac{DN_{15,pre} + DN_0}{2}$$

$$DA_{2k} = OFF + S_l \cdot \frac{DN_{k-1} + DN_k}{2}, k = 1,...,15$$

$$DA_{2k+1} = OFF + S_l \cdot DN_k, k = 0,1,...,15$$

$$l = \begin{cases} 0, & \text{if } 8 > k \geq 0 \\ 1, & \text{if } 15 \geq k \geq 8 \end{cases}$$

where **DA** represents the data to present to the D/A converter, **DN** represents the normalized data which is stored in the register **APC_PF*n***, S_0 represents the left scaling factor stored in register **APC_SCAL*nL***, S_1 represents the right scaling factor stored in register **APC_SCAL*nR***, and **OFF** represents the offset value stored in the register **APC_OFFSET*n***. The subscript ***n*** denotes the index of the ramp profile.

The ramp calculation before interpolation is as depicted in Figure 72.

During each ramp process, each word of the normalized profile is first multiplied by 10-bit scaling factors and added by an offset value to form a bank of 18-bit words. The first 8 words (in the left half part as in Figure 72) are multiplied by the left scaling factor S_0 and the last 8 words (in the right half part as in Figure 72) are multiplied by the right scaling factor S_1. The lowest 8-bit of each word will then be truncated to get a 10-bit result. The scaling factor is 100 in hexadecimal, which represents no scaling on reset. The value smaller than 100 will scale down the ramp profile, and the value larger than 100 will scale up the ramp profile.

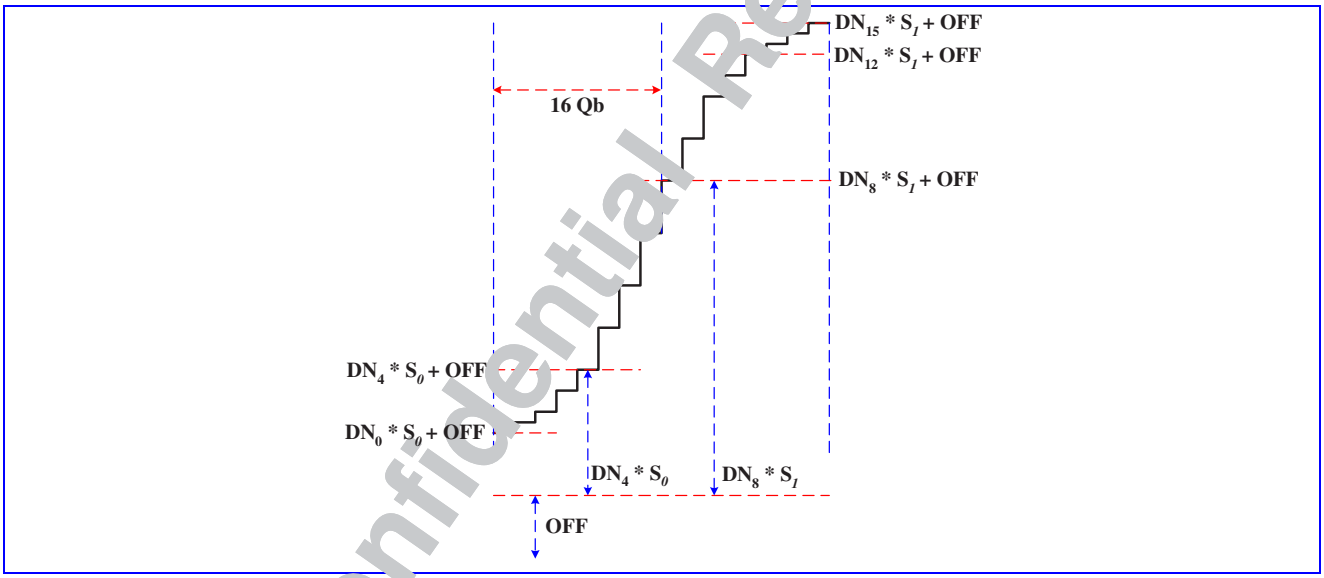

Figure 72 The timing diagram of the APC ramp.

The 16 10-bit words are linearly interpolated into 32 10-bit words. A 10-bit D/A converter is then used to convert these 32 ramp values at a rate of 1.0833MHz, that is, quarter bit rate. The timing diagram is shown in **Figure 73** and the final value will be retained on the output until the next event occurs.

D/A converter can be either powered on continuously or for a programmable duration (of 256 quarter-bits by default). The later option is for power saving.

In immediate mode, the MCU can directly control the AFC value without event triggering. The value written by the MCU immediately takes effect. In this mode, the D/A converter should be powered on continuously. When entering timer-triggered mode from immediate mode (by setting flag I_MODE in the register AFC_CON to be 0), the D/A converter will be kept powered on for a programmable duration (of 256 quarter-bits by default) if the next TDMA_AFC has not been pulsed in the duration. The duration will be prolonged upon receiving next events.

The two modes provide flexibility when controlling the oscillator. The 13-bit DAC proves to be monotonic. Associated with proper AFC algorithm, MT6219 achieves good tracking of the RF channels and the highest performance.

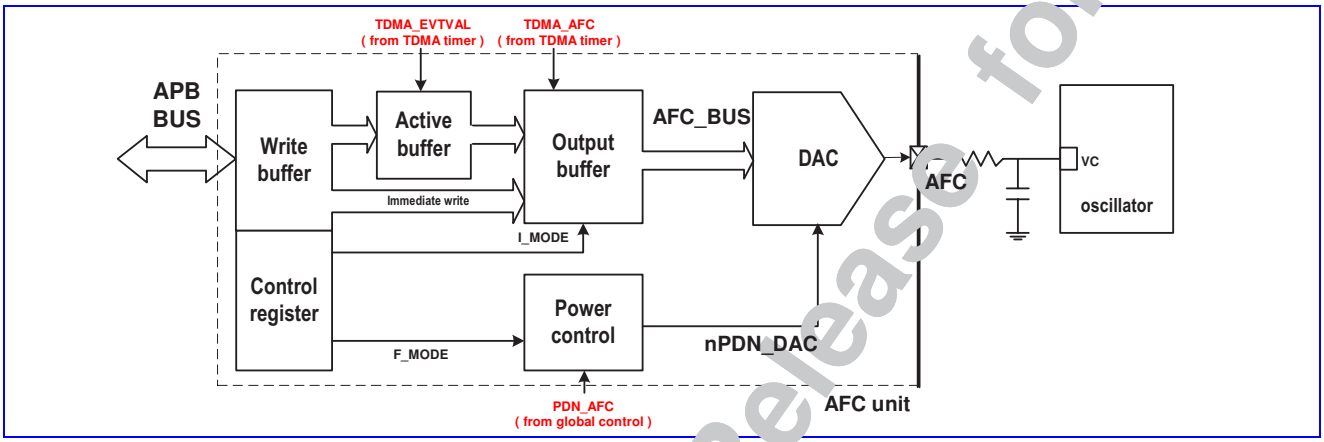

Figure 74 The block diagram of the AFC controller

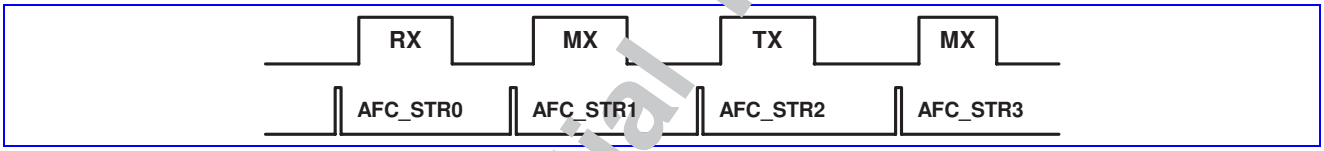

Figure 75 The timing diagram of the AFC controller

Register Definitions

AFC+0000h AFC control register AFC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RDACT	F_MODE	FETENV	I_MODE
Type													R/W	R/W	R/W	R/W
Reset													0	0	0	0

Four control modes are defined and can be controlled through the AFC control register. F_MODE enables the force power up mode. FETENV enables the direct write operation to the active buffer. I_MODE enables the immediate mode. RDACT enables the direct read operation from the active buffer.

RDACT The flag enables the direct read operation from the active buffer. Note the control flag is only applicable to the four data buffer including AFC_DAT0, AFC_DAT1, AFC_DAT2, and AFC_DAT3.

0 APB read from the write buffer.

1 APB read from the active buffer.

FETENV The flag enables the direct write operation to the active buffer. Note the control flag is only applicable to the for data buffer including AFC_DAT0, AFC_DAT1, AFC_DAT2, and AFC_DAT3.

0 APB write to the write buffer.

1 APB write to the active buffer.

F_MODE The flag enables the force power up mode.

0 The force power up mode is not enabled.

1 The force power up mode is enabled.

I_MODE The flag enables the immediate mode. To enable the immediate mode also enable the force power up mode.

0 The immediate mode is not enabled.

1 The immediate mode is enabled.

AFC +0004h AFC data register 0 AFC_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AFCD												
Type				R/W												

The register stores the AFC value for the event 0 triggered by the TDMA timer in timer-triggered mode. When RDACT or FETENV is set, the data transfer operates on the active buffer. On the contrary, when RDACT or FETENV is not set, the data transfer operates on the write buffer.

There are four registers (AFC_DAT0, AFC_DAT1, AFC_DAT2, AFC_DAT3) of the same type, which corresponds to the event triggered by the TDMA timer. The four registers are summarized in **Table 45**.

Immediate mode can only use AFC_DAT0. In this mode, only the control value in the AFC_DAT0 write buffer is used to control the D/A converter. Unlike timer-triggered mode, the control value in AFC_DAT0 write buffer could bypass the active buffer stage and is directly coupled to the output buffer in immediate mode. To use immediate mode, it is recommended to program the AFC_DAT0 in advance and then enable the immediate mode by setting the flag I_MODE in the register AFC_CON.

The register AFC_DATA0, AFC_DAT1, AFC_DAT2, and AFC_DAT3 have no initial values. So it has to be programmed before any AFC event takes place. However, the AFC value for the D/A converter, i.e., the output buffer value, is initially 0 right after power up before any event takes place.

AFCD The field is the AFC sample for the D/A converter.

Register Address	Register Function	Acronym
AFC +0004h	AFC control value 0	AFC_DAT0
AFC +0008h	AFC control value 1	AFC_DAT1
AFC +000Ch	AFC control value 2	AFC_DAT2
AFC +0010h	AFC control value 3	AFC_DAT3

Table 45 AFC Data Registers

AFC +0014h AFC power up period AFC_PUPER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PU_PER												
Type				R/W												