CIRCUIT DESCRIPTION/电路说明

Frequency configuration

The receiver utilizes double conversion. The first IF is 38.850MHz and the second IF is 450kHz. The first local oscillator signal is supplied from the PLL circuit.The PLL circuit in the transmitter generates the necessary frequencies. Fig. 1 shows the frequencies.

频率构成

接收部采用二次变频超外差方式，第一中频为38.85MH,第二中频为450KHz。第一本振频率信号由锁相环电路（PLL）提供，发射部由锁相环电路直接产生所需要的频率。图1现实各种频率。

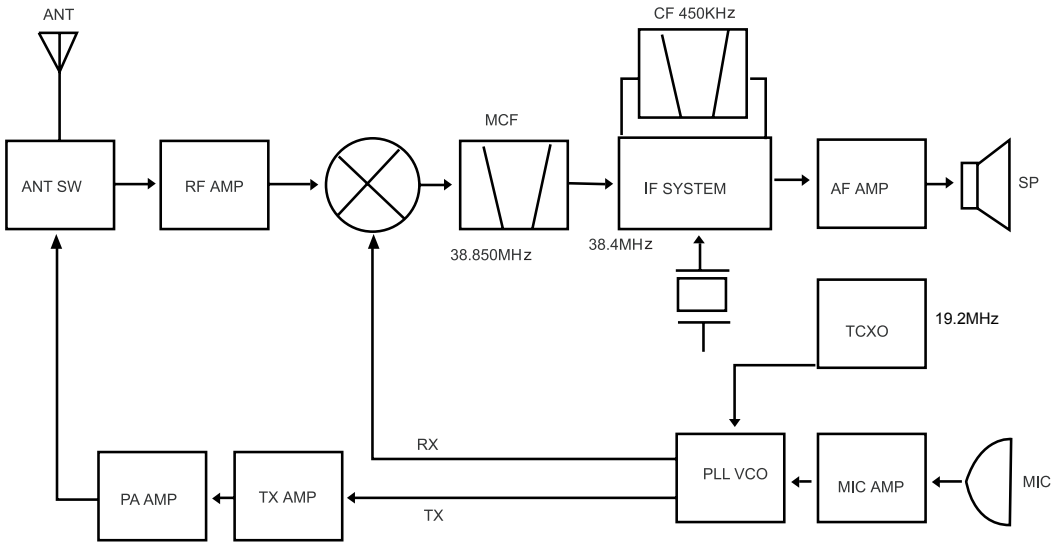

Fig. 1 Frequency configuration/频率构成

Receiver

The receiver is double conversion super heterodyne, designed to operate in the frequency range of 136 to 174MHz. The frequency configuration is shown in Fig. 1.

1) Front - end RF amplifier

An incoming signal from the antenna is applied to an RF amplifier (Q12) after passing through a transmit/receive switch circuit (D1,D2,D3 are off) 。After the signal is amplified (Q12), passing through a band pass filter BPF and is amplified (Q17) again,the signal is filtered through a band pass filter (L17 and L18) to eliminate unwanted signals before it is passed to the first mixer. (See Fig. 2)

接收部

接收部为二次变频超外差方式，设计操作的频率范围是136-174MHz。

图1显示频率构成

1）前端射频放大器

从天线输入的信号经过收发转换电路D1，D2，D3断开）。在射频放大器（Q12）处放大，信号被放大后。经过带通滤波器（BPF）和再次在射频放大器（Q17）处放大，在通过第一混频器之前，经过带通滤波器滤波来消除不要的信号。（参见图2）

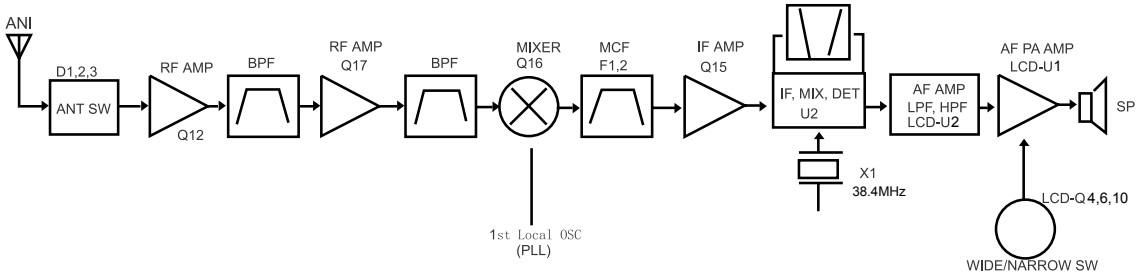

Fig. 2 Receiver section configuration/接收部构成

2) First Mixer

The signal from the RF amplifier is heterodyned with the first local oscillator signal from the PLL frequency synthesizer circuit at the first mixer (Q16) to create a 38.850MHz first intermediate frequency (1st IF) signal. The first IF signal is then fed through two monolithic crystal filters (F1, F2) to further remove spurious signals.

3) IF amplifier

The first IF signal is amplified by Q15, and then enters U2 (FM processing IC). The signal is heterodyned again with a second local oscillator signal within U2 to create a 450kHz second IF signal. The second IF signal is then fed through a 450kHz ceramic filter (F3) to further eliminate unwanted signals before it is amplified and FM detected in U2.

4) AF amplifier

The recovered AF signal obtained from U2 is amplified by LCD-U3 handle, the processed AF signal passes through an AF volume control and is amplified to a sufficient level to drive a loud speaker by an AF power amplifier (LCD-U2).

5) Squelch

Part of the AF signal from the IC enters the FM IC again, and produce the corresponding noise level R25 by R52 to go to the analog port of the microprocessor (LCD-U3). LCD-U3 determines whether to output sounds from the speaker by checking whether the input voltage is higher or lower than the preset value.To output sounds from the speaker, LCD-U3 sends a high signal to the MUTE and AFCO lines through LCD-Q10,Q11, Q12.(See Fig. 3)

2） 第一混频器

来自射频放大器的信号与来自锁相环频率合成 器电路的第一本振信号在第一混频器（Q16）处混频并生成38.850MHz的第一中频（1st IF）信号。第一中频信号通过两个单片晶体滤波器（F1，F2）进一步消除邻道的杂波信号。

3）中频放大器

第一中频信号通过Q15放大，然后进入芯片U2（调频处理芯片）,信号在U2中与第二本振信号再次混频生成一个450KHz陶瓷滤波器（F3）滤除无用杂散信号。

4）音频放大器

在U2中鉴频解调出的音频信号通过LCD-U3处理放大 ，经处理的音频信号通过音量控制电路再经过音频功率放大器（LCD-U2）放大后、驱动扬声器。

5） 噪音抑制电路

从IC输出的音频信号的一部分再进入IC，R25生成一个对应于噪音电平的直流电压通过R52，进入到微处理器的模拟端口 (LCD-U3)。LCD-U3 通过检测输入的电压是高于还是低于预设值来决定是否从扬声器输出声音。要通过扬声器输出声音， LCD-U3向静音和自动频率控制振荡器连线发送一个高电平信号，通过LCD-Q10，Q11，Q12。（见图3）。

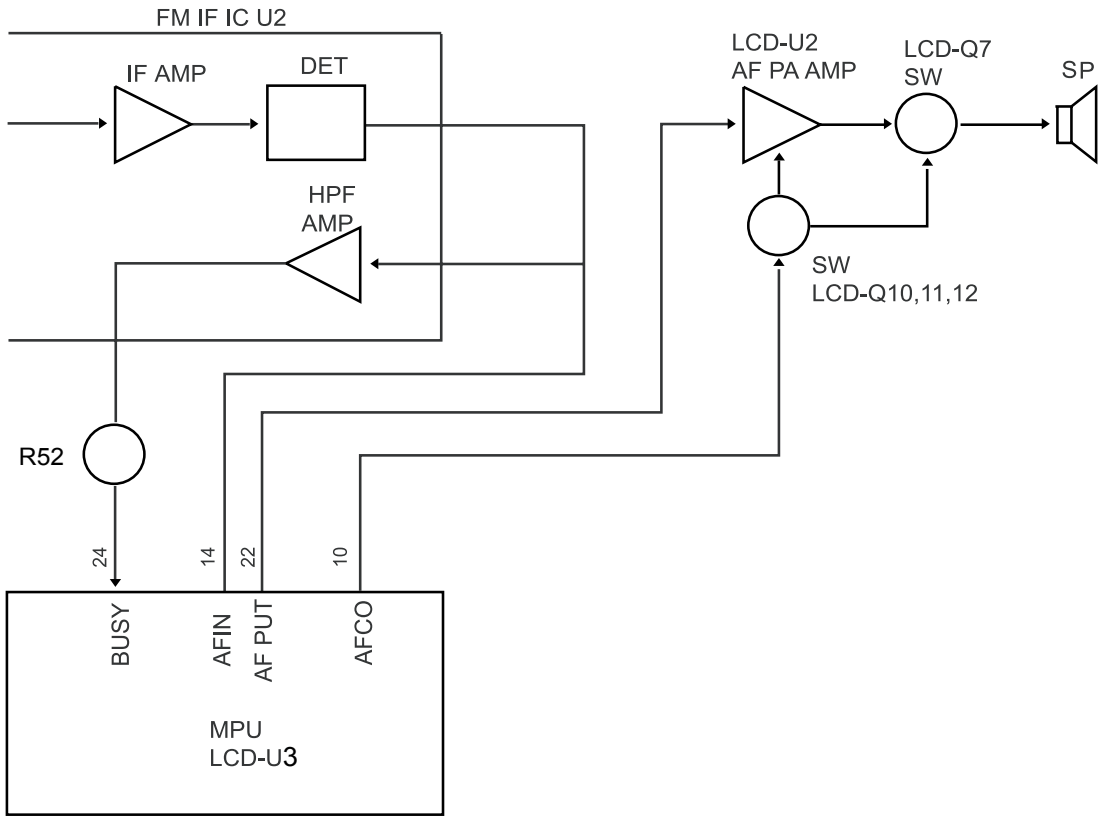

Fig.3 AF Amplifier and squelch/图3 音频放大器和噪音抑制电路

6) Receive signaling

QT/DQT

300 Hz and higher audio frequencies of the output signal from IF IC are entered the microprocessor (LCD-U3). LCD-U3 determines whether the QT or DQT matches the preset value, and controls the MUTE and AFCO and the speaker output sounds according to the squelch results.

3. PLL frequency synthesizer

The PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission.

1) PLL

The frequency step of the PLL circuit is 5 or 6.25kHz. A 19.2MHz reference oscillator signal is divided at U3 by a fixed counter to produce the 5 or 6.25kHz reference frequency. The voltage controlled oscillator (VCO) output signal is buffer amplified by Q18, then divided in U3 by a dual-module programmable counter .The divided signal is compared in phase with the 5 or 6.25kHz reference signal in the phase comparator in U3. The output signal from the phase comparator is filtrered through a low-pass filter and passed to the VCO to control the oscillator frequency. (See Fig.4)

2) VCO

The operating frequency is generated by Q25 in transmit mode and Q20 in receive mode. The oscillator frequency is controlled by applying the VCO control voltage, obtained from the phase comparator, to the varactor diodes (D9, D10 in transmit mode and D4, D5 in receive mode).In receive mode causing RX-V supplied and turn Q27 on .In transmit mode causing TX-V supplied and turn Q22 on. The outputs from Q20, Q25 are amplified by Q26，Q21 and sent to the buffer amplifiers.

6）接收信令

QT/DQT

来自于中频芯片输出信号的300Hz和更高的音频，所得到的信号微处理器（LCD-U3）处理。LCD-U3确定QT或DQT是否匹配预设置、并且根据噪声抑制电路的结果控制MUTE和AFCO以及扬声器输出声音。

3. 锁相环频率合成器

锁相环电路生成用于接收的第一本振信号和用于发送的射频载波信号。

1）锁相环电路

锁相环电路的步进频率5或6.25KHz。19.2MHz的参考振荡器信号通过一个混合计数器在U3中被分频并生成5或6.25KHz的参考频率。压空振荡器（VCO）输出的信号通过Q18缓冲放大器，然后U3中被可编程脉冲吞除计算器分频。被分频的信号在带有5或6.25KHz参考信号的相位比较器的U3中被比较。从相位比较器输出的信号进入一个低通滤波器后，并通过压空振荡器来控制振荡频率。（参见图4）

2）压控振荡器

在发射模式中通过Q25产生操作频率，在接收模式中通过Q20产生操作频率。通过相位比较器到变容二极管（在发射模式中为D9和D10，在接收模式中为D4和D5）采用压空振荡器控制电压来控制振荡频率。在接收模式中，由于RX-V供电，导通Q22。在发射模式中，由于TX-V供电，导通Q27。Q20和Q25的输出通过Q26和Q21被放大并被发送到缓冲放大器。

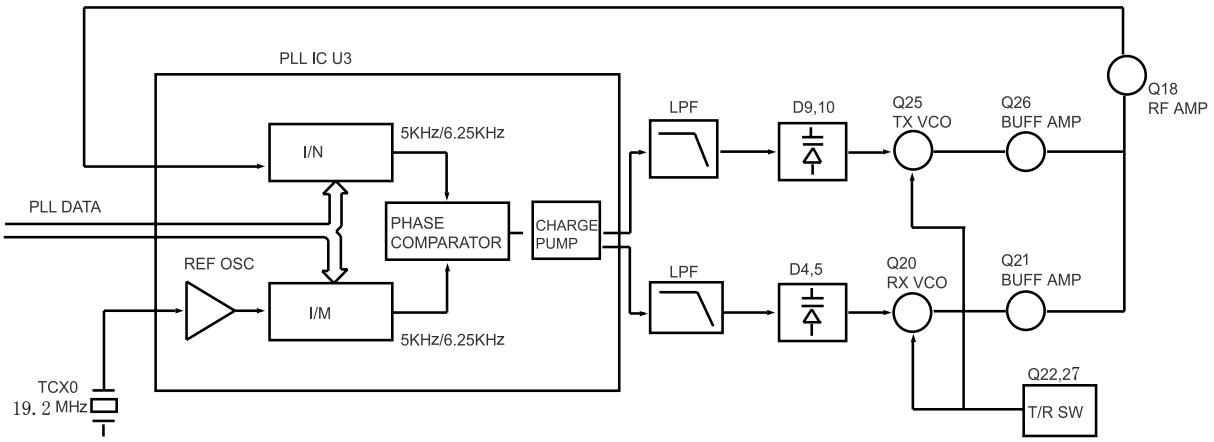

Fig. 4 PLL circuit/图4 锁相环电路

3) UNLOCK DETECTOR

If a pulse signal appears at the LD pin of U3, an unlock condition occurs, and the DC voltage obtained from D7, R133, R135 and R130 causes the voltage applied to the UL pin of the microprocessor to go low. When the microprocessor detects this condition, the transmitter is disabled,ignoring the push-totalk switch input signal. (See Fig.5)

3）失锁检测器

如果U3的LD管脚上出现高电平，则产生失锁状态。并从D7，R133,R135获得直流电压，且R130产生的提供给微处理器UL管脚的电压降低。当微处理器检测到此种情况时，不能进行发射，无视通话转换开关输入信号。（参见图5）

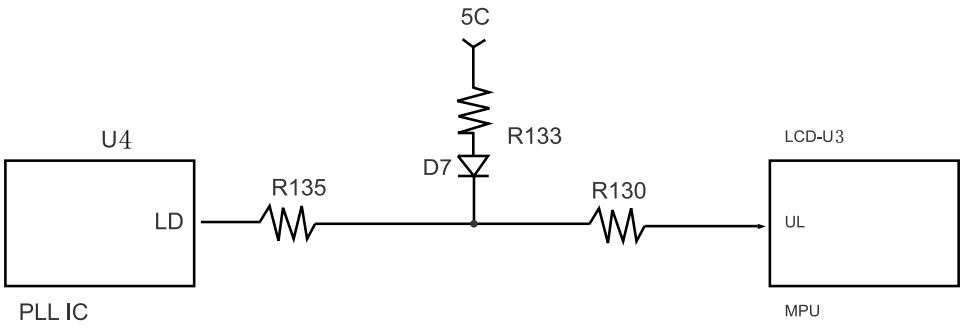

Fig.5 Unlock detector circuit /图**5** 失锁检测器电路

4. Transmitter

1) Transmit audio

The modulation signal from the microphone is amplified by U4 (A/2), passes through a preemphasis circuit, and amplified by the other U4 (B/2) to perform IDC operation.The signal then passes through a low-pass filter (splatter filter) and cuts 3kHz and higher frequencies.The resulting signal goes to the VCO through the VCO modulation terminal for direct FM modulation. (See Fig. 6)

2) QT/DQT encoder

A necessary signal for QT/DQT encoding is generated by LCD-U3 and FM-modulated to the PLL reference signal. Since the reference OSC does not modulate the loop characteristic frequency or higher, modulation is performed at the VCO side by adjusting the balance. (See Fig. 6)

4. 发射部

1）发射音频

来自于话筒的调制信号通过U4（A/2）放大，经过一个预加重电路，并通过另一个U4（B/2）放大后进入IDC处理。然后信号通过一个低通滤波器（分离滤波器）并滤除比3KHz频率更高的部分。得到的信号进入压控振荡器直接进行调频调制。

2）QT/DQT编码器

QT/DQT编码所需的信号通过LCD-U3产生，被锁相环电路的基准率调整。由于基准振荡器不能对频率环路特性外的频率进行调制，因此通过分配器在压控振荡器一侧进行调制。（参见图6）

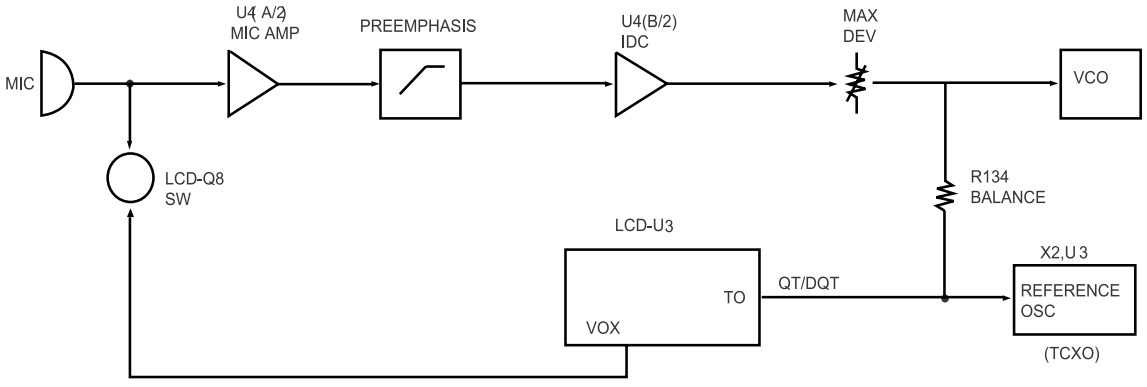

Fig.6 Transmit audio QT/DQT/图6 发射音频QT/DQT

3) VCO and RF amplifier

The transmit signal obtained from the VCO buffer amplifier Q26, is amplified by Q6,7,8. This amplified signal is passed to the power amplifier, Q10 and Q11, which consists of a 2-stage FET amplifier and is capable of producing up to 5W of RF power. (See Fig.7)

3）压控振荡器和射频放大器

从压控振荡缓冲放大器Q26,接收到的发送信号通过Q6,7,8被放大.这个放大信号通过功率放大器,Q10和Q11(包括一个二级场效应管放大器),并能产生5W射频功率.(参见图7)

4) ANT switch and LPF

The RF amplifier output signal is passed through a low pass filter network and a transmit/receive switching circuit before it is passed to the antenna terminal. The transmit/receive switching circuit is comprised of D1, D2 and D3. D3 turned on (conductive) in transmit mode and off (isolated) in receive mode.

4) 天线转换开关和LPF

在其到达天线终端之前，射频放大器输出信号通过一个低通滤波器网络和发射/接收转换电路。发射/接收转换电路由D1，D2和D3构成。D3在发射模式下开启（通导），在接收模式下关闭（隔离）。

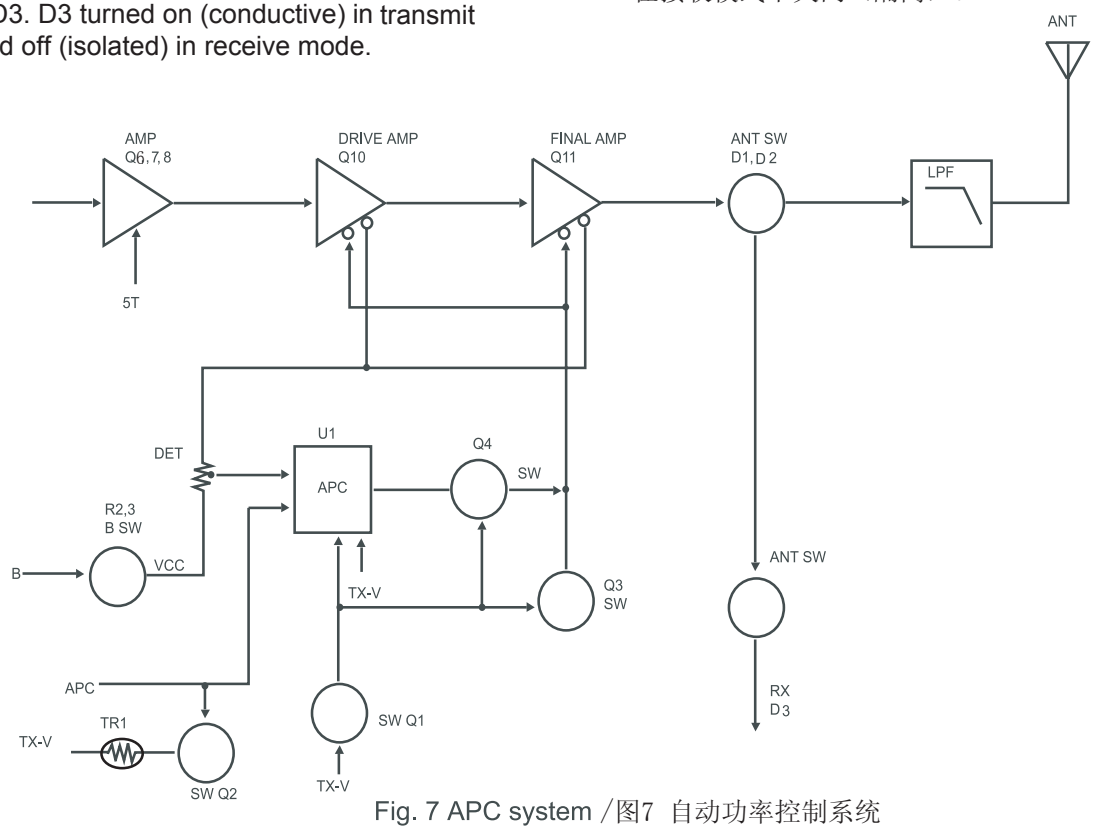

Fig. 7 APC system /图7 自动功率控制系统

5) APC

The automatic power control (APC) circuit stabilizes the transmitter output power at a predetermined level by sensing the drain current of the final amplifier Field Effect Transistor (FET) . The voltage comparator, U1 (B/2), compares the voltage obtained from the above drain current with a reference voltage which is set using the microprocessor. An APC voltage proportional to the difference between the sensed voltage and the reference voltage appears at the output of U1 (A/2). This output voltage controls the gate of the FET power amplifier, which keeps the transmitter output power constant. The transmitter output power can be varied by the microprocessor which in turn changes the reference voltage and hence, the output power.

5) 自动功率控制

自动功率控制（APC）电路，通过测检末级放大器场效应管的漏极电流来稳定发射的输出功率。电压比较电路，U1（B/2）用微处理器设定的参考电压来比较从末级电流所获得的电压。自动功率控制电压与U1（A/2）输出的自动检测电压和参考电压之间的差值成正比。此输出电压控制场效应管功率放大器，保持发射部输出功率常数。发射部输出功率可以通过微处理器进行改变，在微处理器中改变参考电压来控制输出功率。

6) Terminal protection circuit

When the thermistor (TH1) reaches about 80°C, the protection circuit turns on Q2 to protect transmitting final amplifier (Q22) from the over heating.

6) 温度保护电路

当热敏电阻（TH1）的温度达到80°C时，保护电路开启Q2来保护末级放大器避免过热。

5. Power supply

The battery power source is internally regulated by the circuit (LCD-U3) and outputs 5V DC.This 5V DC is also supplied to the microprocessor (LCD-U3) and reset circuit（LCD-Q8 current）.This reference voltage is used for the following DC power sources: 5V DC (RX-V for the receiver, TX-V for the transmitter, and VCO-V for part of VCO).

5. 电源

电池电源通过电路（LCD-U3）内部调整并输出直流电压5V。同时直流输出电压5V也供应给微处理器(LCD-U3)和复位电路（LCD-Q8电流），参考电压用于以下直流电源：5V直流（RX-V用于接收，TX-V用于发射，VCO-V用于压控振荡器的一部分）。

6. Control system

The microprocessor (LCD-U3) is operating at a clock of 32.768KHz. This microprocessor controls the EEPROM data transfer,PLL data and other various functions.

6. 控制系统

微处理器（LCD-U3）在32.768MHz的情况下运行。微处理器控制EEPROM的数据转移，锁相环数据和其它各种功能。