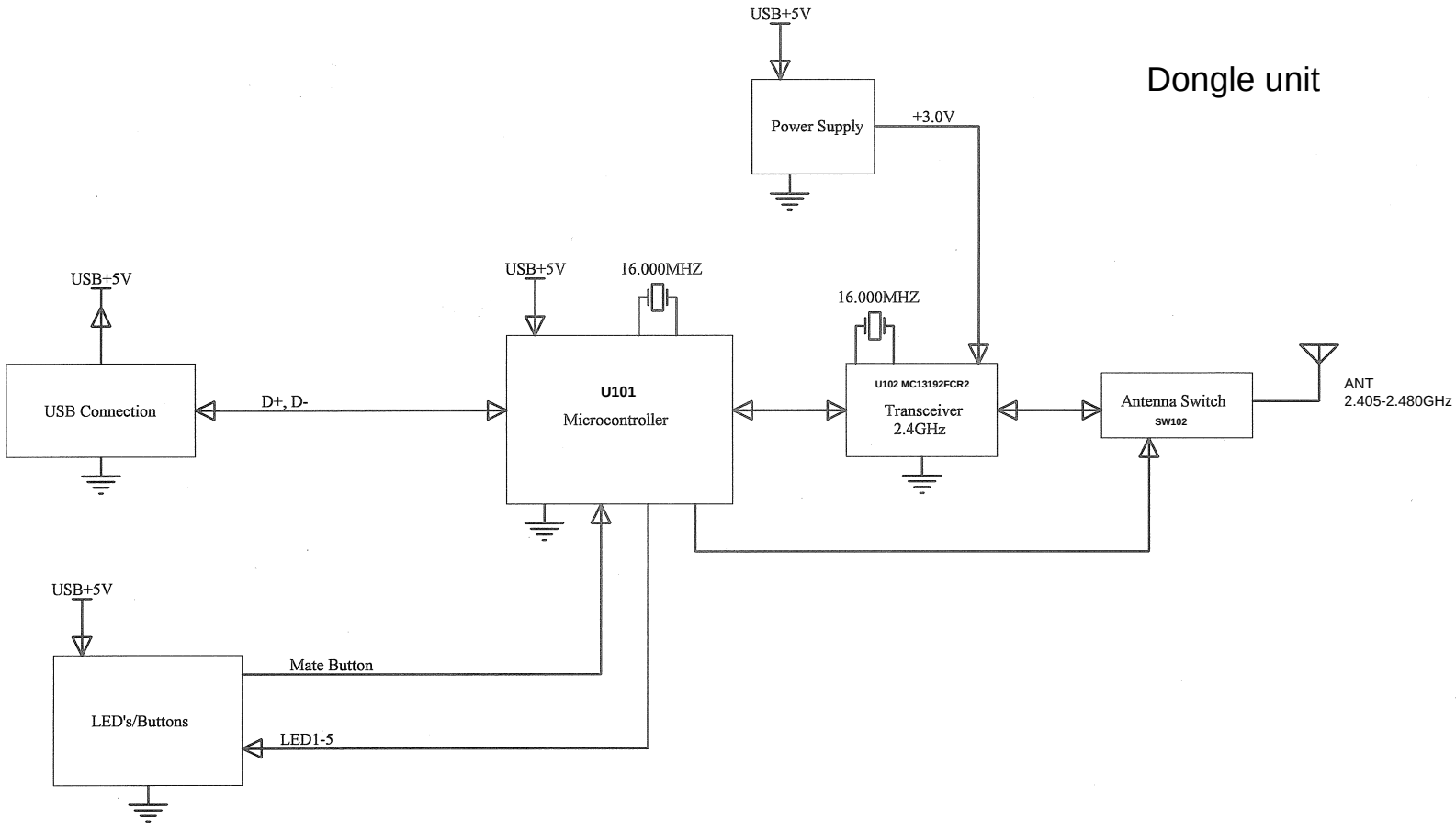
Dongle unit



IntelliSwitch Rx Block Diagram

Madentec Limited
4664 - 99 St.
Edmonton, Alberta
T6E 5H5

Size	FCSM No.	DWG No.	Rev
A			2

Scale	Date : 5/4/07	Sheet 1 OF 1

4.3 Transmit Path Description

For the transmit path, the TX data that was previously stored in RAM is retrieved (packet mode) or the TX data is clocked in via the SPI (stream mode), formed into packets per the 802.15.4 PHY, spread, and then up-converted to the transmit frequency.

If the MC13192/MC13193 is in packet mode, data is processed as an entire packet. The data is first loaded into the TX buffer. The MCU then requests that the MC13192/MC13193 transmit the data. The MCU is notified via an interrupt when the whole packet has successfully been transmitted.

In streaming mode, the data is fed to the MC13192/MC13193 on a word-by-word basis with an interrupt serving as a notification that the MC13192/MC13193 is ready for more data. This continues until the whole packet is transmitted.

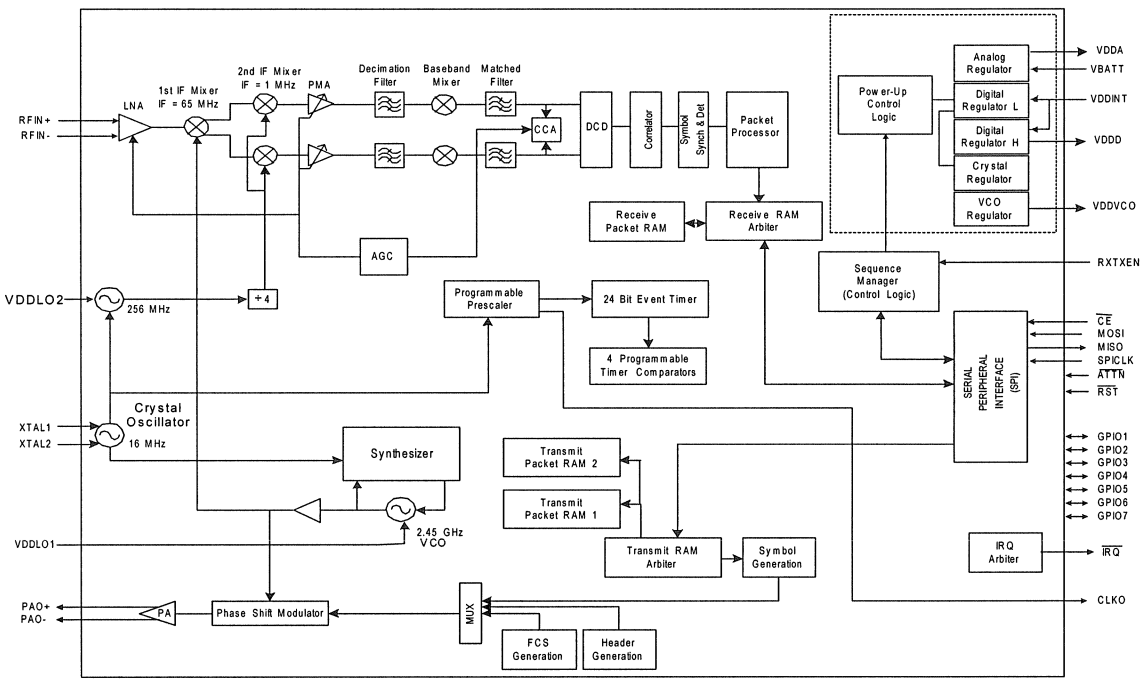


Figure 3. MC13192 Simplified Block Diagram