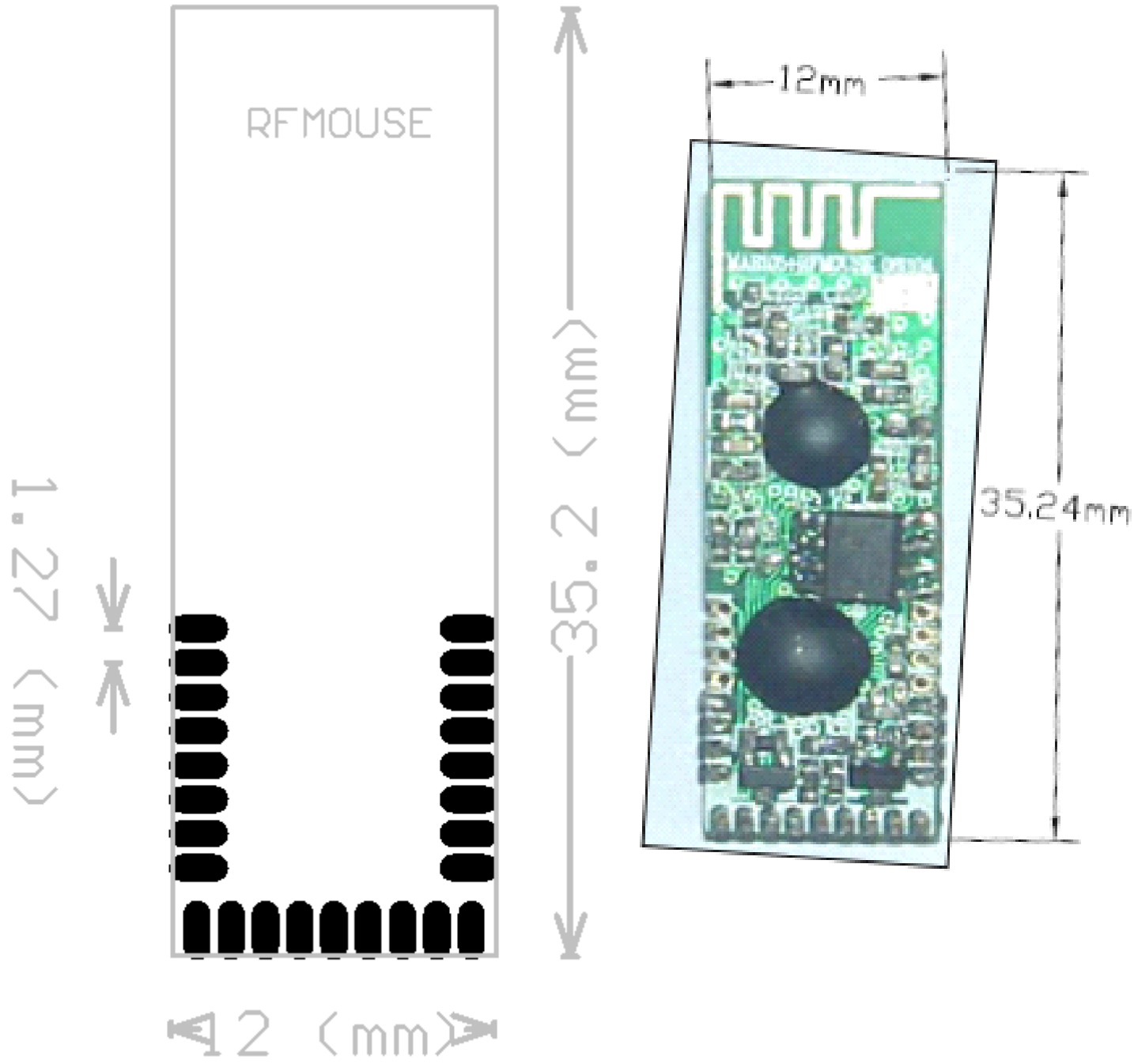
Circuit description

The transmitter of the EUT is supplied by 2*AA batteries and employing GFSK modulation in 2.4GHz band. The antenna is PCB antenna without connector.
The 16M crystal oscillator driver the base of MCU. Details see following pages.
The ground is only that of the printed circuit board, no external ground connection.

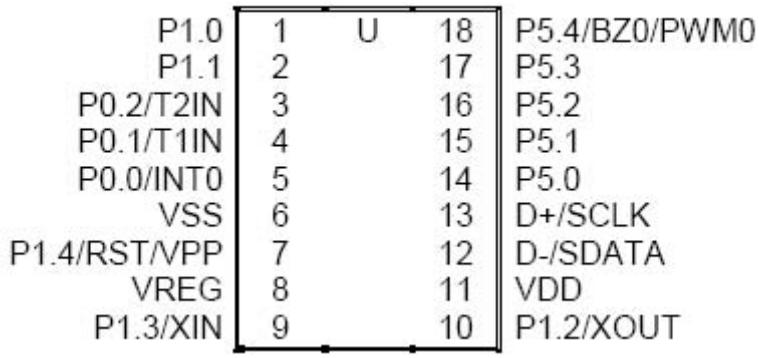
7. MAR105P+RF MOUSE资料



MAR105P+RF MOUSE 图示

MCC689-01A 资料

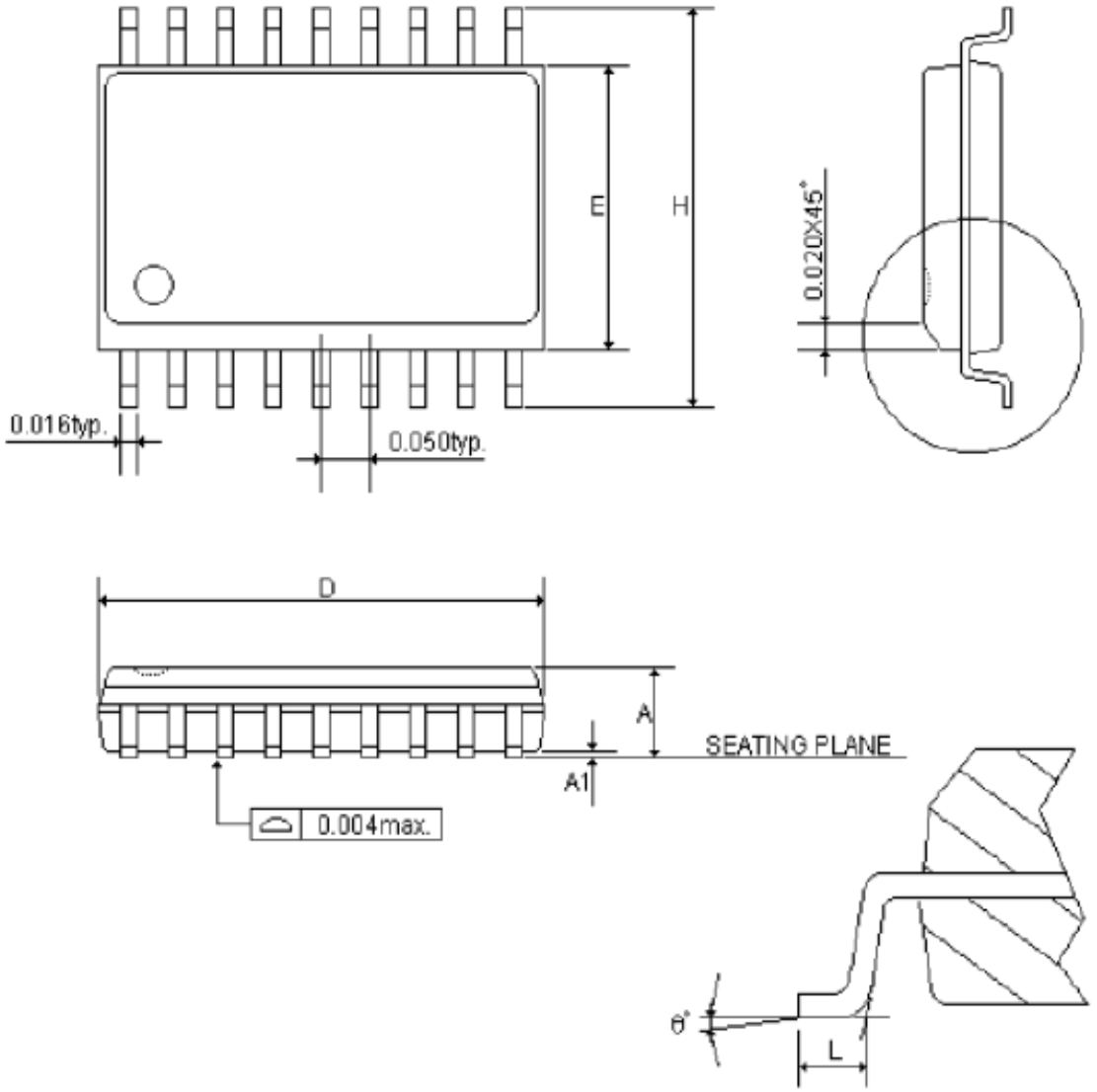
8.1 SOP-18PIN 封装片资料



脚位描述

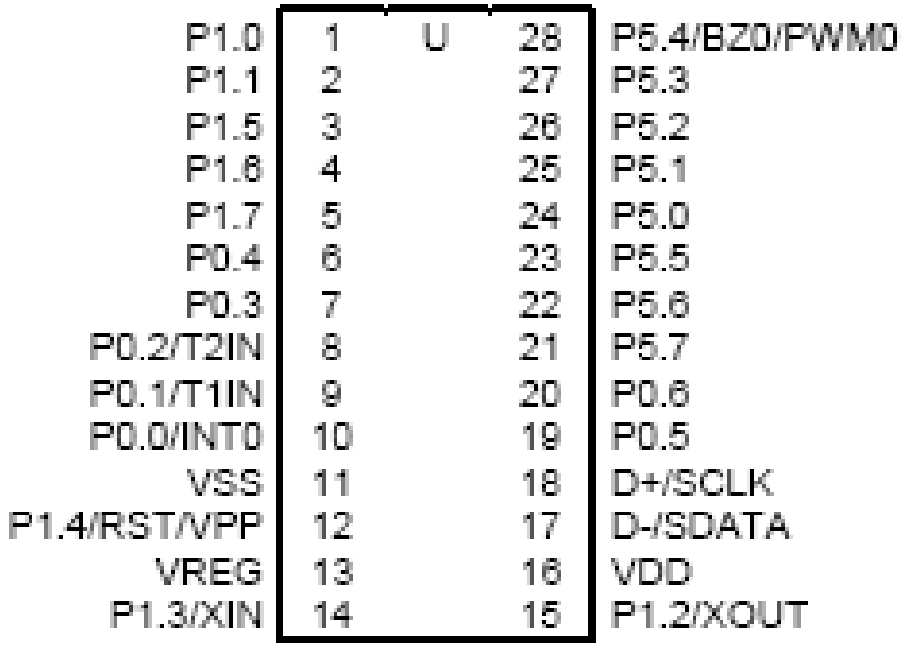
PIN NAME	TYPE	DESCRIPTION
VDD, VSS	P	Power supply input pins for digital circuit.
P0.0/INT0	I/O	P0.0: Port 0.0 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode. Built wakeup function. INT0: External interrupt 0 input pin
P0.1/T1IN	I/O	P0.1: Port 0.1 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode. Built wakeup function. T1IN: T1 timer capture input pin.
P0.2/T2IN	I/O	P0.2: Port 0.1 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode. Built wakeup function. T2IN: T2 timer capture input pin.
P0[6:3]	I/O	P0: Port 0 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode.
P1.0	I/O	P1.0: Port 1.0 bi-direction pin Schmitt trigger structure and built-in pull-up resisters as input mode. Open-Drain function controlled by "P1OC" register. Built wakeup function.
P1.1	I/O	P1.1: Port 1.1 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode. Open-Drain function controlled by "P1OC" register. Built wakeup function.
P1.2/XOUT	I/O	XOUT: Oscillator output pin while external crystal enable P1.2: Port 1.2 bi-direction pin under internal 16M RC and external RC. Schmitt trigger structure and built-in pull-up resisters as input mode. Built wakeup function.
P1.3/XIN	I/O	XIN: Oscillator input pin while external oscillator enable (crystal and RC). P1.3: Port 1.3 bi-direction pin under internal 16M RC. Schmitt trigger structure and built-in pull-up resisters as input mode.
P1.4/RST/VPP	I, P	RST is system external reset input pin under Ext. RST mode. Schmitt trigger structure, active "low", normal stay to "high". P1.4 is input only pin without pull-up resistor under P1.4 mode. Built wakeup function. OTP 12.3V power input pin in programming mode.
P1[7:5]	I/O	P1: Port 1 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode.
P5.0	I/O	P5.0: Port 5.0 bi-direction pin Schmitt trigger structure and built-in pull-up resistors as input mode.
P5.1	I/O	P5.1: Port 5.1 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode
P5.4/BZ0/PWM0	I/O	P5.4: Port 5.4 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode. BZ0: 1/2 TC0 counter output pin. PWM0: PWM0 output.
P5[7:2]	I/O	P5: Port 5 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode.
VREG	O	3.3V voltage output from USB 3.3V regulator.
D+, D- SCLK, SDATA	I/O I/O	USB differential data line. PS/2 clock and data lines

封装尺寸



SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	0.093	0.099	0.104	2.362	2.502	2.642
A1	0.004	0.008	0.012	0.102	0.203	0.305
D	0.447	0.455	0.463	11.354	11.557	11.760
E	0.291	0.295	0.299	7.391	7.493	7.595
H	0.394	0.407	0.419	10.008	10.325	10.643
L	0.016	0.033	0.050	0.406	0.838	1.270
θ°	0°	4°	8°	0°	4°	8°

8.2 SSOP-28PIN 封装片资料



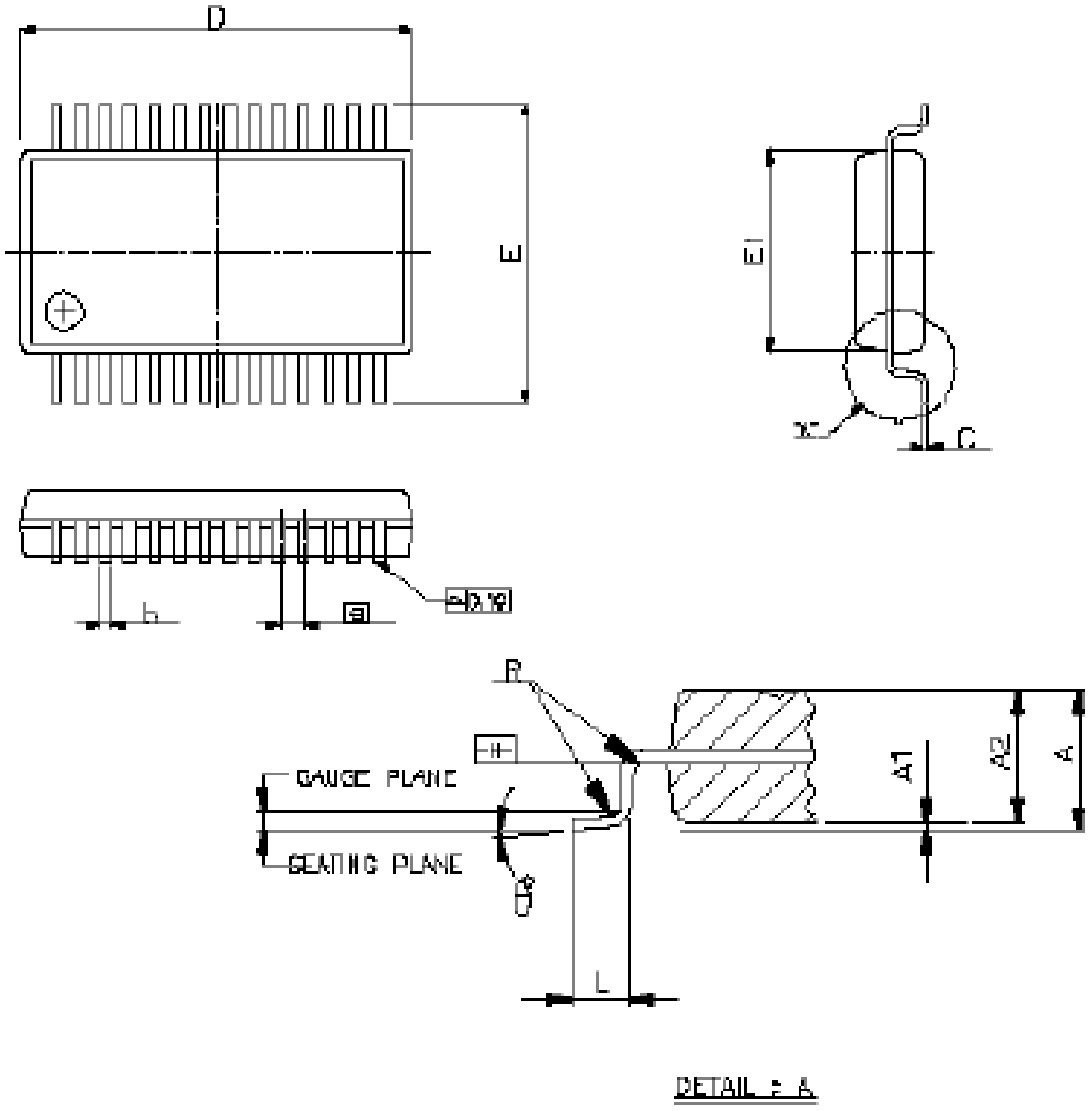
脚位描述：

BONDING PAD LOCATION

NO	PAD NAME	X (um)	Y (um)	NO	PAD NAME	X (um)	Y (um)
1	P1.0	-90.87	964.57	16	VDD	265.69	-963.5
2	P1.1	-200.87	964.57	NC	NC	381.85	-963.5
3	P1.5	-310.87	964.57	17	SDATA	525.53	-963.5
4	P1.6	-420.87	964.57	17	DN	655.85	-963.5
5	P1.7	-530.87	964.57	18	DP	765.85	-963.5
6	P0.4	-640.87	964.57	18	SCLK	888.57	-963.5
7	P0.3	-928	690.62	19	P0.5	929.57	-429.89
8	P0.2/T2IN	-928	580.62	20	P0.6	929.57	-319.89
9	P0.1/T1IN	-928	470.62	21	P5.7	929.57	-209.89
10	P0.0/INT0	-928	360.62	22	P5.6	929.57	-99.89
11	VSS	-928	250.62	23	P5.5	929.57	10.11
12	P1.4/RST	-928	128.02	24	P5.0	929.57	120.11
13	VREG	-82.3	-963.5	25	P5.1	349.13	964.57
14	XIN/P1.3	36.69	-963.5	26	P5.2	239.13	964.57
15	XOUT/P1.2	146.69	-963.5	27	P5.3	129.13	964.57
				28	P5.4/BZ0/PWM0	19.13	964.57

PAD SIZE = 88um * 88um, PITCH SIZE = 110um

Note: The IC substrate should be connected to VSS in the PCB layout artwork.

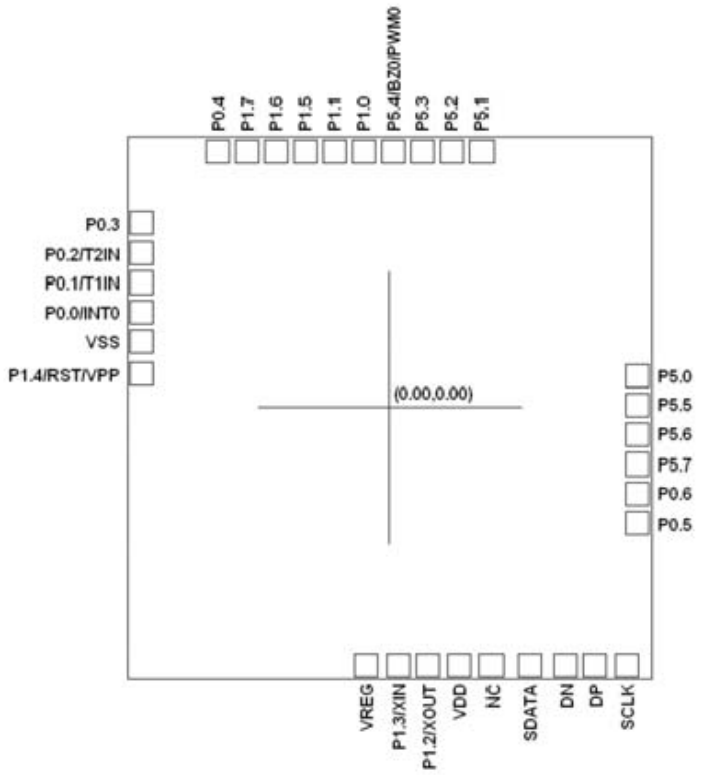


DETAIL : A

SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	-	-	0.08	-	-	2.13
A1	0.00	-	0.01	0.05	-	0.25
A2	0.06	0.07	0.07	1.63	1.75	1.88
b	0.01	-	0.01	0.22	-	0.38
C	0.00	-	0.01	0.09	-	0.20
D	0.39	0.40	0.41	9.90	10.20	10.50
E	0.29	0.31	0.32	7.40	7.80	8.20
E1	0.20	0.21	0.22	5.00	5.30	5.60
[e]	0.0259BSC			0.65BSC		
L	0.02	0.04	0.04	0.63	0.90	1.03
R	0.00	-	-	0.09	-	-
θ°	0°	4°	8°	0°	4°	8°

8.3 **DICE（OTP） 资料**

CHIP DIAGRAM



PAD SIZE = 88um * 88um, PITCH SIZE = 110um

Note: The IC substrate should be connected to VSS in the PCB layout artwork.

烧录点：P1.0，P1.1，VSS，VDD，RST，P5.0，P5.1。

BONDING PAD LOCATION

NO	PAD NAME	X (um)	Y (um)	NO	PAD NAME	X (um)	Y (um)
1	P1.0	-90.87	964.57	16	VDD	265.69	-963.5
2	P1.1	-200.87	964.57	NC	NC	381.85	-963.5
3	P1.5	-310.87	964.57	17	SDATA	525.53	-963.5
4	P1.6	-420.87	964.57	17	DN	655.85	-963.5
5	P1.7	-530.87	964.57	18	DP	765.85	-963.5
6	P0.4	-640.87	964.57	18	SCLK	888.57	-963.5
7	P0.3	-928	690.62	19	P0.5	929.57	-429.89
8	P0.2/T2IN	-928	580.62	20	P0.6	929.57	-319.89
9	P0.1/T1IN	-928	470.62	21	P5.7	929.57	-209.89
10	P0.0/INT0	-928	360.62	22	P5.6	929.57	-99.89
11	VSS	-928	250.62	23	P5.5	929.57	10.11
12	P1.4/RST	-928	128.02	24	P5.0	929.57	120.11
13	VREG	-82.3	-963.5	25	P5.1	349.13	964.57
14	XIN/P1.3	36.69	-963.5	26	P5.2	239.13	964.57
15	XOUT/P1.2	146.69	-963.5	27	P5.3	129.13	964.57
				28	P5.4/BZ0/PWM0	19.13	964.57

9. PAN3101 资料

Pin Description

Pin No.	Name	Type	Definition
1	OSCIN	IN	Resonator input
2	OSCOUT	OUT	Resonator output
3	SDIO	I/O	Serial interface bi-direction data
4	SCLK	IN	Serial interface clock
5	LED	OUT	LED control
6	VSS	GND	Chip ground
7	VDD	PWR	Chip power, 5V power supply
8	VREF	BYPASS	Voltage reference

模组尺寸图：

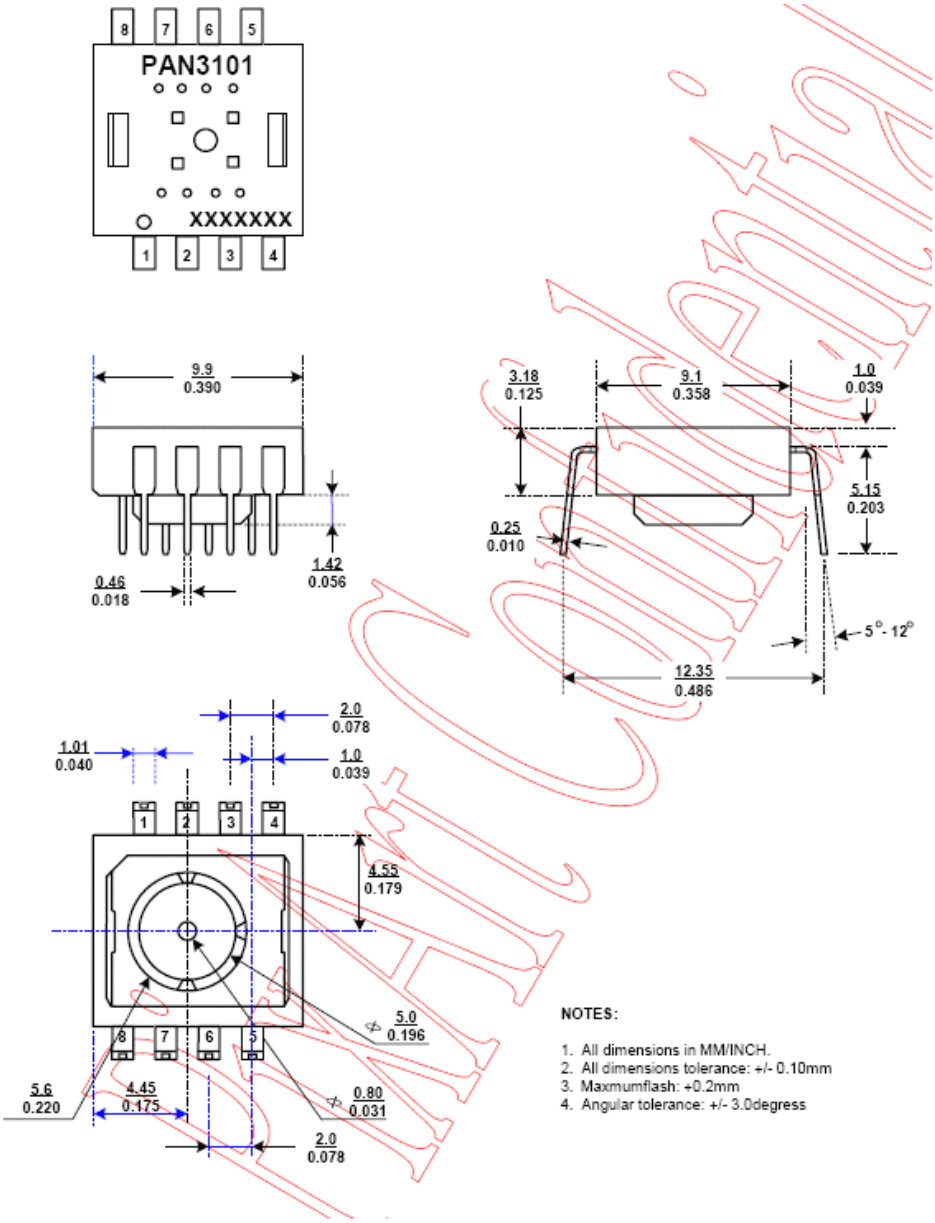


Figure 15. Package outline drawing

10. SNAD02 资料

BLOCK DIAGRAM

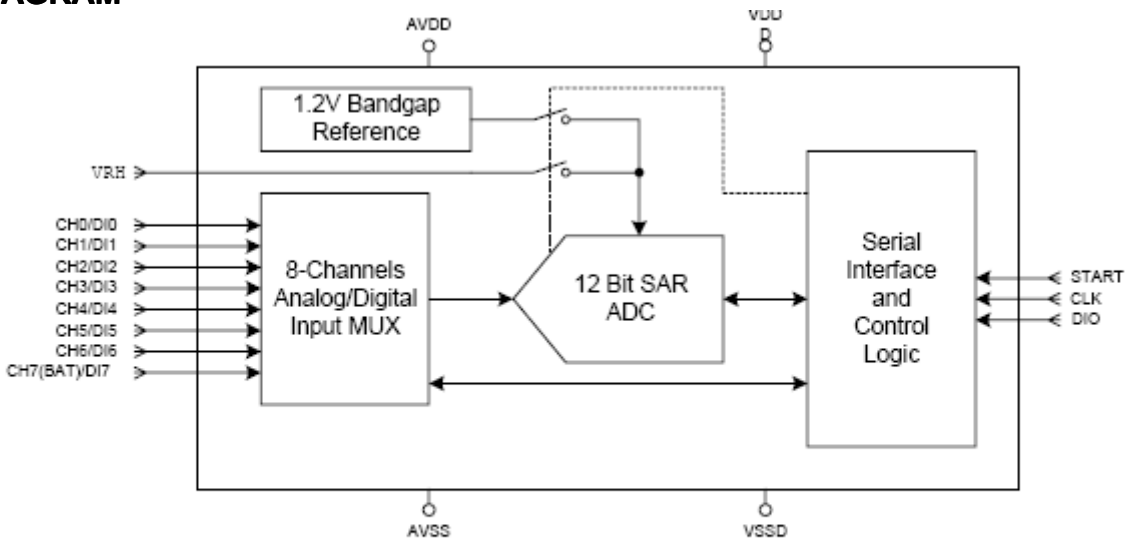


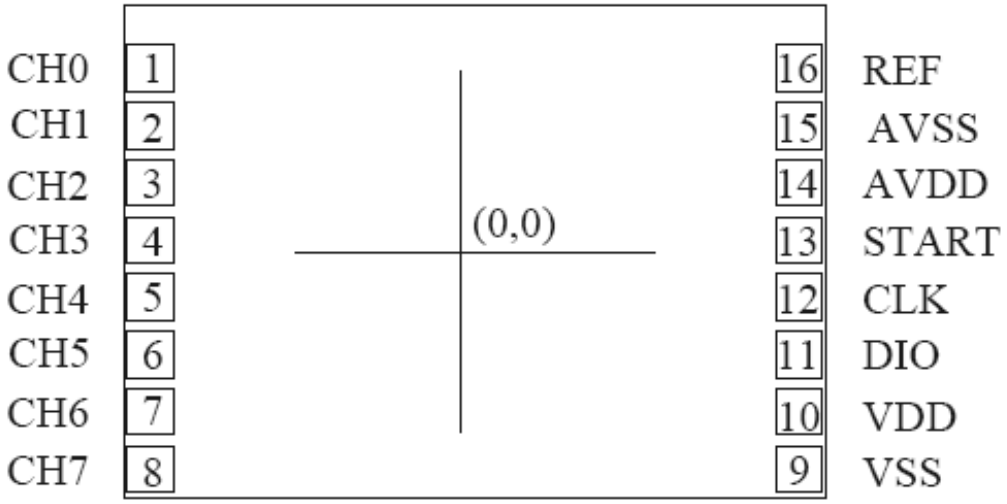
Figure-1 Block diagram of ADC

PIN ASSIGNMENTS

Pin Name	I/O	Description
CH[7] ~ CH[0]	I	Analog input / digital input
REF	I	Reference voltage of analog signal
VDD	I	Positive power
VSS	I	Negative power
AVDD	I	Positive power of analog circuit
AVSS	I	Negative power of analog circuit
START	I	Command initialization signal (from host controller)
CLK	I	Clock of data communication and AD conversion (from host controller)
DIO	IO	Data input and output of data communication

PAD DIAGRAM

NO	PAD NAME	X(um)	Y(um)	NO	PAD NAME	X(um)	Y(um)
1	CH0	-623.50	352.50	9	VSS	623.50	-417.50
2	CH1	-623.50	242.50	10	VDD	623.50	-307.50
3	CH2	-623.50	132.50	11	DIO	623.50	-197.50
4	CH3	-623.50	22.50	12	CLK	623.50	-87.50
5	CH4	-623.50	-87.50	13	START	623.50	22.50
6	CH5	-623.50	-197.50	14	AVDD	623.50	132.50
7	CH6	-623.50	-307.50	15	VSS	623.50	242.50
8	CH7	-623.50	-417.50	16	REF	623.50	352.50



CHIP SIZE=1350 x 950um

Note: The substrate MUST be connected to Vss in PCB layout