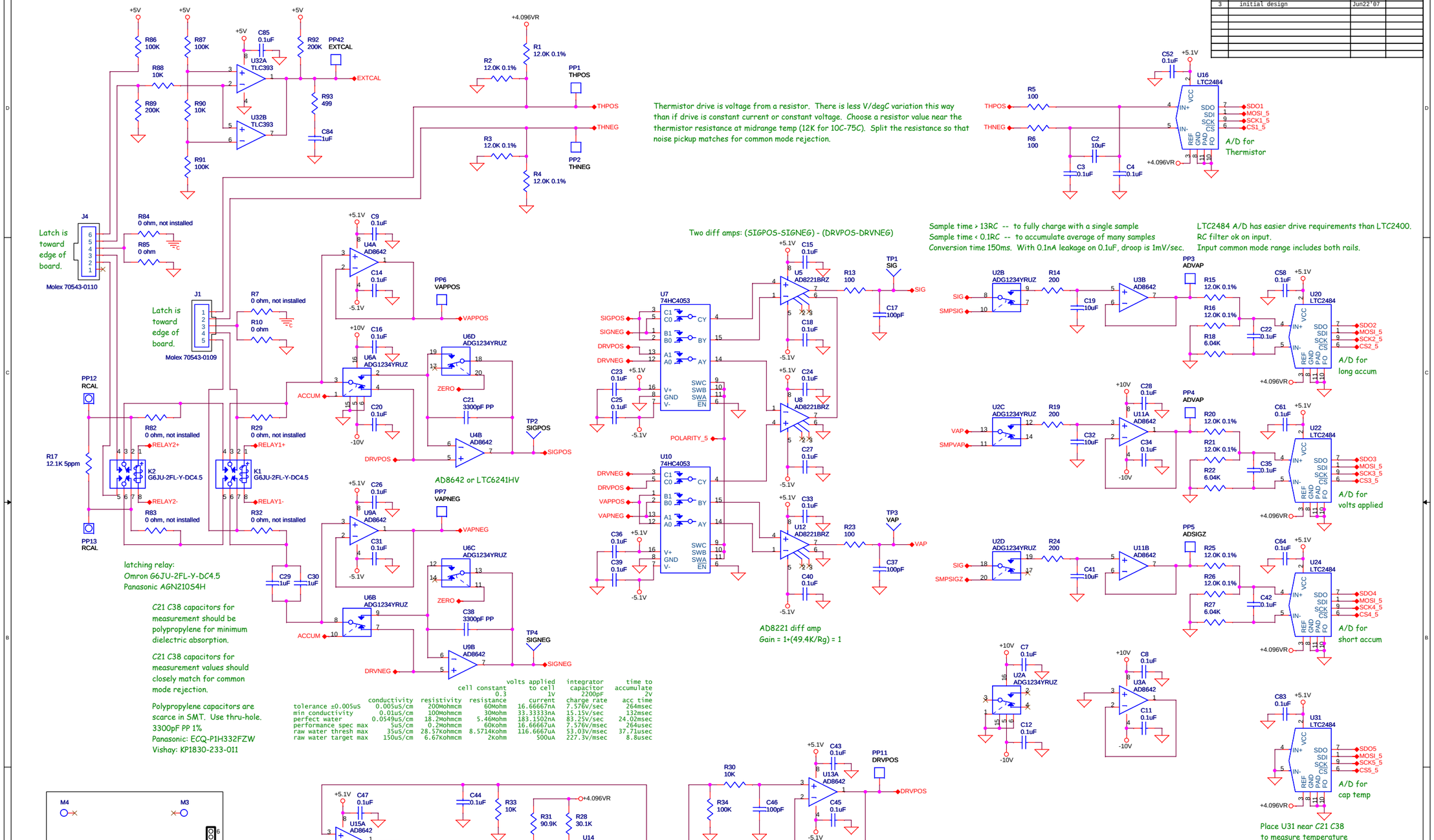
| REVISION HISTORY | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVAL |
| 3 | initial design | Jun22'07 | |

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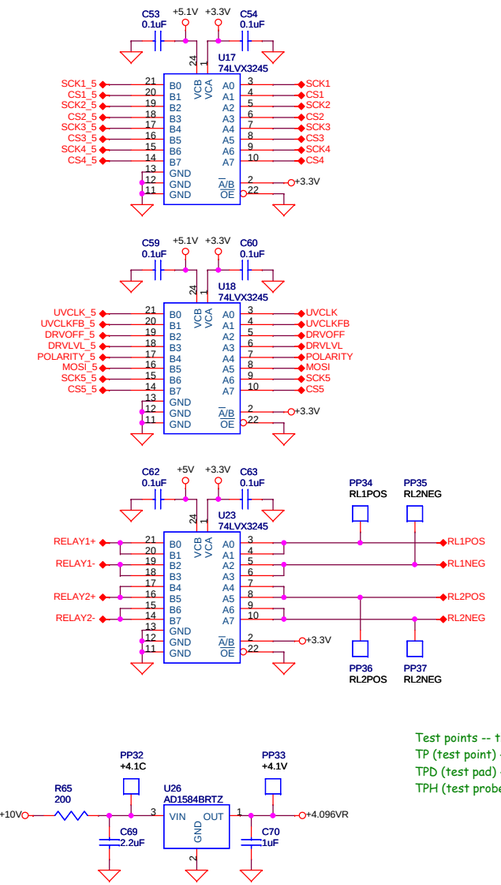
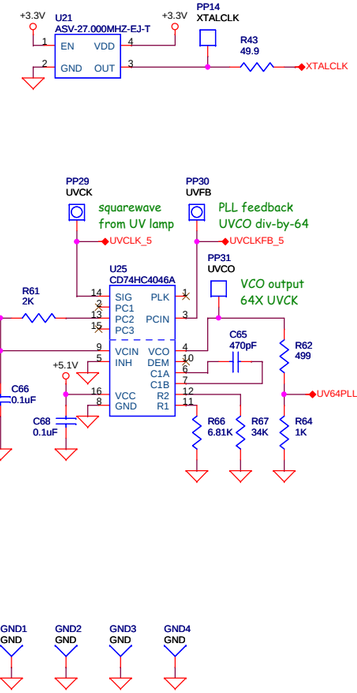
481 California Avenue, Grants Pass, OR 97526

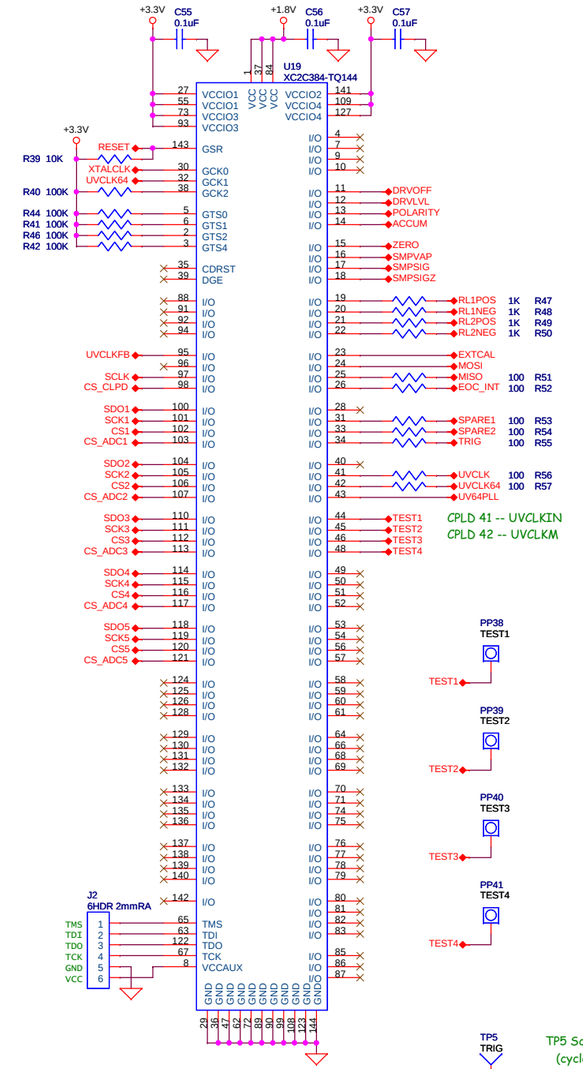
| APPROVALS | DATE |
|---|---|
| Drawn: | |
| Checked: | |
| Engineer: | |

TITLE: TOC analog circuit for Diamond

| SIZE | DWG NO | Rev |
|---|---|---|
| C | AS4002500-98 | 3 |
| SCALE | Friday, June 22, 2007 | SHEET 1 of 2 |

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A/D timing

BitsyX controls the CPLD function by writing a code word to its
SPI port.  These functions are TOC timing sequences for each range,
or let BitsyX do A/D timing (such as during initialization).

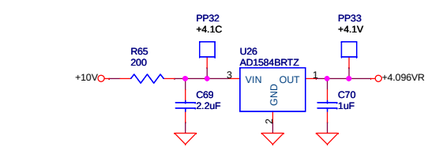
LTC2484 conversion operation begins at the rising edge of CS or
32nd falling edge of SCK, whichever happens is first.  To prevent
early start of conversion, the CPLD holds SCK Hi to the LTC2484
until the end of a TOC sequence.
At the end of a TOC sequence, conversion is started by SCK Lo.
Conversion takes about 150mS.

Because the CPLD must hold CS Lo to all LTC2484s while waiting for
the end of a TOC sequence, each SDO needs a buffer that is enabled
by CS from BitsyX to prevent contention.  This can be done in the
CPLD with a logical mux to a single tristate output for MISO to the
BitsyX.  The logical mux passes the SPI clock only to the selected
LTC2484.

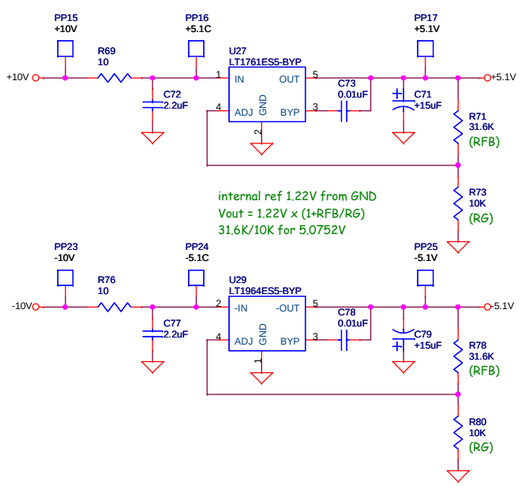
From BitsyX:
SCK is normally Lo.  CS is normally Hi.
On interrupt
  Assert one CS Lo to select a LTC2484.
  Pulse SCK 32 times, read SDO on positive edges of SCK.
  De-assert CS.
  Repeat for each LTC2484.

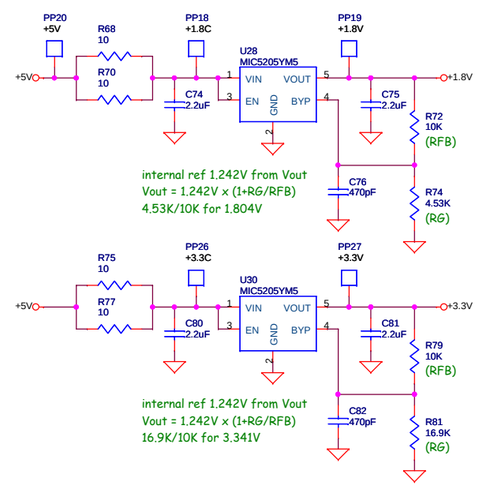
From LTC2484s:
SDO output is enabled when CS is asserted Lo.
SDO data is valid 15-200nS after the falling edge of SCK.
SDO is initially bit31, bit30 after first falling edge of SCK, etc.
Ignore bit31 and bit30.
Bit29 is sign/overflow.  Overflow is indicated by Bit29=Bit28.
Bit28-0 is A/D conversion value, two's complement signed integer.
Bit4-0 is 'noise bits' below the last significant bit.

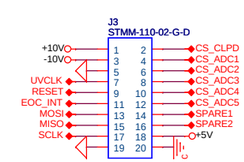
From CPLD:
State_1 -- Wait for CS assert -- (CONVSTART=1 CONVDONE=1)
  Assert EOC_INT while CONVSTART and CONVDONE flags are set.
  CS and SCK pass thru to LTC2484s.
  If in direct control mode then
    BitsyX does at least one read from each LTC2484.
    LTC2484 begins conversion at the end of read.
    When direct control mode ends,
      clear CONVDONE flag -- go to State_4.
  If not in direct control mode then
    When BitsyX asserts CS Lo to any LTC2484,
      clear CONVSTART flag -- go to State_2.
State_2 -- Count SCK pulses -- (CONVSTART=0 CONVDONE=1)
  For each LTC2484:
    BitsyX selects one LTC2484 by holding that CS Lo to CPLD.
    CPLD counts rising edges of SCK.
    CS and SCK pass thru to LTC2484 until . . .
    On 31st rising edge of SCK, CPLD asserts WAIT flag.
    If WAIT, CPLD holds CS Lo and SCK Hi to LTC2484.
    BitsyX reads last bit, then SCK Lo, then CS Hi to CPLD.
  When all LTC2484 WAIT flags are asserted
    and all CS from BitsyX are Hi,
    clear CONVDONE flag -- go to State_3.
State_3 -- Wait for conversion trigger -- (CONVSTART=0 CONVDONE=0)
  BitsyX continues to hold CS Hi and SCK Lo to CPLD.
  On next TOC conversion trigger,
    assert CONVSTART flag -- go to State_4.
State_4 -- Conversion -- (CONVSTART=1 CONVDONE=0)
  BitsyX continues to hold CS Hi and SCK Lo to CPLD.
  Clear all WAIT flags.
  CPLD asserts SCK Lo to all LTC2484s.  Conversion begins.
  CPLD continues to hold CS Lo to all LTC2484s to enable SDOs.
  Each LTC2484 asserts its SDO Lo to CPLD when conversion is done.
  When all LTC2484s are done,
    assert CONVDONE flag -- go to State_1.
```

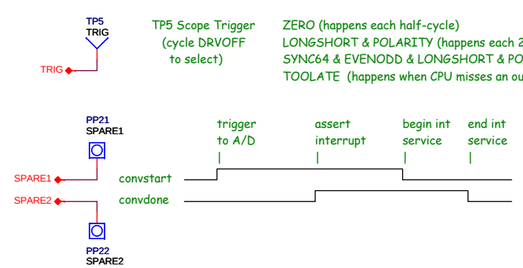



Test points -- three types of test points, identified by the value field
TP (test point) -- 0.040" plated hole with silkscreen and clearance for Components Corp TP105-01-02
TPD (test pad) -- probe contact point, 0.038" square metal pad with 0.052" square silkscreen
TPH (test probe hole) -- same as above with 0.025" hole in the middle of the square pad

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