IP2902 Photographic Record

Photograph of front and back of IP2905 Receiver circuit board.

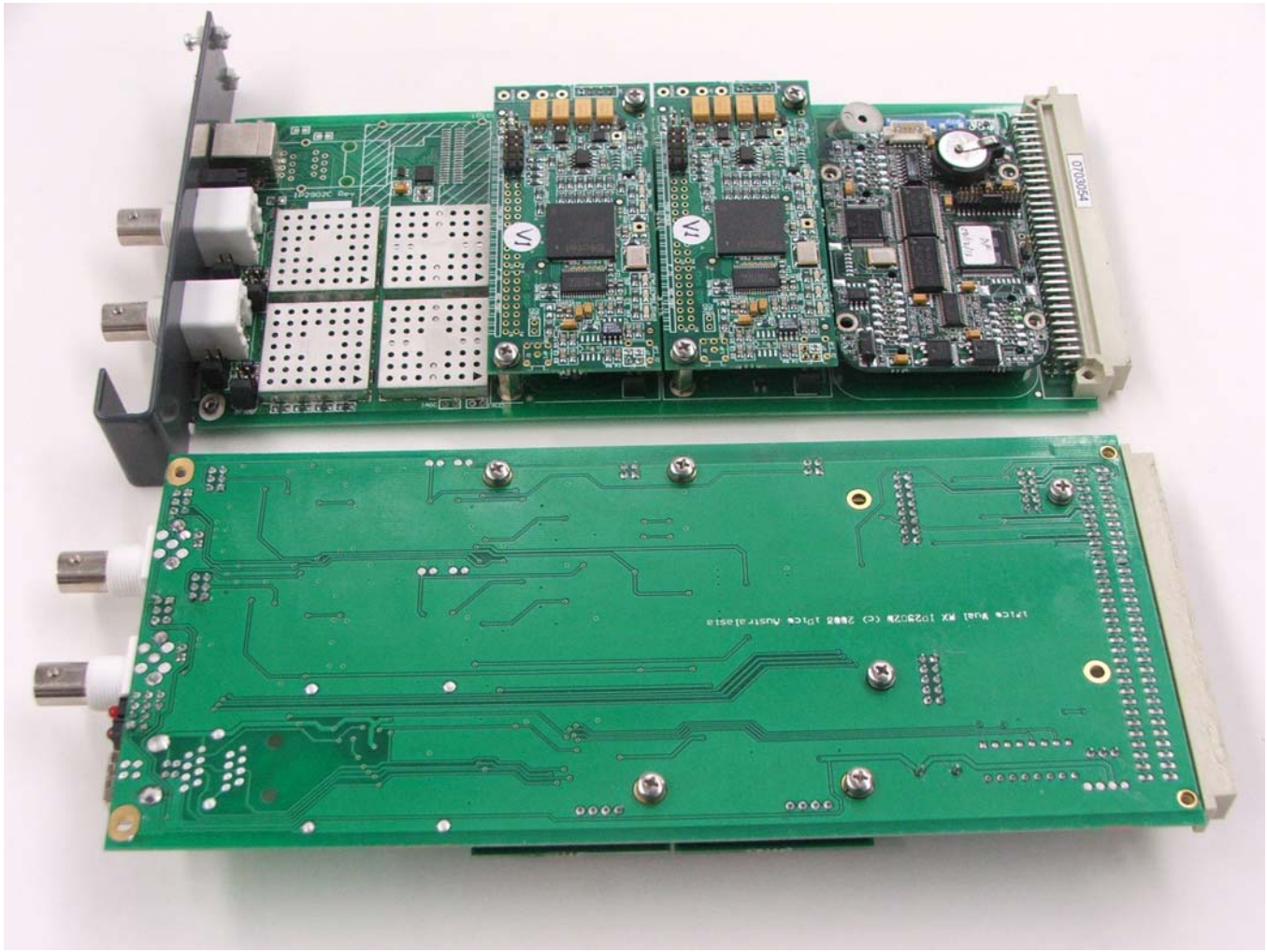
Top Photograph
Input from receiver antennas via BNC connectors.

TRF receiver under metal shields

Dual Digital Signal Processors (V1)

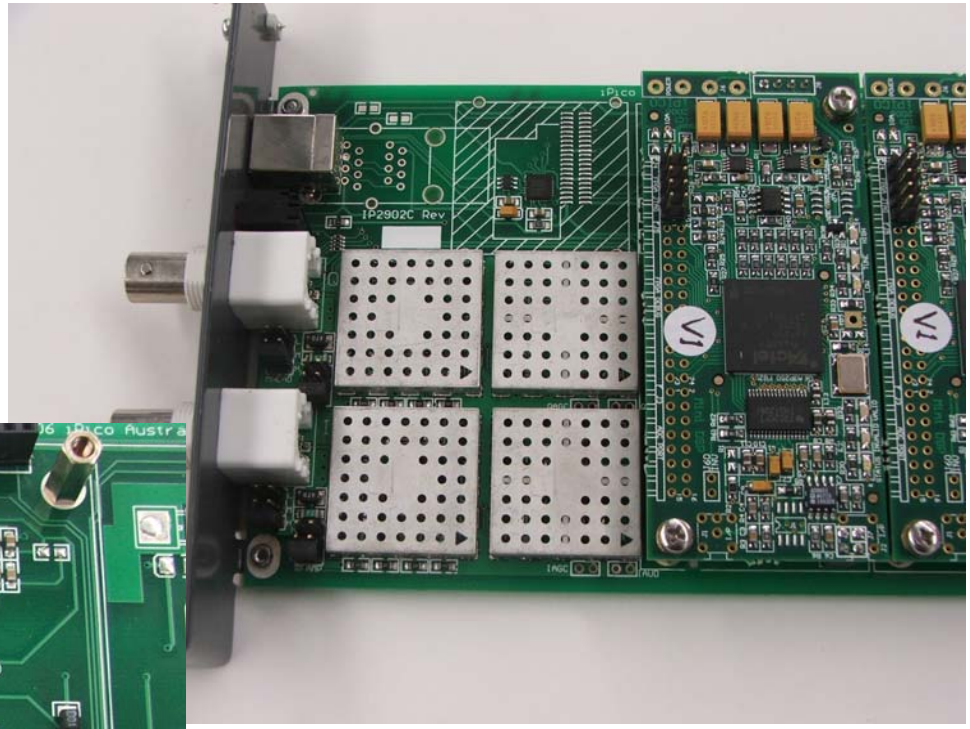
Dual Frequency Tag Decoder.

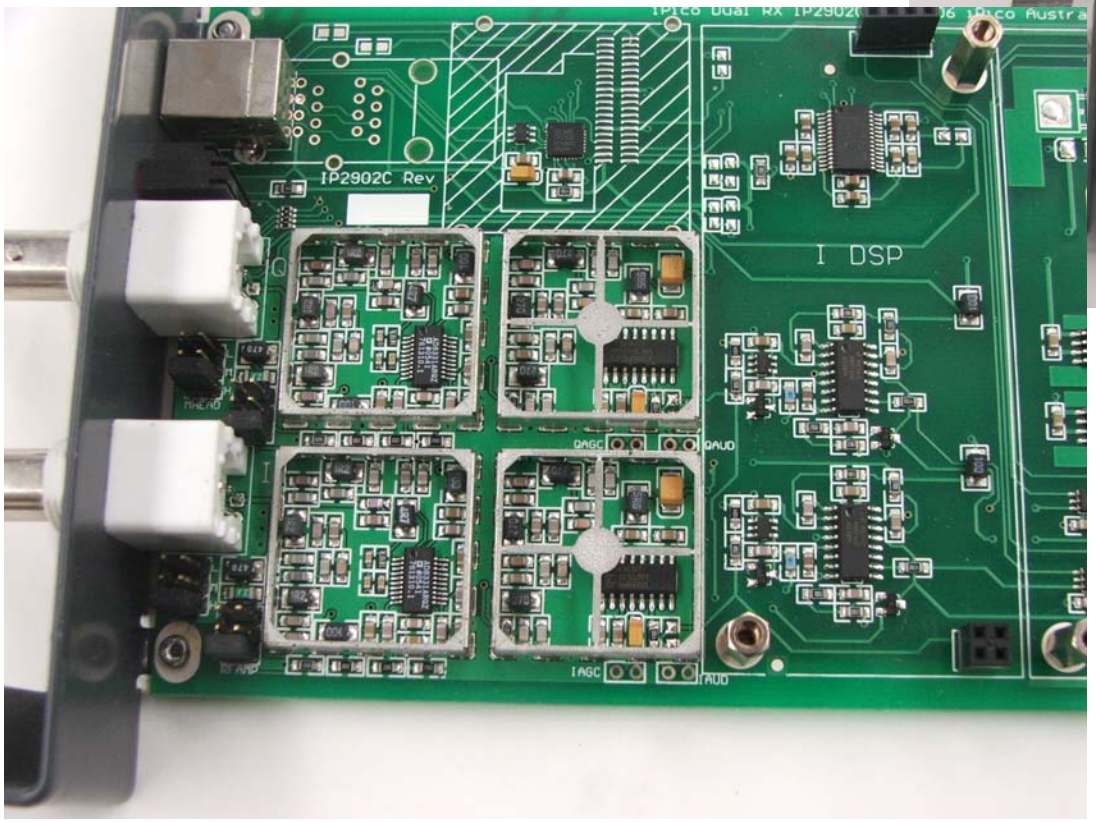
No components are mounted on the rear surface f the receiver pcb.



Dual channel TRF reiver section located under metal shields.

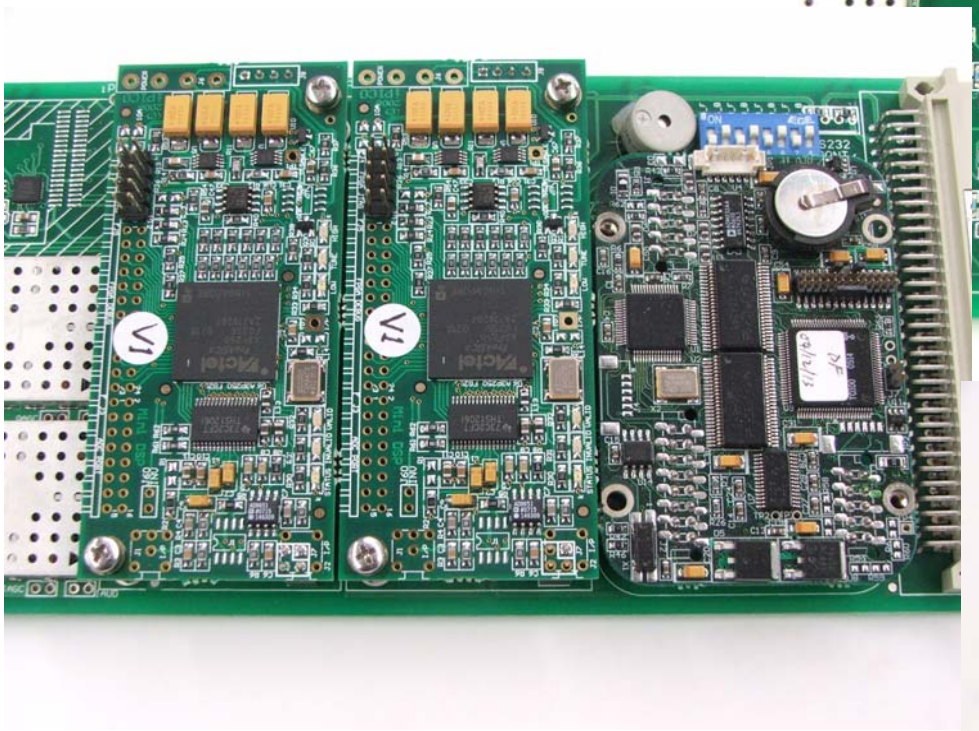
With shields removed - below

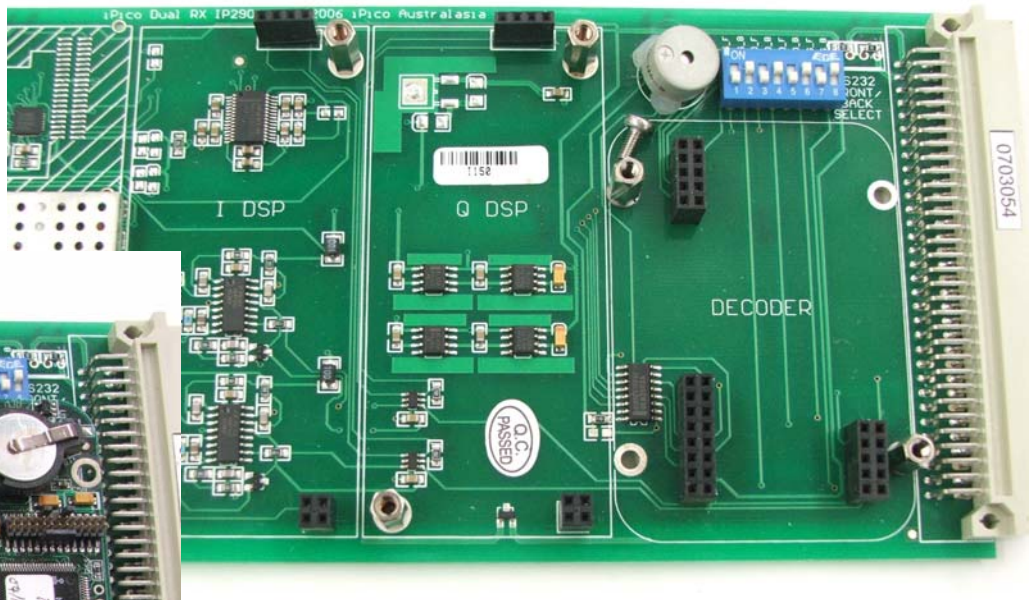


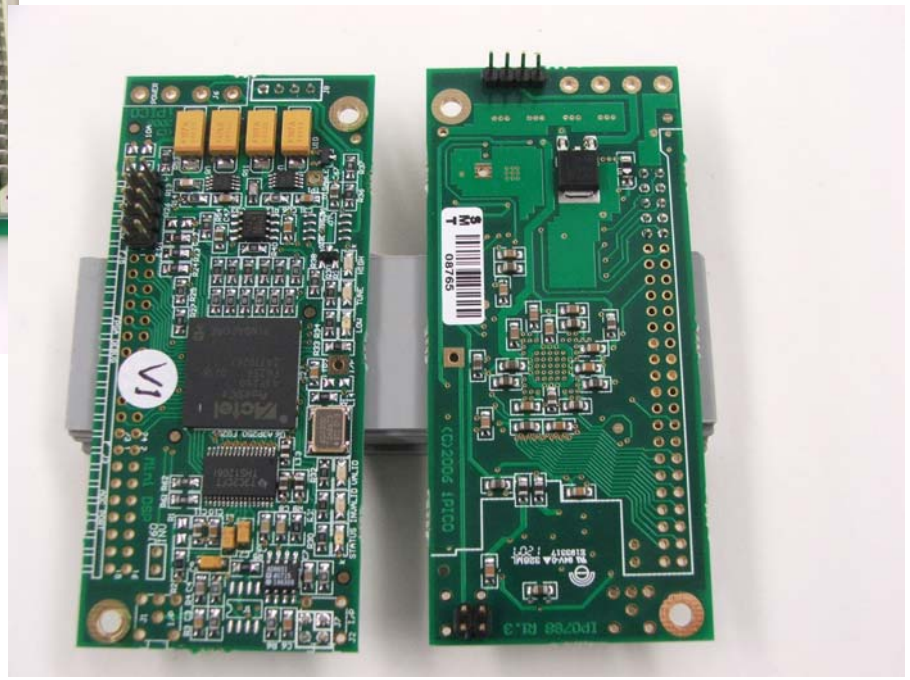


Digital Signal Processor modules Front and Back

Showing location on main pcb and both sides of DSP







FPGA Decoder

Photograph shows front and rear views of pcb