The *CC2430* hardware implementation is shown in Figure 42. Please refer to [1] for further details.

In transmit mode the FCS is appended at the correct position defined by the length field. The FCS is not written to the TXFIFO, but stored in a separate 16-bit register.

In receive mode the FCS is verified by hardware. The user is normally only interested in the correctness of the FCS, not the FCS sequence itself. The FCS sequence itself is therefore not written to the RXFIFO during receive.

Instead, when MDMCTRL0L.AUTOCRC is set the two FCS bytes are replaced by the RSSI value, average correlation value (used for LQI) and CRC OK/not OK. This is illustrated in Figure 43.

The first FCS byte is replaced by the 8-bit RSSI value. See the RSSI section on page 168 for details.

The seven least significant bits in the last FCS byte are replaced by the average correlation value of the 8 first symbols of the received PHY header (length field) and PHY Service Data Unit (PSDU). This correlation value may be used as a basis for calculating the LQI. See the Link Quality Indication section on page 168 for details.

The most significant bit in the last byte of each frame is set high if the CRC of the received frame is correct and low otherwise.

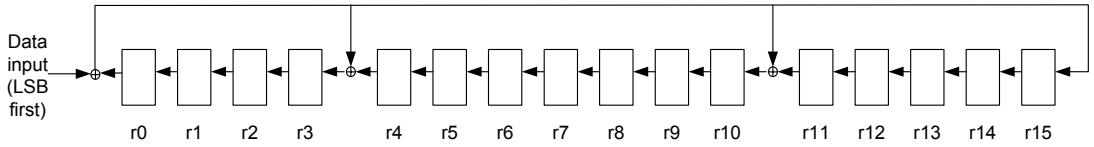

Figure 42: *CC2430* Frame Check Sequence (FCS) hardware implementation [1]

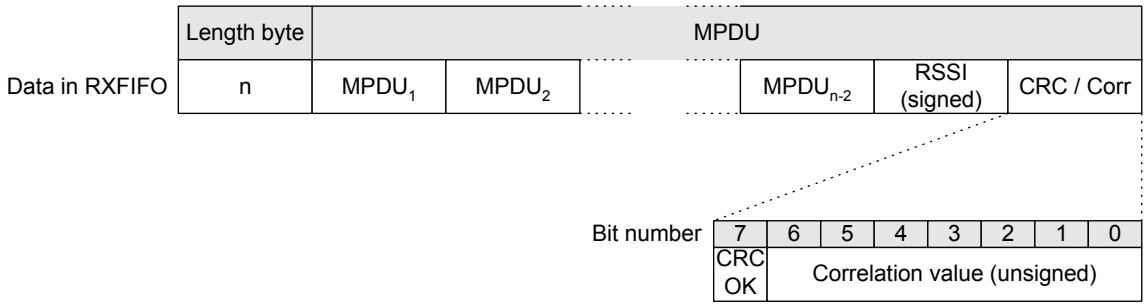

Figure 43: Data in RXFIFO when MDMCTRL0L.AUTOCRC is set

14.17 RF Data Buffering

CC2430 can be configured for different transmit and receive modes, as set in the MDMCTRL1L.TX_MODE and MDMCTRL1L.RX_MODE control bits. Buffered mode (mode 0) will be used for normal operation of *CC2430*, while other modes are available for test purposes.

14.17.1 Buffered transmit mode

In buffered transmit mode (TX_MODE=0), the 128 byte TXFIFO is used to buffer data before transmission. A synchronization header is automatically inserted before the length field during transmission. The length field must always be the first byte written to the transmit buffer for all frames.

Writing one or multiple bytes to the TXFIFO is described in the FIFO access section on page 157. A DMA transfer can be configured to write transmit data to the TXFIFO.

Transmission is enabled by issuing a STXON or STXONCCA command strobe. See the Radio control state machine section on page 166 for an illustration of how the transmit command strobes affect the state of *CC2430*. The STXONCCA strobe is ignored if the channel is busy. See section 14.25 on page 169 for details on CCA.

The preamble sequence is started 12 symbol periods after the transmit command strobe. After the programmable start of frame delimiter

has been transmitted, data is fetched from the TXFIFO.

The TXFIFO can only contain one data frame at a given time.

After complete transmission of a data frame, the TXFIFO is automatically refilled with the last transmitted frame. Issuing a new STXON or STXONCCA command strobe will then cause ***CC2430*** to retransmit the last frame.

Writing to the TXFIFO after a frame has been transmitted will cause the TXFIFO to be automatically flushed before the new byte is written. The only exception is if a TXFIFO underflow has occurred, when a SFLUSHTX command strobe is required.

14.17.2 Buffered receive mode

In buffered receive mode (RX_MODE 0), the 128 byte RXFIFO, located in ***CC2430*** RAM, is used to buffer data received by the demodulator. Accessing data in the RXFIFO is described in the FIFO access section on page 157.

The RF interrupt generated by RFSTATUS.FIFOP and also the RFSTATUS.FIFO and RFSTATUS.FIFOP register bits are used to assist the CPU in supervising the RXFIFO. Please note that these status bits are only related to the RXFIFO, even if ***CC2430*** is in transmit mode.

A DMA transfer should be used to read data from the RXFIFO. In this case a DMA channel can be setup to use the RADIO DMA trigger (see DMA triggers on page 94) to initiate a DMA transfer using the RFD register as the DMA source.

Multiple data frames may be in the RXFIFO simultaneously, as long as the total number of bytes does not exceed 128.

See the RXFIFO overflow section on page 158 for details on how a RXFIFO overflow is detected and signaled.

14.18 Address Recognition

CC2430 includes hardware support for address recognition, as specified in [1]. Hardware address recognition may be enabled or disabled using the MDMCTRL0H.ADDR_DECODE control bit. Address recognition uses the following RF registers

- IEEE_ADDR7-IEEE_ADDR0
- PANIDH:PANIDL
- SHORTADDRH:SHORTADDRL.

Address recognition is based on the following requirements, listed from section 7.5.6.2 in [1]:

- The frame type subfield shall not contain an illegal frame type
- If the frame type indicates that the frame is a beacon frame, the source PAN identifier shall match macPANId unless macPANId is equal to 0xFFFF, in which case the beacon frame shall be accepted regardless of the source PAN identifier.
- If a destination PAN identifier is included in the frame, it shall match macPANId or shall be the broadcast PAN identifier (0xFFFF).
- If a short destination address is included in the frame, it shall match either macShortAddress or the broadcast address (0xFFFF). Otherwise if an extended destination address is included in the frame, it shall match aExtendedAddress.
- If only source addressing fields are included in a data or MAC command frame, the frame shall only be accepted if the device is a PAN coordinator and the source PAN identifier matches macPANId.

If any of the above requirements are not satisfied and address recognition is enabled, ***CC2430*** will disregard the incoming frame and flush the data from the RXFIFO. Only data from the rejected frame is flushed, data from previously accepted frames may still be in the RXFIFO.

Incoming frames are first subject to frame type filtering according to the setting of the MDMCTRL0H.FRAMET_FILT register bit.

Following the required frame type filtering, incoming frames with reserved frame types (FCF frame type subfield is 4, 5, 6 or 7) are however accepted if the RESERVED_FRAME_MODE control bit in the RF register MDMCTRL0H is set. In this case, no further address recognition is performed on