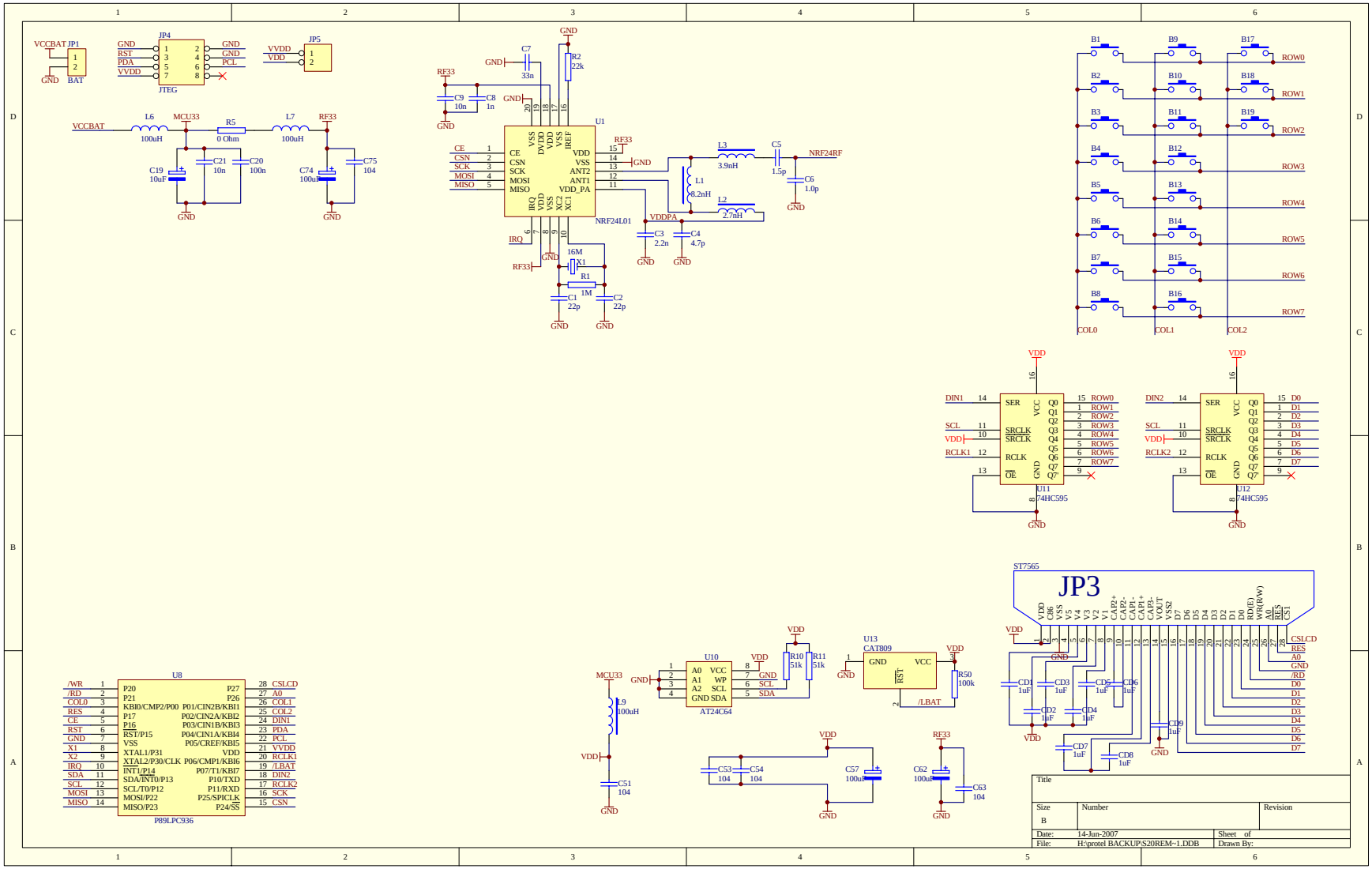
JP1
VCCBAT
GND
BAT
JP4
GND
RST
PDA
VVDD
JTEG
JP5
VVDD
VDD
L6
100uH
MCU33
R5
0 Ohm
L7
100uH
RF33
VCCBAT
C19
10uF
C21
10n
C20
100n
C74
100uF
C75
104
C7
33n
R2
22k
C9
10n
C8
1n
U1
NRF24L01
CE
CSN
SCK
MOSI
MISO
IRQ
VDD
VSS
ANT2
ANT1
VDD_PA
XC1
IREF
L3
3.9nH
C5
1.5p
NRF24RF
C6
1.0p
L1
8.2nH
L2
2.7nH
VDDPA
C3
2.2n
C4
4.7p
16M
X1
R1
1M
C1
22p
C2
22p
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
B13
B14
B15
B16
B17
B18
B19
ROW0
ROW1
ROW2
ROW3
ROW4
ROW5
ROW6
ROW7
COL0
COL1
COL2
U11
74HC595
U12
74HC595
DIN1
DIN2
SCL
RCLK1
RCLK2
SER
SRCLK
RCLK
OE
VCC
GND
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q7'
D0
D1
D2
D3
D4
D5
D6
D7
U8
P89LPC936
/WR
/RD
COL0
RES
CE
RST
GND
X1
X2
IRQ
SDA
SCL
MOSI
MISO
P20
P21
KBI0/CMP2/P00
P17
P16
RST/P15
VSS
XTAL1/P31
XTAL2/P30/CLK
INT1/P14
SDA/INT0/P13
SCL/T0/P12
MOSI/P22
MISO/P23
P27
P26
P01/CIN2B/KBI1
P02/CIN2A/KBI2
P03/CIN1B/KBI3
P04/CIN1A/KBI4
P05/CREF/KBI5
VDD
P06/CMP1/KBI6
P07/T1/KBI7
P10/TXD
P11/RXD
P25/SPICLK
P24/SS
CSLCD
A0
COL1
COL2
DIN1
PDA
PCL
VVDD
RCLK1
/LBAT
DIN2
SCK
CSN
U10
AT24C64
A0
A1
A2
GND
VCC
WP
SCL
SDA
R10
51k
R11
51k
U13
CAT809
RST
/LBAT
R50
100k
L9
100uH
C51
104
C53
104
C54
104
C57
100uF
C62
100uF
C63
104
ST7565
JP3
VDD
C96
VSS
V5
V4
V3
V2
V1
CAP2+
CAP2-
CAP1-
CAP1+
CAP3-
VOUT
VSS2
D7
D6
D5
D4
D3
D2
D1
D0
RD(E)
WR(R/W)
A0
RES
CS1
CSLCD
RES
A0
GND
/RD
D0
D1
D2
D3
D4
D5
D6
D7
CD1
1uF
CD2
1uF
CD3
1uF
CD4
1uF
CD5
1uF
CD6
1uF
CD7
1uF
CD8
1uF
CD9
1uF
Title
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B
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Revision
Date:
14-Jun-2007
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File:
H:\protel BACKUP\S20REM~1.DDB
Drawn By: