

This document is designed to provide general information for use of the WISE100 Module. .

Guidelines

FCC Part 15

THIS DEVICE COMPLIES WITH PART 15 OF THE FCC RULES. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS:

- (1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE, AND
- (2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED, INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRED OPERATION.

Specifications

Dimensions Connector

Mated Height requirement is 0.36 inch or 9.15 mm

Samtec CLP-114-02-L-D mating connector is required. Space for connector on PCB (4.57 mm or .180 inch) x (18.21 mm or .717 inch)

See the section on shield size

Module Power Consumption Profile

The Riga WISE100 module has a continuous background current of 1.5uA

During transmission on average it will consume 165mA for 150ms.

GPIO

17 GPIO connections (with alternate functions) are available on the module. (See the module connector pin-out diagram below.) These GPIO pins can take at a maximum 3.3v. Voltages exceeding this amount will result in damage to the module circuitry, and will void the warranty on the product.

Power Supply

The module uses 3.3VDC power. The power supplied to the module should have a voltage **ripple less than or equal to 4 mV peak to peak.**

PCB material and layout considerations

It should be noted that all RF module will be affected badly by noise in its power. The PCB design should take RF noise reductions techniques into account. The mating PCB should use FR-4 glass epoxy. All components on the board should have decoupling capacitors to reduce any transient interruptions in the power supply. The decoupling capacitors should be placed as closely as possible to each component they are decoupling. Long thin traces should be avoided as they can create inductance and as a result noise.

The layout of components and tracks on the board should be placed so that there are no traces, and or components under the ceramic antenna of the Riga-Module. Specifically there should be no components or tracks within 1.5 cm of the antenna located on in the corner of the module.

Inter chip communication

Existing systems that have serial communication will typically connect the TTL tx and rx pins to the microcontroller in the existing PCB. GPIO 9 and 10 are used for this function.

Existing systems that have or require SPI interface will typically connect via GPIO pints 0,1, and 2

Wakeup / Interrupt

(GPIO 8, 14, 15, 16) is reserved as an external interrupts. These Pins may be used to wakeup the Riga Module when the Maxinet Microcontroller comes out of sleep and/or detects a change in environment settings.

Addressing / DIP switches

Typical communication requires the assignment of an address, or multicast ID that is assigned via dip switch, or software configuration. Module addresses and multicast ID's can be assigned at the time of manufacturing or later during product manufacturing. If a dip switch is used, the required number of GPIO pins may be used to identify the address or multicast ID. One side of the dip switch should be attached to 3.3 VDC through a pull up resistor. The other side of the dip switch should be attached to ground.

Firmware

Riga can provides customized firmware on the module for our customers. A quote on your specific requirements can be provided.

Antenna

The module contains an on board "F" antenna.

Other Features

The module is RoHS compliant.

FCC approved (documentation available on request)

IC approved (Documentation available on request)

The module has a built in industry standard 128 bit AES compliant encryption engine.

Riga WISE1000 Module Connector Pin-out:

Samtec Connector CLP-114-02

VBRD	1	2	VBRD
GPIO[1]	3	4	GPIO[2]
GPIO[12]	5	6	GPIO[0]
GPIO[3]	7	8	GPIO[11]
GPIO[5]	9	10	GPIO[4]
GPIO[7]	11	12	GPIO[6]
GPIO[9]	13	14	GPIO[8]
RSTB	15	16	GPIO[10]
GND	17	18	GND
SIF_CLK	19	20	SIF_MISO
SIF_MOSI	21	22	SIF_LOADB
GPIO[16]	23	24	GPIO[15]
GPIO[14]	25	26	GPIO[13]
GND	27	28	GND

Overview of Connector Features

VBRD – 5 or 3.3 VDC (Module # dependent)

SPI – GPIO 0,1,2

I2C – GPIO 1,2

UART – (RS 232/485) GPIO 9,10

ADC (Analog to Digital Converts) – GPIO 5,4,6,7, (0-3.3 volts, Input 12 bit resolution)

Timers – 2 16 bit general purpose timers and 1 16 bit sleep timer.

Digital I/O – GPIO 1-17

Hardware Interrupts – GPIO 8, 14, 15, 16

SPI interface:

Master out 6

Master in 3

Master Clock is 4

UART

Modules TX is pin 13

Modules RX is pin 16

Wake-up

Module pin number 24 - Wake up Device

Module pin number 25 - Wake up module