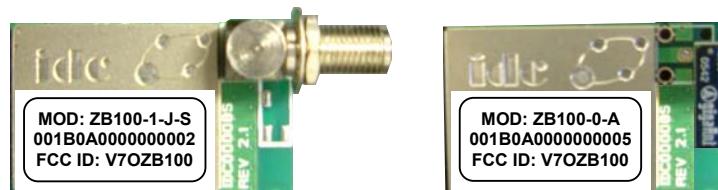
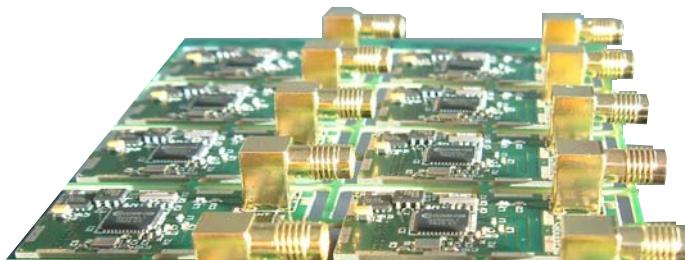




ZigBee Ready OEM Modules ZB100 - *

Compact 2.4GHz 802.15.4 / ZigBee Ready
Modules for Wireless Networking Applications in
Industry

Product Datasheet





Document Revision

Document History

Version	Date	Author	Description of Changes
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Introduction

The ZB100 range of OEM Modules from Intelligent Distributed Controls Limited, have been designed around the CC2430/CC2431 System on Chip (SoC) single chip solutions from Texas Instruments. The range of RF transceiver modules are available with various RP-SMA, SMA and chip antenna configurations, and are supplied in a pin header footprint common to all variants.

All modules are capable of supporting the industry leading ZigBee protocol stack (Z-Stack™) from Texas Instruments, for wireless point-to-point, star, tree and mesh networks based on the IEEE 802.15.4 compliant PHY and MAC layers, and providing 16 channels in the 2.45GHz licence-free ISM band. The shielded module is only 21.6 x 35 mm in board area, 3.5mm thick excluding the pin headers and SMA or RP-SMA RF connector. The module footprint also includes a MAC address chip (each device being unique). In addition to the nominal 3.3V chip level supply (2.0 to 3.6V) for battery applications, the modules also contain an isolated regulator allowing the device to be powered from industrial power supply voltages anywhere between 4 and 30V, making the device ideal for industrial sensor applications.

Applications

- Home control and industrial automation
- Industrial monitoring
 - Machinery condition monitoring – vibration, temperature etc.
 - Environmental monitoring – temperature, humidity, pressure, vibration, flow
- OEM wireless devices
- Asset tracking and inventory management
- Building automation / management
 - Lighting
 - Temperature
 - Smoke/CO detectors
- Wireless barcode and tag reading
- Remote metering
- Security –
 - Access control
 - Role calling

Key Features

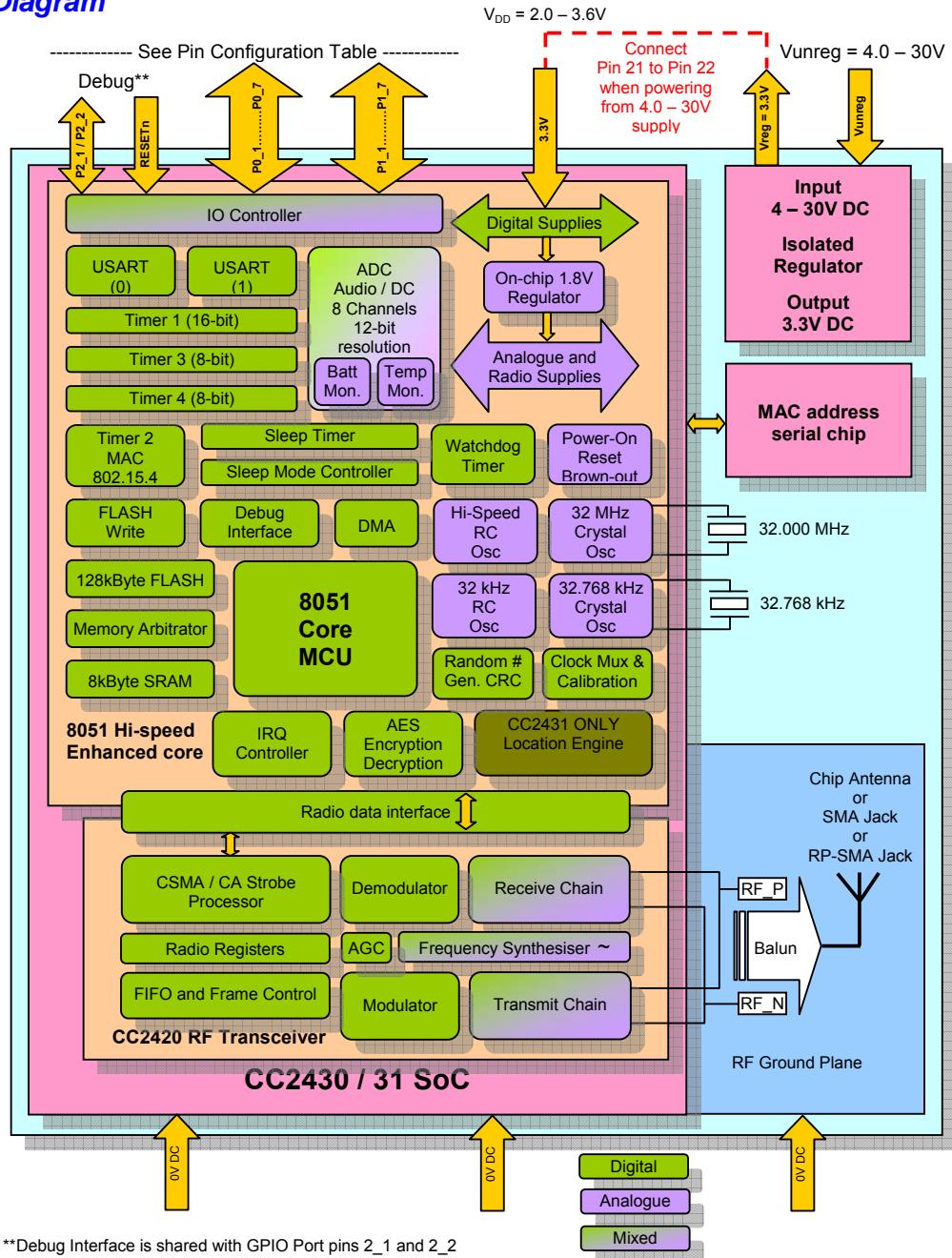
- Compact Design – all shielded modules have the same 21.6 x 35 mm board area footprint, antenna ready
- 2.0 – 3.6V supply voltage extending to 30V when using the on board isolated regulator
- On board unique MAC address chip
- Optional CC2431 SoC which includes a location detection hardware module
- Industry leading CC2420 RF transceiver core, IEEE 802.15.4 compliant
- FCC CFR 47 Part 15 (US) and ETSI EN 300 440 (EU) Certified for Unlicensed Operation
- 128kB FLASH, 8kB SRAM (4kB with data retention in all power modes) Memory space for Full-Funtion Device (FFD)
- Certified for use with up to 9dBi dipole omnidirectional antenna (FCC restricted on channel 26 – see FCC Restrictions)
- AES security coprocessor
- Hardware programming and debug support using the Texas Instruments development kit
- Digital RSSI and optional harware location engine (CC2431)
- Over-the-air (OTA) programming capability
- 32.768kHz crystal controlled RTC
- 32MHz high speed 8051 core MCU with wide range of configurable IO interfaces
 - Powerful DMA
 - Watchdog Timer
 - 802.15.4 MAC timer, 16 bit timer and two 8 bit timers, random number gen.
 - Battery monitor and temperature sensor
 - 20 general purpose IO lines available on pin header with 20mA sink/source on two pins
 - 12-bit ADC with up to 8 inputs and configurable resolution
 - 2 configurable UART / SPI interfaces
- Very low power –
 - With 8051 core running at 32MHz and radio enabled, RX = 27mA, TX = 27mA
 - 0.5 µA in powerdown mode, where external interrupts or the RTC can wake up the system
 - 0.3 µA in stand-by mode, where external interrupts can wake up the system
 - Very fast wake-up from low power modes to active mode

Module Description

System-on-Chip (SoC)

The CC2430 System-on-Chip is provided by Texas Instruments, and combines the market leading CC2420 RF transceiver (Chipcon / Ti), with an industry standard high-performance and peripheral enhanced 8051 micro-controller unit (MCU). With the memory arrangement provided on the ZB100, and the ability to support the industry leading ZigBee protocol stack (Z-Stack™) from Texas Instruments, this module range forms the basis for design solutions from the bottom "end-device", right through to the most complex "full-function device" requirements. Below provides a detailed view of the SoC complete with all peripherals, and additional components forming the ZB100.

Block Diagram





CC2431 – Location Engine

The CC2431 System-on-Chip is identical to the CC2430 in respect of MCU, memory, peripherals and radio operation, with the addition of a hardware location detection module – microcode in silicon. This can be used in applications requiring location management e.g. asset tracking. Mobile devices (blind nodes – unknown position) receive signals from nodes with known locations. Based on the varying signal strengths from received from these fixed nodes, the location engine calculates an estimate of its own position.

Accuracy of 3 to 5 metres in typical applications can be achieved. Coverage is approximately 64 x 64 metres, with a location estimate resolution of 0.5m. The time to perform the calculation takes less than 40µs, and requires minimal CPU loading, as the calculations are performed in microcode. Once the result has been calculated, this can then be reported as an X/Y coordinate back through the network to say a PC for visual representation.

Voltage Regulators

The ZB100 module can be powered from two sources, both referenced to the modules 0V ground connections.

- 1) Battery / 3.3V DC source (V_{DD}). This is the SoC digital chip supply and can be anywhere between 2.0 and 3.6V, and is primarily intended for battery powered applications. This provides power to all digital elements of the SoC, and also the Serial / MAC integrated circuit.
- 2) Higher voltage DC source (V_{unreg}). This connects to an isolated linear 3.3V regulator, which accepts DC input in the range of 4.0 to 30V, making it ideally suited to industrial applications. The output of the isolated regulator is then linked (on the OEM board) into the Battery / 3.3V DC source, providing the required 3.3V for the SoC.

In addition, there is a 1.8V analogue regulator internal to the SoC powered from the, which provides power to the analogue sections and RF radio sections of the device. This is self-contained, and the 1.8V regulated output is not made available for any external devices.

MCU Core

The CC2430/31 SoC contains an enhanced 8051 micro-controller with the core CPU running at 32MHz. This operates the standard 8051 instruction set on 1 cycle per instruction as opposed to the standard 12 cycles per instruction.

Memory

The onboard memory of the ZB100 consists of the following:

FLASH

128kByte of FLASH memory divided into 64 pages of 2kbyte each. This is the smallest erasable unit in memory, whilst the smallest writable element is 32 bytes. The worst case FLASH memory endurance is 1000 erase/write cycles. Programming can be performed from within resident firmware, or over the 2-wire debug interface. Over-the-air programming is possible and available on the ZB100. FLASH sectors can be locked for security and auto powers down during low frequency CPU read access.

SRAM

A total of 8192 bytes of data memory is provided on chip, divided into two 4096 byte sectors, with the upper sector having data retention in all power modes, and the lower sector with retention in active and power mode 1 only.

ROM

The ROM is a 64bit 1-wire serial device that communicates over a single IO pin of the SoC. This provides a unique identity for the ZB100 module, with the option for this to be a complete UID-64 bit MAC address, which contains the IEEE assigned 24-bit company identifier (Intelligent Distributed Controls Ltd. = 001B0AH), and a 40-bit node address.



Off-board Memory

Additional memory may be connected to the ZB100 via a serial port configured in SPI mode. Up to 2Mbyte of extra FLASH may be added in this way.

DMA Controller

A powerful DMA controller is provided which can be used to relieve the processor from data movement thereby improving the overall processing efficiency. The DMA controller can move data from/to a peripheral unit to/from memory with minimal CPU intervention. The DMA controller controls data exchange over the entire range of the XDATA memory space, and since most of the SFRs are mapped into the XDATA memory space, data transfers to/from peripherals can be manipulated. Use of the DMA can also reduce power consumption by keeping the CPU in a low power mode, whilst moving data to or from a peripheral unit. The main features of the DMA controller are given below:

- Five independent DMA channels
- Three configurable levels of DMA channel priority
- 31 configurable transfer trigger events
- Independent control of source and destination address
- Single block and repeated transfer modes
- Supports length field in transfer data setting variable transfer length
- Can operate in word or byte size modes

GPIO

The CC2430/31 provides three 8-bit ports of general purpose IO – Ports 0, 1 and 2. Ports 0 and 1 are complete 8-bit wide ports (P0_0 P0_7; P1_0 P1_7), and are available on the ZB100 header. Port 2 has only 5 usable elements, two of which are taken by the 32.768 kHz crystal for RTC applications, and P2_0 is directly interfaced to the serial number integrated circuit (MAC address). This leaves P2_1 and P2_2 brought out to the ZB100 header as two further general purpose IO pins. P2_1 and P2_2 are also used for the debug interface – see later.

All ports are both bit and byte addressable, and each port pin can be configured to operate as either a general purpose IO or as a peripheral IO.

Each port pin has the following configurable features:

- Output drive current of $\pm 4\text{mA}$ (Sink/Source), with the exception of P1_0 and P1_1 which are high current drives providing $\pm 20\text{mA}$ capability
- Configurable $20\text{k}\Omega$ pull-up or pull-down or tri-state when configured as an input with the exception of P1_0 and P1_1
- Retention of IO mode and output value when in lowest power modes
- GPIOs configured as inputs can be used to generate inputs
- GPIOs (Port0 and Port1) configured as inputs can each be associated with one DMA trigger for immediate transfer to a mapped XDATA location on input transition changes
- Four radio test signals can be output on port pins P1_4 to P1_7
- Peripheral units have two alternative port locations to maximise port utilisation and minimise pin selection conflicts

Unused IO pins should either be configured as outputs or as inputs with the pull-up resistor configured. In both cases unused pins should not be connected to V_{DD} or 0V to avoid excessive current consumption.



ADC

The ADC supports up to 12-bit analogue to digital conversion via a multiplexer which accepts up to eight single-ended channels through the GPIO interface. Two further internal channels are provided – on chip temperature sensor, and a battery monitor input which is essentially the V_{DD} supply divided by 3, for an early warning detection of battery failure. In addition a positive reference voltage multiplexer / selector can be programmed to choose between an on-chip reference voltage, the analogue voltage supply, a single ended external reference via AIN7, or a differential external reference via AIN6-AN7. The ADC features are as follows:

- Selectable decimation rates (7, 9, 10 and 12 bits)
- Eight individual single-ended input channels, which may be paired for differential signals
- Reference voltage, selectable between internal, single-ended external, differential external or $AVDD_SOC (V_{DD})$
- Interrupt request generation
- DMA triggers at end of conversions
- Temperature Sensor input
- Battery Monitor Input

Temperature Sensor

The temperature sensor provides a further additional channel to the ADC. This provides a voltage measurement relative to temperature over the temperature range of -40° to $+80^{\circ}\text{C}$. This provides an on-chip temperature reading accuracy of $\pm 2^{\circ}\text{C}$ over the temperature range of -20° to $+80^{\circ}\text{C}$ once a calibration has been performed at room temperature. The actual voltage reading for a given temperature is based on the temperature coefficient of $2.45\text{mV}/^{\circ}\text{C}$ calculated from the room calibration point.

Battery Monitor

The battery monitor $AVDD_SOC/3$ provides a further additional channel to the ADC. This provides a linear relationship to the SoC supply (V_{DD}), thereby providing the ability (using a threshold value) to detect early warning of low-supply/battery status.

Timers

A total of six timers are provided by the SoC with varying configurable attributes as follows:

Timer 1 (16-bit)

Timer 1 may be used for a wide variety of control and measurement applications (input capture, output compare and PWM) with the ability to perform motor control functionality. The main features of Timer 1 are as follows:

- Three capture/compare channels
- Rising, falling or any edge capture
- Set, clear or toggle output compare
- Free-running, modulo or up/down counter operation
- Clock pre-scaler for divide by 1, 8, 32 or 128
- Interrupt request generated on each capture/compare and terminal count
- DMA trigger function



Timer 2 (MAC)

The MAC timer is mainly used for general time keeping in the 802.15.4 MAC layer, providing timing for the CSMA-CA algorithms. The main features of the MAC timer are as follows:

- 16-bit up-counter providing symbol/frame periods of 16 μ s/320 μ s
- Adjustable period with accuracy of 31.25ns
- 8-bit timer compare function
- 20-bit overflow count
- 20-bit overflow count compare function
- Start of Frame Delimiter capture function
- Timer start/stop synchronous with 32.768 kHz clock and time keeping maintained by Sleep Timer
- Interrupts generated on compare and overflow
- DMA trigger capability

Timers 3 and 4 (8-bit)

Timers 3 and 4 support typical requirements such as output compare and PWM functions, or basic software timing requirements. The main features of Timer 1 are as follows:

- Two compare channels
- Free-running, modulo or up/down counter operation
- Clock pre-scaler for divide by 1, 2, 4, 8, 16, 32, 64 or 128
- Interrupts generated on compare and terminal count
- DMA trigger capability

Watchdog Timer

The watchdog timer consists of a 15-bit counter clocked by the 32.768 kHz crystal oscillator. This provides a means of resetting the processor if it fails to reset the watchdog within the selected period through software. This may happen where the application is subject to an electrically noisy environment, power glitches etc. or where high reliability of the software is required. The watchdog timer provides the following features:

- Four selectable time intervals – 1.9 ms, 15.625 ms, 0.25 s, 1 s.
- Watchdog Mode (Generates CPU reset if timed out)
- Timer Mode (Generates Interrupt only if timed out)
- Independent from system clock

Sleep Timer

The sleep timer is used to set the interval from entering the low power sleep state and returning to active mode.

- 24-bit up counter driven from the 32.768 kHz oscillator.
- 24-bit compare for waking through interrupt
- Low power mode operation in PM2
- Maximum period = 512 seconds (approx.8.5minutes)

USARTs

Two serial communication USARTs are provided on the SoC – USART(0) and USART(1). These can be operated and configured separately into either UART (asynchronous) or SPI (synchronous) modes. Both USARTs have identical functionality, but are configured on separate port pins. A second “alternative” configuration is also possible providing more efficient use of the port pins for peripheral use.



UART

UART mode provides an asynchronous serial communications interface consisting of two or four wire (TxD, RxD and optionally CTS and RTS). In addition standard GPIO pins can be configured to provide further modem functions e.g. DSR, DTR and CD, as these can be interrupt configured.

Each UART provides the following features:

- 8 or 9 data bits
- Odd, even or no parity
- Configurable Start and Stop bit level
- Configurable LSB or MSB first transfer
- Independent receive and transmit interrupts
- Independent receive and transmit DMA triggers
- Parity and framing error status
- Up to 230,400 bps data speed, configurable via an internal baud rate generator derived from the system clock

SPI

SPI mode provides a synchronous serial communication interface through either a 3-wire or 4-wire interface. The full 4-wire interface consists of the following pin functions:

- MOSI – Master Out Slave In
- MISO – Master In Slave Out
- SCK – Serial Clock
- SSN – Slave Select

The SPI mode provides the following features:

- Selectable 3-wire or 4-wire interface
- Master or Slave presentation
- Configurable SCK polarity and phase, SCK speed is configured via an internal baud rate generator derived from the system clock
- Configurable LSB or MSB first transfer

When selected for Slave presentation (4-wire mode), the SSN pin is used as an edge triggered chip-select input.

Random Number Generator / CRC

The Random Number Generator is a 16-bit linear feedback shift register (Polynomial $X^{16} + X^{15} + X^2 + 1$) and provides the following features:

- Generates pseudo-random bytes for either use by the firmware, or by the Command Strobe Processor CSMA / CA
- Calculate CRC16 of bytes written to the upper Random Number Generator register
- Seeded by value written to the lower Random Number Generator register twice – Usually for standard CRC16 calculations, the seed value is either 0x0000 or 0xFFFF.

AES Coprocessor

The data encryption is performed by a dedicated co-processor contained in the SoC silicon which supports the Advanced Encryption standard, AES. This allows encryption/decryption to be performed with minimal CPU intervention. This coprocessor provides the following features:

- Supports all security suites in the IEEE 802.15.4 standard
- ECB, CBC, CFB, OFB, CTR and CBC-MAC modes with hardware support for CCM mode
- 128-bits key and IV/Nonce, and DMA transfer trigger capability

The AES coprocessor can add security to wired links (UART / SPI) but primarily is intended for the wireless link. AES encryption is performed on blocks of data (128-bit wide), prior to transmitting a packet payload over the radio, and AES decryption after receiving a payload packet.

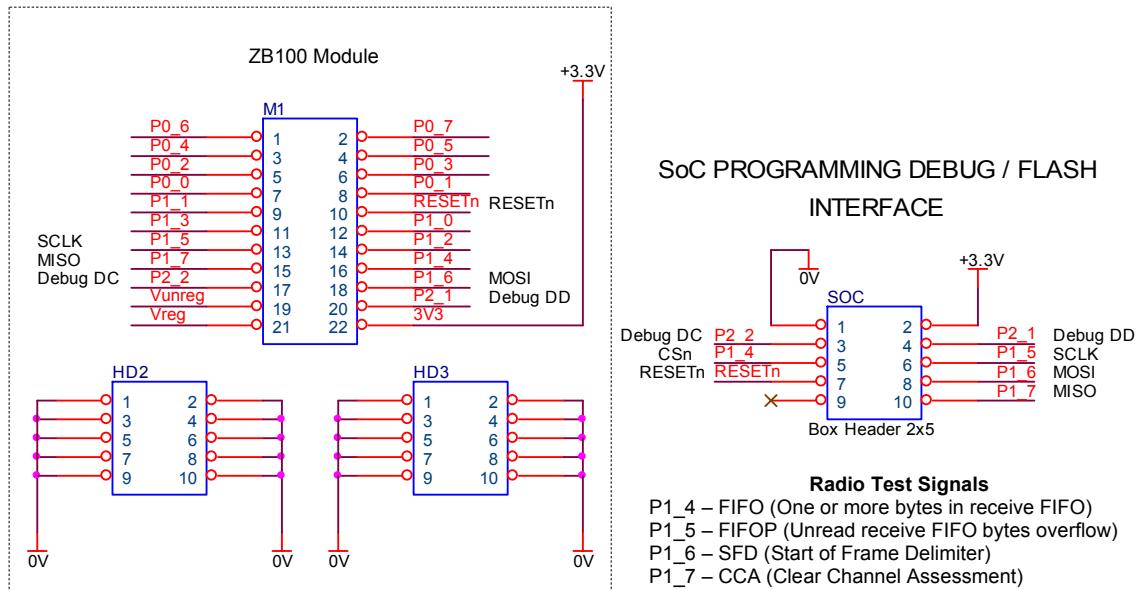
Ref [4] for further detail on AES operation.

2-wire Debug Interface

The Debug Interface operates a proprietary 2-wire serial interface used for in-circuit debugging. Through this interface it is possible to erase and write (program) the FLASH memory, and debug by controlled program execution (stop/start, single stepping, breakpoints etc.).

The 2-wire debug interface shares with two GPIO port pins, and the debug mode is entered by a specific operation of the debug clock in conjunction with the precessor RESETn pin. When not in debug mode, the port pins revert back to standard general purpose IO pins.

The following details are for providing a programming interface for use with the Texas Instruments CC2430 Development Kit – CC2430DK. This uses a 10-way ribbon interface for programming and debugging the SoC. In addition, this example interface can also provide a single SPI port. Alternatively Radio Test signals can be configured to be outputs on the Port Pins P1_4 to P1_7 as given below.



MAC Address

The MAC address can be either hard-coded into FLASH, or take the address from the on-board 1-wire serial device connected to the CC2430/31 Port P2_0. This device can be either a generic 24-bit serial number, or a user specific EUI-64 global identifier whereby the first 24-bits provide the OUI, and the remaining 40-bits provide the serialisation. The IEEE assigned OUI for Intelligent Distributed Controls Limited is 00-1B-0A.

OEMs may hardcode their own UID and serialisation or take the Intelligent Distributed Controls OUI as appropriate

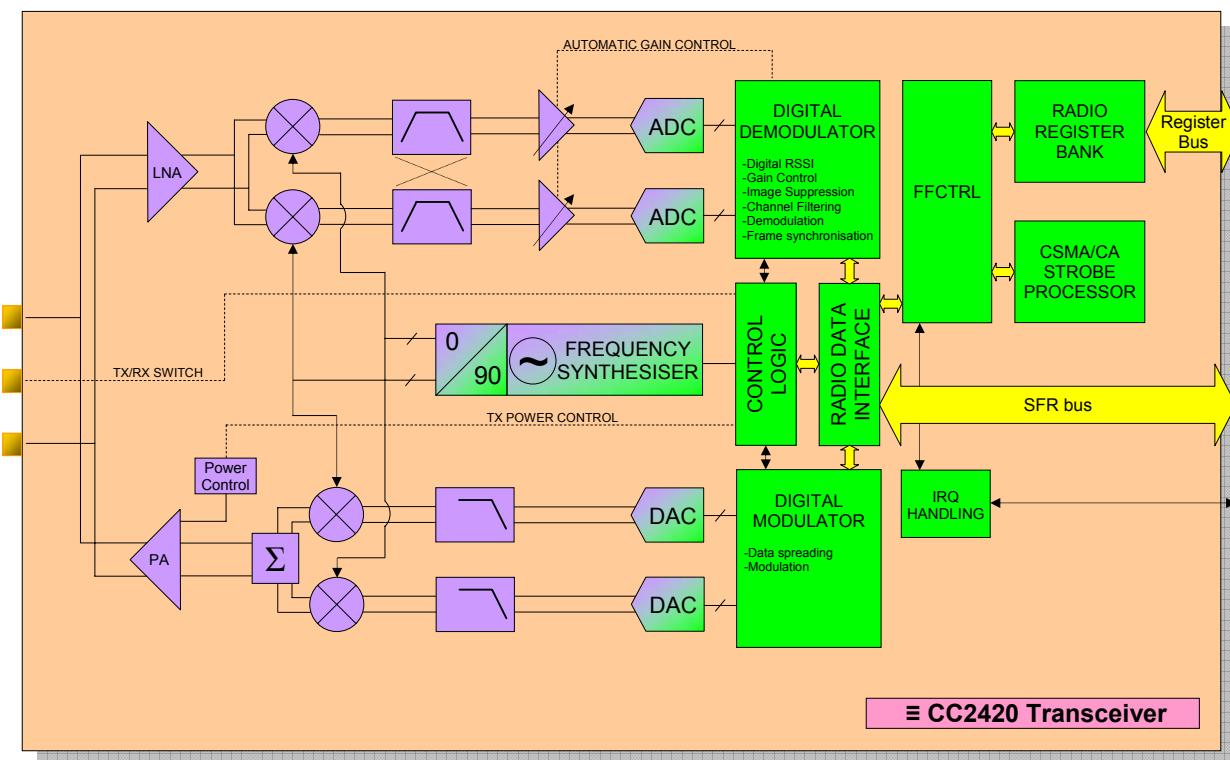
See Reference [6] for implementing the 1-wire interface in software.

Radio Section

The radio core is based on the industry standard Chipcon/TI CC2420 transceiver. The IEEE 802.15.4 compliant radio is shown below in a simplified block diagram. Operation of the radio is configured through a set of RF registers and controlled through a set of command strobes (single byte instructions) which control the functionality of the radio. E.g. enable frequency synthesiser, enable receive mode, enable transmit mode etc. The RF registers also provide status information from the radio. All command strobes from the CPU to the radio pass through the CSMA/CA Strobe Processor

Refer to [1] for more detailed description of the radio operation.

Block Diagram



Receiver

The CC2430/31 SoC contains a low-IF receiver. The received RF signal is amplified by a low-noise amplifier (LNA) and down-converted in quadrature to the 2MHz intermediate frequency. The complex I/Q signal is then bandpass filtered and amplified with a variable gain amplifier. The gain of the amplifier is digitally controlled, and the AGC feedback loop ensures that the ADC operates inside its dynamic range. The signal is digitised by the ADCs. The AGC, final channel filtering, demodulation, de-spreading, symbol-correlation and byte synchronisation are performed digitally.

IRQ handling presents an interrupt when a start of frame delimiter has been detected. A 128 byte receive FIFO is provided to buffer the received data. The firmware may read the receive FIFO through the SFR interface, ideally by DMA transfer into CPU memory. The receive FIFO is provided with overflow detection, informing the CPU via interrupt.

The CRC is verified in hardware, and the RSSI and correlation values are appended to the received frame. The clear channel assessment, CCA, is available through an interrupt in receive mode. AES decryption (if adopted) is then handled by the CPU and AES coprocessor independent from the radio.



Transmitter

The CC2430/31 SoC transmitter is based on direct up-conversion. AES encryption (if adopted) is applied prior to transferring the data to the 128 byte transmit FIFO buffer. Preamble and start of frame delimiters are generated in hardware. The IEEE 802.15.4 direct sequence spread spectrum modulation format is then applied by taking each byte and slitting it into two symbols (4-bits each). The least significant symbol is transmitted first and for multi-byte fields, the least significant byte is transmitted first. Each symbol is mapped to one-of-sixteen pseudo-random sequences of 32 “chips” each. The chip sequence is then transmitted at 2MChip/s with the least significant chip first for each symbol. The modulation format is Offset – Quadrature Phase Shift Keying (O-QPSK), with half-sine chip shaping. This is equivalent to Minimum Shift Keying (MSK), whereby each “chip” is transmitted as a half sine alternatively between the I and Q channels with one half period offset. The result for the I and Q channels are then output to the DACs, and then via low pass filtering to the up-conversion mixers.

The resulting RF signal is then amplified in the programmable power amplifier (PA), and fed to the antenna via the differential connection. Output power is programmed through the TXCTRLL Register. The maximum power attainable is 0.6dBm. Internal TX/RX switching simplifies the antenna interface matching. The biasing of the PA and LNA is done by connecting the TX/RX switch to the two differential RF connections through a DC path. The signal then pass through a discrete microstrip balun to either the board mounted chip antenna, or SMA / RP-SMA RF connector.

Frequency Synthesiser

Frequency synthesis is provided by a completely integrated VCO and 90° phase splitter for the I and Q local oscillator (LO) signals to the up/down conversion mixers. The VCO operates in the frequency range 4800 – 4967 MHz, divided by two for the I and Q signals (2400 – 2483.5MHz). The VCO characteristics will change with temperature and/or voltage supply and the desired operating frequency. To compensate for this the PLL self-calibrates (bias current and tuning range) every time the RX mode or TX mode are enabled.

The on-chip voltage regulator delivers the regulated 1.8 V supply voltage for the radio circuitry.



Specifications

DC Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
Supply Inputs					
Operating Supply Voltage V_{DD}	2.0	3.3	3.6	V	SoC power supply (Header Pin 22) referenced to signal/RF ground plane (0V).
External Supply V_{unreg}	4.0	---	30.0	V	Header Pin 19 – Isolated Regulator output 3.3V - Pin 21 requires linking to Pin 22 to power SoC. Isolated section therefore draws no leakage current when operating module from Pin 22 only (E.g. battery). Minimum input voltage to guarantee 3.3V output.
Isolated Regulator Output Voltage	3.234	3.3	3.366	V	Header Pin 21 – referenced to 0V.
Isolated Regulator Output Current		50	100**	mA	Nominally 50mA continuous (4-30V input), ** 100mA peak for short periods, dependent on input voltage. Regulator has current and thermal limiting.
Isolated Regulator Drop-out voltage		380	450	mV	Full load 100mA output.
Isolated Regulator quiescent current		75		µA	Up to 8mA typical on full 100mA load.
SoC Current Consumption – CC2430 & CC2431					
MCU Active Mode, 32 MHz, low MCU activity		9.5		mA	32 MHz XOSC running. No radio or peripherals active. Low MCU activity : no flash access (i.e. only cache hit), no RAM access.
MCU Active Mode, 32 MHz, medium MCU activity		10.5		mA	32 MHz XOSC running. No radio or peripherals active. Medium MCU activity: normal flash access1, minor RAM access.
MCU Active Mode, 32 MHz, high MCU activity		12.3		mA	32 MHz XOSC running. No radio or peripherals active. High MCU activity: normal flash access1, extensive RAM access and heavy CPU load.
MCU Active and RX Mode		26.7		mA	MCU running at full speed (32MHz), 32MHz XOSC running, radio in RX mode, -50 dBm input power. No peripherals active. Low MCU activity.
MCU Active and TX Mode, 0dBm		26.9		mA	MCU running at full speed (32MHz), 32MHz XOSC running, radio in TX mode, 0dBm output power. No peripherals active. Low MCU activity.
Power mode 1 (PM1)		190		µA	Digital regulator on, 16 MHz RCOSC and 32 MHz crystal oscillator off. 32.768 kHz XOSC, POR and ST active. RAM retention.
Power mode 2 (PM2)		0.5		µA	Digital regulator off, 16 MHz RCOSC and 32 MHz crystal oscillator off. 32.768 kHz XOSC, POR and ST active. RAM retention.
Power mode 3 (PM3)		0.3		µA	No clocks. RAM retention. POR active.



Parameter	Min	Typ	Max	Unit	Condition/Note
MAC address Chip Current Consumption (Active for initial read only on power up / reset)					
Active Power		5		µA	Powered via data pin of SoC, power, control address and data all via a single pin.
Standby Power		0		µA	No serial chip communication.
IO Parameters					
General purpose Input programmable pull-up / pull-down		20		kΩ	P1_0 (Header Pin 12) and P1_1 (Header Pin 9) do not have this feature. All are configurable for external interrupt.
General purpose output drive current sink / source		±4		mA	P1_0 (Header Pin 12) and P1_1 (Header Pin 9) have ±20mA drive capability.
ADC Resolution	7		12	bit	Programmable conversion resolution / decimation rate.
Analogue Input Resistance		197		kΩ	Simulated using conversion 4MHz clock speed.
Internal reference		1.25		V	External reference can be selected on AIN7 / P0_7 (Header Pin 2) or AIN6-AIN7 for differential input conversion.
Input Voltage including External reference AIN6/AIN7			V _{DD}	V	
Conversion Time		20		µs	7-bit setting (64 decimation rate).
		36		µs	9-bit setting (128 decimation rate).
		68		µs	10-bit setting (256 decimation rate).
		132		µs	12-bit setting (512 decimation rate).
ADC Current Consumption		1.2		mA	
Temperature Sensor Temp. Coefficient		2.45		mV/°C	Fitted from -20 °C to +80 °C.
Temp. Sensor Accuracy	-2	0	2	°C	Over range -20 °C to +80 °C when using 2.45mV/°C after 1-point calibration at room temperature.
Temp. Sensor Current Consumption		280		µA	When enabled.
Battery Monitor		V _{DD} /3		V	Additional analogue input channel which measures the Analogue V _{DD} divided by 3 for use as a battery monitor.
UART Mode maximum Baud Rate			230,400	bps	For system clock set to 32MHz.
SPI Maximum Clock Rate			4	MHz	For system clock set to 32MHz.
Timer Input Capture	31.25			ns	With Sysclk = 32MHz.
Watchdog Timer		1.9		ms	Clock source 32.768kHz (count = 64)
		15.625		ms	Clock source 32.768kHz (count = 512)
		0.25		s	Clock source 32.768kHz (count = 8192)
		1		s	Clock source 32.768kHz (count = 32768)

**Memory**

Parameter	Min	Typ	Max	Unit	Condition/Note
FLASH Memory		128		kbyte	64 pages of 2kbyte each
Page erase time		20		ms	
Chip mass erase time		200		ms	
Write time		20		µs	Per 4 bytes
Data Retention		100		years	At room temperature
Program erase/write	1000			cycles	endurance
SRAM		4096		bytes	Data retention in all power modes
SRAM		4096		bytes	Data retention in power modes 0 (active) and 1.
MAC / Serial Chip		64		bit	ROM accessed through 1-wire interface

RF Frequency, Output Power Levels and Data Rates

Parameter	Min	Typ	Max	Unit	Condition/Note
RF Frequency Range	2400		2483.5	MHz	Programmable in 1 MHz steps, 5 MHz between channels for compliance with [1].
No. of channels		16			** – See RF channel table.
Channel Spacing		5		Mhz	**
Radio bit rate		250		kbps	**
Radio Chip Rate		2.0		MChip/s	**
Receiver Sensitivity		-92		dBm	PER = 1%, as specified by [1].
Nominal Output power		0		dBm	Delivered to a single ended 50 Ω load through a balun and output power control set to 0x5F (TXCTRLL register).
Programmable output power range		26		dBm	The output power is programmable in 16 steps from typically -25.2 to +0.6 dBm.
Antenna nominal RX / TX impedance		50		Ω	

The RF channels and associated frequencies defined by the IEEE 802.15.4 standard are as follows:

RF Channel	Frequency	RF Channel	Frequency	RF Channel	Frequency
11	2405 MHz	17	2435 MHz	23	2465 MHz
12	2410 MHz	18	2440 MHz	24	2470 MHz
13	2415 MHz	19	2445 MHz	25	2475 MHz
14	2420 MHz	20	2450 MHz	26	2480 MHz
15	2425 MHz	21	2455 MHz		
16	2430 MHz	22	2460 MHz		

[1] IEEE std. 802.15.4 - 2003: Wireless Medium Access Control (MAC) and Physical Layer (PHY) specifications for Low Rate Wireless Personal Area Networks (LR-WPANs).



Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit	Condition/Note
Supply Voltage V_{DD}	-0.3		3.9	V	Header Pin 22 – referenced to 0V.
Supply Voltage V_{unreg}				V	Header Pin 19 – referenced to 0V.
Voltage on any digital IO pin	-0.3		$V_{DD}+0.3$ max 3.9	V	
Input RF Level			10	dBm	
Storage temp	-50		+150	°C	Device not programmed.



Caution!! ZB100 Modules are ESD sensitive devices.
Precautions should be taken when handling the device in order to prevent permanent damage.

Physical Dimension and Environmental Conditions

All modules are RoHS Compliant in construction.

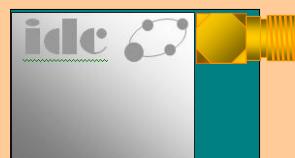
Parameter	Value	Notes / Module Codes
Size – board profile	21.6 x 35 mm	Excludes over-hang of SMA or RP-SMA RF connectors. See dimensional drawings for RF connector positions and board overhang etc.
Module height	3.5 mm	Board and RF shield combined - excluding pin headers.
Total height above OEM daughter board (See Dimensional drawings)	4.8 mm	ZB100-0-A; ZB100-1-A
	12.3 mm	ZB100-0-B; ZB100-0-D; ZB100-1-B; ZB100-1-D
	16.3 mm	ZB100-0-C; ZB100-0-E; ZB100-1-C; ZB100-1-E
	12.3 mm	ZB100-0-F-z; ZB100-0-H-z; ZB100-1-F-z; ZB100-1-H-z
	12.3 mm	ZB100-0-G-z; ZB100-0-J-z; ZB100-1-G-z; ZB100-1-J-z
Weight (approx.)	6 g	ZB100-0-A; ZB100-1-A
	8 g	ZB100-0-B; ZB100-0-D; ZB100-1-B; ZB100-1-D
	10 g	ZB100-0-C; ZB100-0-E; ZB100-1-C; ZB100-1-E
	8 g	ZB100-0-F-z; ZB100-0-H-z; ZB100-1-F-z; ZB100-1-H-z
	10 g	ZB100-0-G-z; ZB100-0-J-z; ZB100-1-G-z; ZB100-1-J-z
Operating Temperature	-20°C to +70°C	-40°C to +85°C Storage and Operational with minor degradation of clock stability / accuracy.
Operating Relative Humidity	80% RH	

For in-depth specifications please refer to the Related Documents - [1].

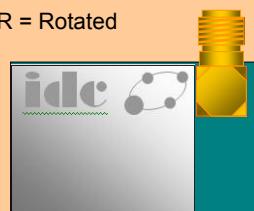
Module Coding**ZB100-x-y-z****(x) = System-on-Chip**0 = CC2430
1 = CC2431 (c/w location engine)**(y) = Antenna Style**A = Chip Antenna
B = Vertical SMA Jack
C = Vertical SMA Bulkhead Jack
D = Vertical RP-SMA Jack
E = Vertical RP-SMA Bulkhead Jack
F = R/A SMA Jack
G = R/A SMA Bulkhead Jack
H = R/A RP-SMA Jack
J = R/A RP-SMA Bulkhead Jack

R/A = Right-angled
RP-SMA = Reverse Polarity SMA**(z) = R/A RF Connector Orientation**

S = Straight

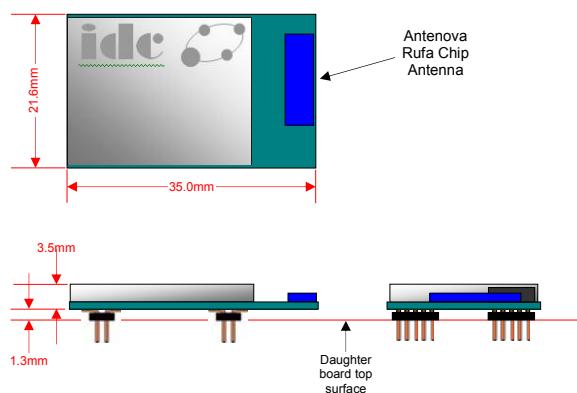


R = Rotated

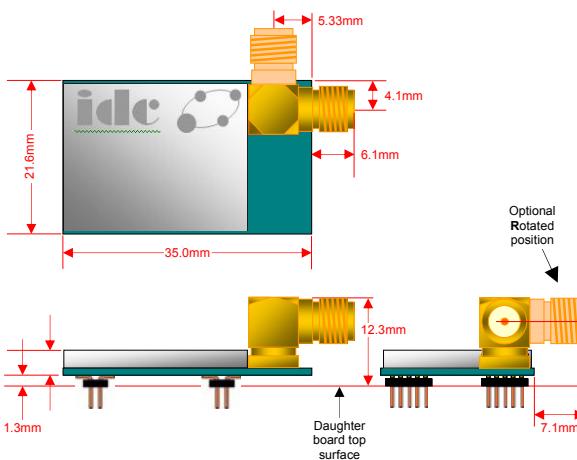
**Examples**ZB100-0-A
CC2430 with Chip AntennaZB100-1-B
CC2431 with vertical SMA JackZB100-0-J-R
CC2430 with R/A RP-SMA bulkhead
mounted in the rotated position

Module Dimensional Detail

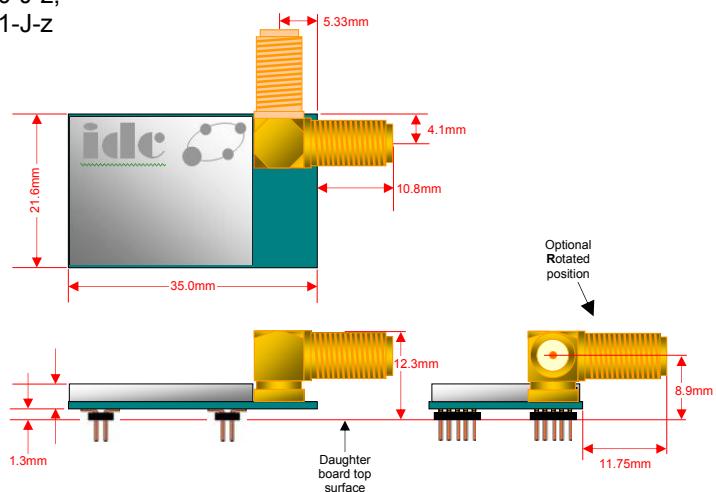
Chip Antenna Versions
ZB100-0-A, ZB100-1-A



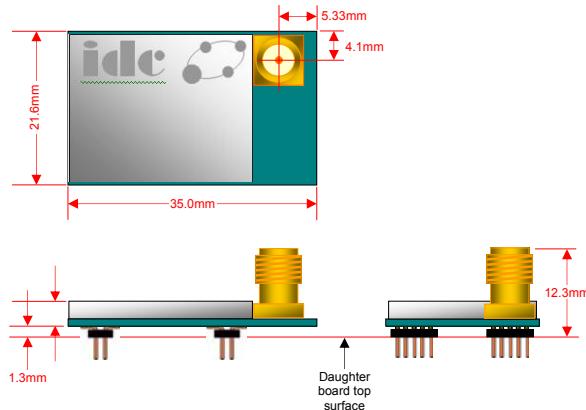
R/A SMA and RP-SMA Versions
ZB100-0-F-z; ZB100-0-H-z;
ZB100-1-F-z; ZB100-1-H-z



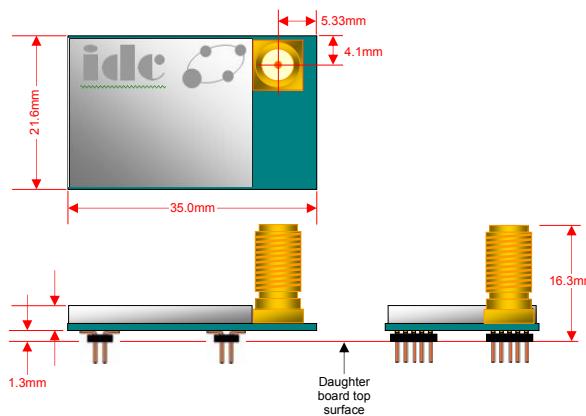
R/A SMA and RP-SMA Bulkhead Versions
ZB100-0-G-z; ZB100-0-J-z;
ZB100-1-G-z; ZB100-1-J-z



Vertical SMA and RP-SMA Versions
ZB100-0-B; ZB100-0-D; ZB100-1-B; ZB100-1-D



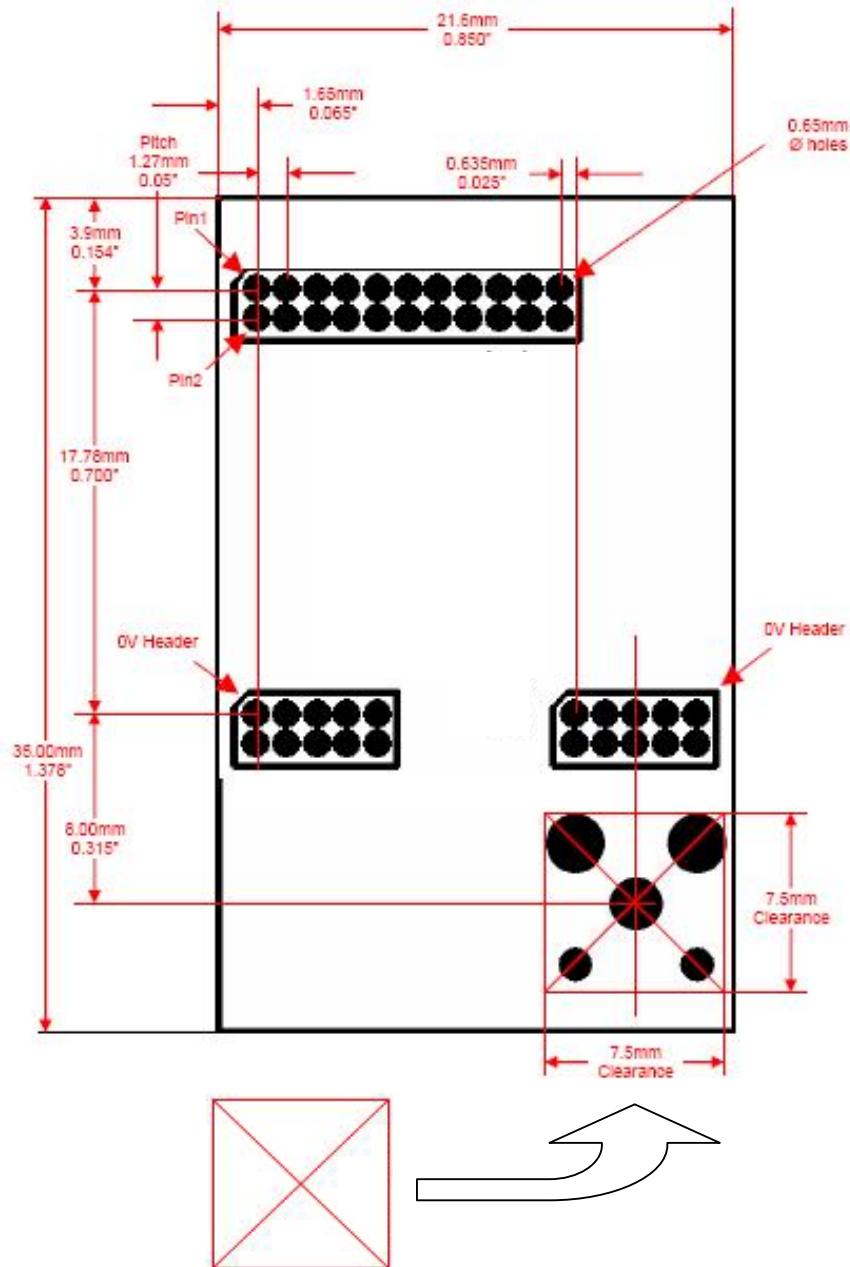
Vertical SMA and RP-SMA Bulkhead Versions
ZB100-0-C; ZB100-0-E; ZB100-1-C; ZB100-1-E



PCB Mounting Information

Daughter board PCB Layout and connector pads – top view:

22 way header (See table)
2 off 10 way headers for 0V grounding



The module requires a clearance hole on the daughter board. This area will need removing to allow for the SMA and RP-SMA RF connector legs and signal pin.

Not applicable if using the chip antenna



Pin Configuration

Connections of the 22-way header are as follows: 0V/Signal ground is provided by the two 10-way headers.

Pin #	Pin Ref.	Use	Description
1	P0_6	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4mA$ drive strength in output mode
		ADC - AIN6	Analogue Input 6 – single ended (Differential with AIN7) 8 – 12 bit resolution
2	P0_7	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source $\pm 4mA$ drive strength in output mode
		ADC – AIN7	Analogue Input 7 – single ended (Differential with AIN6) 8 – 12 bit resolution
3	P0_4	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4mA$ drive strength in output mode
		ADC – AIN4	Analogue Input 4 – single ended (Differential with AIN5) 8 – 12 bit resolution
		USART0 / SPI (SSN)	SPI0-SSN Data – Slave Select (Input)
		USART0 / UART (CTS)	UART0 – Clear-to-Send (Input)
		USART1 / SPI (MOSI)	SPI1-MISO – Data - Master Input / Slave Output
		USART1 / UART (TxD)	UART1 – Transmit Data (Output)
		TIMER1 (CC2)	TIMER1 – Channel 2 - Capture (Input) / Compare (Output)
4	P0_5	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4mA$ drive strength in output mode
		ADC – AIN5	Analogue Input 5 – single ended (Differential with AIN4) 8 – 12 bit resolution
		USART0 / SPI (SCK)	SPI0-SCK – Clock (Output)
		USART0 / UART (RTS)	UART0 – Ready-to-Send (Output)
		USART1 / SPI (MISO)	SPI1-MISO – Data - Master Input / Slave Output
		USART1 / UART (RxD)	UART1 – Receive Data (Input)
5	P0_2	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4mA$ drive strength in output mode
		ADC – AIN2	Analogue Input 2 – single ended (Differential with AIN3) 8 – 12 bit resolution
		USART0 / SPI (MISO)	SPI0-MISO – Data - Master Input / Slave Output
		USART0 / UART (RxD)	UART0 – Receive Data (Input)
		USART1 / SPI (SSN)	SPI1-SSN – Slave Select (Input)
		USART1 / UART (CTS)	UART1 – Clear-to-Send (Input)
		TIMER1 (CC0)	TIMER1 – Channel 0 - Capture (Input) / Compare (Output)



Pin #	Pin Ref.	Use	Description
6	P0_3	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4\text{mA}$ drive strength in output mode
		ADC – AIN3	Analogue Input 3 – single ended (Differential with AIN2) 8 – 12 bit resolution
		USART0 / SPI (MOSI)	SPI0-MOSI – Data - Master Output / Slave Input
		USART0 / UART (TxD)	UART0 – Transmit Data (Output)
		USART1 / SPI (SCK)	SPI1-SCK – Clock (Output)
		USART1 / UART (RTS)	UART1 – Ready-to-Send (Output)
		TIMER1 (CC1)	TIMER1 – Channel 1 - Capture (Input) / Compare (Output)
7	P0_0	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4\text{mA}$ drive strength in output mode
		ADC – AIN0	Analogue Input 0 – single ended (Differential with AIN1) 8 – 12 bit resolution
8	P0_1	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4\text{mA}$ drive strength in output mode
		ADC – AIN1	Analogue Input 1 – single ended (Differential with AIN0) 8 – 12 bit resolution
9	P1_1	GPIO	NO configurable Pull Up / Pull Down in Input Mode, interrupt source, $\pm 20\text{mA}$ drive strength in output mode
		TIMER1 (CC1) (Alt2)	TIMER1 – Channel 1 - Capture (Input) / Compare (Output) – Alternative Pin
		TIMER4 (CC1)	TIMER4 – Channel 1 - Capture (Input) / Compare (Output)
10	RESETn	SoC RESET	Used as SoC reset, or in conjunction with the two Debug pins DD and DC in order to enter the debug / programming mode
11	P1_3	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4\text{mA}$ drive strength in output mode
		USART0 / SPI (SCK) (Alt2)	SPI0-SCK – Clock (Output) – Alternative Pin
		USART0 / UART (RTS) (Alt2)	UART0 – Ready-to-Send (Output) – Alternative Pin
		TIMER3 (CC0)	TIMER3 – Channel 0 - Capture (Input) / Compare (Output)
12	P1_0	GPIO	NO configurable Pull Up / Pull Down in Input Mode, interrupt source, $\pm 20\text{mA}$ drive strength in output mode
		TIMER1 (CC2) (Alt2)	TIMER1 – Channel 2 - Capture (Input) / Compare (Output) – Alternative Pin
		TIMER4 (CC0)	TIMER4 – Channel 0 - Capture (Input) / Compare (Output)
13	P1_5	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4\text{mA}$ drive strength in output mode
		USART0 / SPI (MOSI) (Alt2)	SPI0-MOSI – Data - Master Output / Slave Input – Alternative Pin
		USART0 / UART (TxD) (Alt2)	UART0 – Transmit Data (Output) – Alternative Pin
		USART1 / SPI (SCK) (Alt2)	SPI1-SCK – Clock (Output) – Alternative Pin
		USART1 / UART (RTS) (Alt2)	UART1 – Ready-to-Send (Output) – Alternative Pin



Pin #	Pin Ref.	Use	Description
14	P1_2	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4\text{mA}$ drive strength in output mode
		USART0 / SPI (SSN) (Alt2)	SPI0-SSN Data – Slave Select (Input) – Alternative Pin
		USART0 / UART (CTS) (Alt2)	UART0 – Clear-to-Send (Input) – Alternative Pin
		TIMER1 (CC0) (Alt2)	TIMER1 – Channel 0 - Capture (Input) / Compare (Output) – Alternative Pin
15	P1_7	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4\text{mA}$ drive strength in output mode
		USART1 / SPI (MISO) (Alt2)	SPI1-MISO – Data - Master Input / Slave Output – Alternative Pin
		USART1 / UART (RxD) (Alt2)	UART1 – Receive Data (Input) – Alternative Pin
		TIMER3 (CC1) (Alt2)	TIMER3 – Channel 1 - Capture (Input) / Compare (Output) – Alternative Pin
16	P1_4	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4\text{mA}$ drive strength in output mode
		USART0 / SPI (MISO) (Alt2)	SPI0-MISO – Data - Master Input / Slave Output – Alternative Pin
		USART0 / UART (RxD) (Alt2)	UART0 – Receive Data (Input) – Alternative Pin
		USART1 / SPI (SSN) (Alt2)	SPI1-SSN – Slave Select (Input) – Alternative Pin
		USART1 / UART (CTS) (Alt2)	UART1 – Clear-to-Send (Input) – Alternative Pin
		TIMER3 (CC1)	TIMER3 – Channel 1 - Capture (Input) / Compare (Output)
17	P2_2	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4\text{mA}$ drive strength in output mode
		DC	Debug Clock – used in conjunction with RESETn and DD
18	P1_6	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4\text{mA}$ drive strength in output mode
		USART1 / SPI (MOSI) (Alt2)	SPI1-MOSI – Data – Master Output / Slave Input – Alternative Pin
		USART1 / UART (TxD) (Alt2)	UART1 – Transmit Data (Output) – Alternative Pin
		TIMER3 (CC0) (Alt2)	TIMER3 – Channel 0 - Capture (Input) / Compare (Output) – Alternative Pin
19	Vunreg	Reg. Input	On-board regulator (4 to 30V). The regulator can provide 100mA max.
20	P2_1	GPIO	Configurable Pull Up / Pull Down in Input mode, interrupt source, $\pm 4\text{mA}$ drive strength in output mode
		DD	Debug Data – used in conjunction with RESETn and DC
21	Vreg	Reg. Output	Vout from the Regulator Section. Link to Pin 22 when powering the SoC using the on-board regulator.
22	3.3V	SoC V_{DD}	SoC Supply Voltage (2.0 to 3.6V) – 3V battery powered connection point.

NOTE: Refer to CC2430.pdf and/or CC2431.pdf Datasheets from the Texas Instruments Website for in-depth detail for configuring and programming the SoC device.



Agency Certifications

EUROPEAN UNION (ETSI)



The ZB100 Module has been certified for use in European Union countries.

If the ZB100 Modules are incorporated into a product, the manufacturer must ensure compliance of the final product to the European harmonised EMC and low-voltage/safety standards. A Declaration of Conformity must be issued for each of these standards and kept on file as described in Annex II of the R&TTE Directive.

Furthermore, the manufacturer must maintain a copy of the ZB100 Modules documentation and ensure the final product does not exceed the specified power ratings, antenna specifications, and/or installation requirements as specified in the user manual. If any of these specifications are exceeded in the final product, a submission must be made to a notified body for compliance testing to all required standards.

IMPORTANT: The 'CE' mark must be affixed to a visible location on the OEM product. The 'CE' mark shall consist of the initials 'CE' taking the form shown above.

- If the CE marking is reduced or enlarged, the proportions given in the above example must be respected.
- The CE marking must have a height of at least 5mm except where this is not possible on account of the nature of the apparatus.
- The CE marking must be affixed visibly, legibly, and indelibly.

UNITED STATES (FCC)



This equipment complies with Part 15 of the FCC rules and regulations.

To fulfill the FCC Certification requirements, an OEM manufacturer must comply with the following regulations:

1. The modular transmitter must be labelled with its own FCC ID number, and, if the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following:

Example of Label required for OEM products containing the following Model codes:

ZB100-x-A Chip Antenna

ZB100-x-D RF connector – Vertical RP-SMA

ZB100-x-E RF connector – Vertical RP-SMA bulkhead

ZB100-x-H-y RF connector – Right-angled RP-SMA

ZB100-x-J-y RF connectot – Right-angled RP-SMA bulkhead

Note: x refers to the System-on-Chip variant – either CC2430 or CC2431.

y refers to mountng position for right angled connectors – See Model Coding Section.

Contains FCC ID: VO7ZB100

The enclosed device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (i) this device may not cause harmful interference and (ii) this device must accept any interference received, including interference that may cause undesired operation.

Any similar wording that expresses the same meaning may be used.



2. For RF Connector models, the external antennas have been tested and approved specified below. The ZB100 (D, E, H or J) models may be integrated with other types or custom designed antennas which the OEM installer must authorize following the FCC 15.21 requirements.

WARNING: The Original Equipment Manufacturer (OEM) must ensure that the OEM modular transmitter must be labeled with its own FCC ID number. This includes a clearly visible label on the outside of the final product enclosure that displays the contents shown below. If the FCC ID is not visible when the equipment is installed inside another device, then the outside of the device into which the equipment is installed must also display a label referring to the enclosed equipment.

IMPORTANT: This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (i) this device may not cause harmful interference and (ii) this device must accept any interference received, including interference that may cause undesired operation (FCC 15.19)

The internal / external antenna(s) used for this mobile transmitter must provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

IMPORTANT: Modifications not expressly approved by this company could void the user's authority to operate this equipment (FCC section 15.21)

IMPORTANT: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in residential areas is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense (FCC section 15.105).

Approved Antenna List

Part Number	Manufacturer / Description	Gain, dBi	ETSI	FCC
3030A5839-01	Antenova Rufa chip antenna (Left-hand), frequency range 2400 – 2500MHz	2.1dBi Peak	✓	✓
2010B4844-01 (SMA)	Antenova Titanis, swivel antenna (1/2 wave), frequency range 2400 – 2500MHz	2.2dBi Peak	✓	✗
2010B6090-01 (RP-SMA)			✓	✓
NET-WL-ANT009OSC	Solwise omni-directional dipole with RP-SMA connector, frequency range 2400 – 2500MHz See Notes **	8.5±0.5dBi	✓	✓

NOTES:

All testing has been carried out with the CC2430 / CC2431 programmed for maximum RF output power of 0.6 dBm (Register TXCTRLL = 0xFF).

Any omni-directional dipole (articulated or straight) may be used providing the gain is less than that tested using the **NET-WL-ANT009OSC (9dBi)**

** Channel 26 - restriction for use under FCC Part 15 Rules.

The output power for channel 26 (2480MHz) is restricted as follows:

1. Use an omni-directional dipole antenna with gain no greater than 3 dBi.
2. Reduce the radio power accordingly within the software. E.g. for the 9dBi antenna, the power outputs needs reducing by ≥ 6 dB from maximum.



Glossary

ADC	Analogue to Digital Converter	IEEE	Institute of Electrical and Electronic Engineers
AES	Advanced Encryption Standard	IF	Intermediate Frequency
AIN#	Analogue Input Channel #number	IRQ	Interrupt Request
bps	Bits per Second	ISM	Industrial, Scientific and Medical frequency band - a part of the radio spectrum that can be used by anybody without a license in most countries
CBC	Cipher Block Chaining	IV	Initialisation Vector (AES)
CBC-MAC	Cipher Block Chaining Message Authentication Code	kByte	1024 bytes
CC#	Capture Compare #number	LC	Inductor-Capacitor
CCA	Clear Channel Assessment, Radio	LNA	Low Noise Amplifier
CCM	Counter Mode + CBC-MAC	LR-WPAN	Low Rate Wireless Personal Area Network
CD	Carrier Detect	LSB	Least Significant Bit
CE	European marking to indicate conformity	MAC	Medium Access Control layer
CFB	Cipher Feedback	MCU	Microcontroller Unit - For the ZB100, this refers to the 8051 core processor in either the CC2430 or CC2431
CPU	Central Processing Unit	MISO	Master In / Slave Out, SPI Interface
CSMA/CA	Carrier Sense Multiple Access with Collision Avoidance	MOSI	Master Out / Slave In, SPI Interface
CTR	Counter Mode (encryption)	MSB	Most Significant Bit
CTS	Clear to Send, UART Interface	MSK	Minimum Shift Keying
DC₍₁₎	Direct Current	NONCE	Not Once (AES)
DC₍₂₎	Debug Clock	OEM	Original Equipment Manufacturer
DD	Debug Data	OFB	Output Feedback (encryption)
DMA	Direct Memory Access	O-QPSK	Offset-Quadrature Phase Shift Keying
DSR	Data Set Ready	OTA	Over-the-Air – upgrade/programming
DSSS	Direct Sequence Spread Spectrum	OUI	Organisational Unique Identifier (24-bit)
DTR	Data Terminal Ready	PA	Power Amplifier
ECB	Electronic Codebook (encryption)	PC	Personal Computer
ESD	Electro Static Discharge	PCB	Printed Circuit Board
ETSI	European Telecommunications Standards Institute	PER	Packet Error Rate
EUI	Extended Unique Identifier	PHY	Physical Layer
FCC	Federal Communications Commission	PLL	Phase Locked Loop
FFCTRL	FIFO and Frame Control	POR	Power on Reset
FFD	Full-Function Device	PWM	Pulse Width Modulator
FIFO	First In First Out	R&TTE	Radio and Telecommunications Terminal Equipment
FIFOP	FIFO receive buffer overflowed threshold, Radio Interface	RAM	Random Access Memory
FLASH	Non-volatile memory which can be electrically erased and re-programmed		
GPIO	General Purpose Input/Output		
HW	Hardware		



R/A	Right Angled	SPI	Serial Peripheral Interface bus
RC	Resistor / Capacitor	SRAM	Static Random Access Memory
RCOSC	RC Oscillator	SSN	Slave Select Number, SPI Interface
RF	Radio Frequency	ST	Sleep Timer
RP-SMA	Reverse Polarity Sub-miniature Version A – coaxial RF connector with reversed gender (Required for FCC compliance)	SW	Software
RSSI	Received Signal Strength Indicator	TI	Texas Instruments
RTS	Ready to Send, UART Interface	TxD	Transmit Data, UART Interface
ROM	Read only memory	TX	Transmit, Radio
RoHS	Restriction on Hazardous Substances	UART	Universal Asynchronous Receiver/Transmitter
RTC	Real Time Clock	UID	Unique Identifier
RxD	Receive Data, UART Interface	USART	Universal Synchronous/Asynchronous Receiver/Transmitter
SCK	Serial Clock, SPI Interface	VCO	Voltage Controlled Oscillator
SFR	Special Function Register	XOSC	Crystal Oscillator
SMA	Sub-miniature Version A – coaxial RF connector	802.15.4	The IEEE 802.15.4-2003 standard applicable to low-rate wireless Personal Area Networks
SoC	System-on-Chip		



Related Documents

- [1] Chipcon Products from Texas Instruments CC2430 – A True System-on-Chip solution for 2.4GHz IEEE 802.15.4 / ZigBee CC2430 Data Sheet (Rev. 2.1) SWRS036F
- [2] Chipcon Products from Texas Instruments CC2431 – System-on-Chip for 2.4 GHz ZigBee®/IEEE 802.15.4 with Location Engine CC2431 Data Sheet (Rev. 2.01) SWRS034B
- [3] Chipcon Products from Texas Instruments – Application Note AN042 – CC2431 Location Engine Application Note AN042 (Rev. 1.0) SWRA095
- [4] Design Note DN108 – Using AES Encryption in CC111xFx, CC243x, and CC251xFx SWRA172A
- [5] CC1110DK/ CC2430DK/CC2510DK Development Kit - User Manual - Rev. 1.5 SWRU039
- [6] Dallas/Maxim – 1-wire Communication Through Software – App Note 126

Disclaimer

Intelligent Distributed Controls Limited believes that at the time of issue, all information contained herein to be accurate. Intelligent Distributed Controls Limited reserves the right to make changes to this product or documentation without prior notice. Latest available revisions shall be provided on the Website.

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