A6650

Hardware Design

Smart Module Series

Version: 1.0

Date: 2022-04-22

Status: Released

1 Introduction

This document, describing A6650 and its air and hardware interfaces connected to your applications, informs you of the interface specifications, electrical and mechanical details, as well as other related information of the module.

With the application notes and user guides provided separately, you can easily use the module to design and set up mobile applications.

FCC Certification Requirements.
According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.
And the following conditions must be met:
1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3. A label with the following statements must be attached to the host end product: This device contains FCC ID: V5PA6650
4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	FCC Max Antenna Gain (dBi)	IC Max Antenna Gain（dBi）
LTE BAND 2	8.00	10.33
LTE BAND 4	5.00	9.54
LTE BAND 5	9.41	9.67
LTE BAND 7	8.00	11.22
LTE BAND 12	7.62	9.36
LTE BAND 13	7.62	9.87
LTE BAND 14	7.62	9.63
LTE BAND 17	7.62	9.39
LTE BAND 25	8.00	9.74
LTE BAND 26(814-824)	9.35	NA
LTE BAND 26(824-849)	9.41	9.56

LTE BAND 41	8.00	11.16
LTE BAND 66	5.00	10.04
LTE BAND 71	7.62	9.12
BT	NA	NA
WIFI		

5. This module must not transmit simultaneously with any other antenna or transmitter

6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products.

Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: V5PA6650" or "Contains FCC ID: V5PA6650" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring

that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement

IRSS-GEN

"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Déclaration sur l'exposition aux rayonnements RF

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

The host product shall be properly labeled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows:

"Contains IC: 11689A-A6650 "

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.

L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:

"Contient IC:11689A-A6650 " ou "où: 11689A-A6650 est le numéro de certification du module".

2 Product Overview

2.1. Frequency Bands and Functions

A6650E is of Smart LTE modules based on Android operating system, and provides industrial grade performance. Its general features are listed below:

- Supports worldwide LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EV-DO/CDMA, EDGE and GPRS coverage.
- Supports short-range wireless communication via Wi-Fi 802.11a/b/g/n/ac and Bluetooth 5.0 [1].
- Integrates GPS/GLONASS/BDS/Galileo/QZSS/SBAS/NavIC satellite positioning systems.
- Supports multiple audio and video codecs.
- Built-in high performance Adreno™ 702 graphics processing unit.
- Provides multiple audio and video input/output interfaces as well as abundant GPIO interfaces.

Frequency Bands and GNSS Functions

Mode	Frequency Bands
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B66/B71
LTE-TDD	B41
Wi-Fi 802.11a/b/g/n/ac	2402–2482 MHz 5180–5825 MHz
Bluetooth 5.0	2402–2480 MHz
GNSS	GPS:

Key Features

Feature	Details
Application Processor	● 64-bit quad-core ARM Cortex-A53 microprocessor, up to 2.0 GHz ● 512 KB L2 cache
Modem DSP	● Hexagon DSP v66k core

	• 512 KB L2 cache
GPU	Adreno™ 702 GPU with 64-bit addressing, up to 845 MHz
Memory (Optional)	• 32 GB eMMC + 2 GB LPDDR4X • 32 GB eMMC + 3 GB LPDDR4X
Operating System	Android 12*
Power Supply	• Supply voltage: 3.5–4.4 V • Typical supply voltage: 3.8 V
Transmitting Power	• Class 4 (33 dBm ±2 dB) for GSM850 • Class 1 (30 dBm ±2 dB) for PCS1900 • Class E2 (27 dBm ±3 dB) for GSM850 8-PSK • Class E2 (26 dBm ±3 dB) for PCS1900 8-PSK • Class 3 (24 dBm +1/-3 dB) for WCDMA bands • Class 3 (23 dBm ±2 dB) for LTE-FDD bands • Class 3 (23 dBm ±2 dB) for LTE-TDD bands

LTE Features	• Supports 3GPP Rel-10 Cat 4
	• Supports 1.4/3/5/10/15/20 MHz RF bandwidth
	• Supports Multiuser MIMO in DL direction
	• Data rate (Max.):
	  − Cat 4 FDD: 150 Mbps (DL)/ 50 Mbps (UL)
	  − Cat 4 TDD: 130 Mbps (DL)/ 30 Mbps (UL)

UMTS Features	• Supports 3GPP Rel-9 DC-HSDPA, HSPA+, HSDPA. HSUPA and WCDMA
	• Supports QPSK, 16QAM and 64QAM modulations
	• Data rate (Max.):
	  − DC-HSDPA: 42 Mbps (DL)
	  − HSUPA: 5.76 Mbps (UL)
	  − WCDMA: 384 kbps (DL)/ 384 kbps (UL)

GSM Features	**R99** • CSD: 9.6 kbps, 14.4 kbps **GPRS** • Supports GPRS multi-slot class 33 (33 by default)

	• Coding scheme: CS-1, CS-2, CS-3 and CS-4 • Max. 107 kbps (DL), 85.6 kbps (UL) **EDGE** • Supports EDGE multi-slot class 33 (33 by default) • Supports GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) • Downlink coding schemes: MCS 1–9 • Uplink coding schemes: MCS 1–9 • Max. 296 kbps (DL), 236.8 kbps (UL)
WLAN Features	• 2.4 GHz, 802.11b/g/n, up to 150 Mbps • 5 GHz, 802.11a/n/ac, up to 433 Mbps • Supports AP mode and STA mode
Bluetooth Feature [2]	Bluetooth 5.0
GNSS Features [3]	• GPS/GLONASS/BDS/Galileo/QZSS/SBAS/NavIC, L1 + L5
SMS	• Text and PDU mode • Point-to-point MO and MT • SMS cell broadcast
LCM Interface	• Supports one group of 4-lane MIPI DSI • Supports up to HD+ (1680 × 720) @ 60 fps
Camera Interfaces	• Supports two groups of 4-lane MIPI CSI, up to 2.5 Gbps/lane • Supports two cameras (4-lane + 4-lane) or three cameras (4-lane + 2-lane + 1-lane) • Supports up to 25 MP or 13 MP + 13 MP with dual ISP
Video Codec	• Video encoding + decoding: 720P @ 30 fps + 1080P @ 30 fps • Encoding: up to 1080P @ 30 fps; Decoding: up to 1080P @ 30 fps
Audio Interfaces	**Audio inputs:** • Two differential microphone inputs • One single-ended microphone input **Audio outputs:** • Class AB stereo headphone output • Class AB earpiece differential output • Class AB line out differential output
Audio Codec	• EVS, EVRC, EVRC-B, EVRC-WB • G.711, G.729A, and G.729AB • GSM-FR, GSM-EFR, GSM-HR • AMR-NB, AMR-WB
USB Interface	**Type-C interface type:** • Complies with both USB 3.1 or 2.0 specifications, with transmission rating

	up to 5 Gbps on USB 3.1 and 480 Mbps on USB 2.0 ● Supports USB OTG ● Used for AT command communication, data transmission, software debugging, and firmware upgrade
UART Interfaces	Three UART interfaces: UART0, UART1, and UART4 (debug UART) ● UART0: four-wire UART interface supporting RTS and CTS hardware flow control ● UART1: two-wire UART interface ● UART4 (debug UART): two-wire UART interface used for debugging by default
SD Card Interface	● Supports SD 3.0 ● Supports SD card hot-plug
(U)SIM Interfaces	● Two (U)SIM interfaces ● Supports USIM/SIM cards: 1.8/2.95 V ● Supports Dual SIM Dual Standby (supported by default)
I2C Interfaces	● Four I2C interfaces ● Used for peripherals such as camera, sensor, touch panel, etc.
ADC Interface	One generic ADC interface, up to 15-bit resolution
Real Time Clock	Supported
Antenna Interfaces	Main antenna, Rx-diversity antenna, GNSS antenna and Wi-Fi/Bluetooth antenna interfaces
Physical Characteristics	● Size: (40.5 ±0.15) mm × (40.5 ±0.15) mm × (2.85 ±0.2) mm ● Package: LCC + LGA ● Weight: Approx. 10.3 g
Temperature Range	● Operating temperature range [4]: -35 °C to +75 °C ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	● USB interface ● OTA
RoHS	All hardware components are fully compliant with EU RoHS directive.

3 Application Interfaces

3.1. General Description

A6650 is a series of SMD type modules with 146 LCC pins and 128 LGA pins. The following interfaces and functions are described in detail in these subsequent chapters:

- Power supply
- VRTC
- Power output
- Charging interface
- USB interface
- UART interfaces
- (U)SIM interfaces
- SD card interface
- GPIO interfaces
- I2C interfaces
- ADC interface
- Motor drive interface
- LCM interface
- Flash interface
- Touch panel interface
- Camera interfaces
- Sensor interface
- Audio interfaces
- USB_BOOT Interface

3.2. Pin Assignment

The following figure shows the pin assignment of the module.

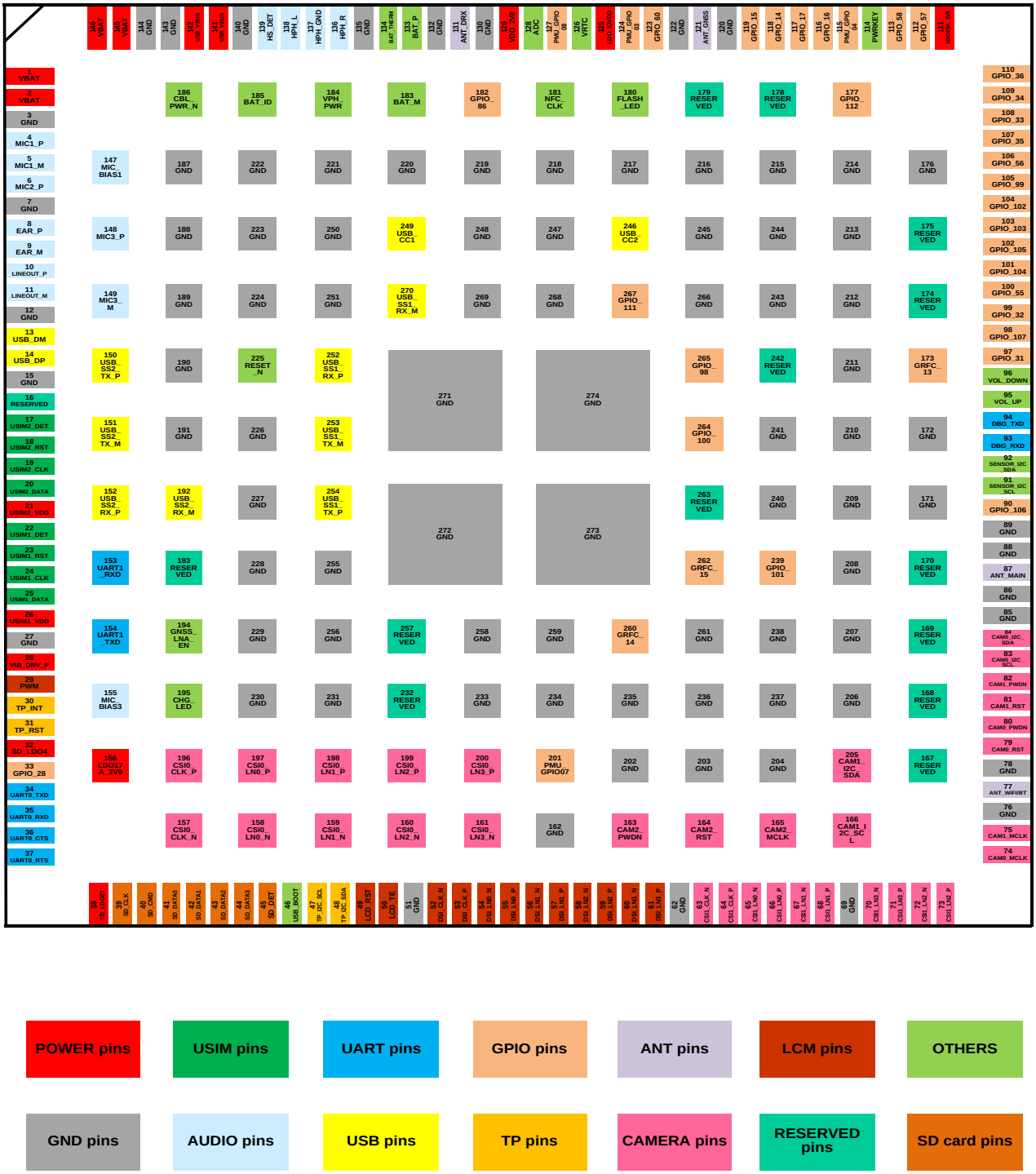


Figure 2: Pin Assignment (Top View)

3.3. Pin Description

I/O Parameter Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PIO	Power Input/Output

Table 7: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	1, 2, 145, 146	PIO	Power supply for the module	Vmin = 3.5 V Vnom = 3.8 V Vmax = 4.4 V	Provide sufficient current up to 3 A. It is suggested to use a TVS for surge protection.
VPH_PWR	184	PO	Power supply for peripherals	Vmin = 3.5 V Vnom = 3.8 V Vmax = 4.4 V	This pin is used to power peripheral devices. Maximum output current is 1 A.
LDO15A_1V8	111	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 200 mA	The power supply for LCM, sensor, cameras and I2C pull-up circuits.
LDO17A_3V0	156	PO	3.0 V output	Vnom = 3.0 V $I_O$max = 192 mA	The power supply for TP and sensor.

LDO_IOVDD	125	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 300 mA	The power is reserved for LCM and camera's IOVDD. This voltage is not adjustable.
VRTC	126	PIO	Power supply for RTC	Vomax = 3.2 V $V_I$min = 2.5 V $V_I$max = 3.2 V	If unused, keep it open.
VDD_2V8	129	PO	2.8 V output	Vnom = 2.8 V $I_O$max = 500 mA	The power supply for camera’s AVDD. This voltage is not adjustable.
Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_BIAS1	147	PO	Bias voltage 1 output for microphone	Vomin = 1.6 V Vomax = 2.85 V	The rated output current is 3 mA.
MIC1_P	4	AI	Microphone input for channel 1 (+)		
MIC1_M	5	AI	Microphone input for channel 1 (-)		
MIC2_P	6	AI	Microphone input for headset (+)		
MIC3_P	148	AI	Microphone input for channel 3 (+)		
MIC3_M	149	AI	Microphone input for channel 3 (-)		
MIC_BIAS3	155	PO	Bias voltage 3 output for microphone	Vnom = 1.8 V	The rated output current is 3 mA. The output voltage is fixed at 1.8 V and cannot be adjusted.
EAR_P	8	AO	Earpiece output (+)		
EAR_M	9	AO	Earpiece output (-)		
LINEOUT_P	10	AO	Audio line differential output (+)		The typical output voltage is 2 Vrms.
LINEOUT_M	11	AO	Audio line differential output (-)		
HPH_R	136	AO	Headphone right channel output		
HPH_GND	137	AO	Headphone reference ground		
HPH_L	138	AO	Headphone left channel output		
HS_DET	139	AI	Headset hot-plug detect		High level by default.

USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	141, 142	PIO	Charging power input. Power supply output for OTG device. USB/adaptor insertion detection	Vmax = 6.0 V Vmin = 4.0 V Vnom = 5.0 V	The maximum output current is 500 mA.
USB_DM	13	AIO	USB differential data (-)		90 Ω differential impedance. USB 2.0 standard compliant.
USB_DP	14	AIO	USB differential data (+)		
USB_SS1_RX_P	252	AI	USB 3.1 channel 1 superspeed receive (+)		90 Ω differential impedance. USB 3.1 standard compliant.
USB_SS1_RX_M	270	AI	USB 3.1 channel 1 superspeed receive (-)		
USB_SS1_TX_P	254	AO	USB 3.1 channel 1 superspeed transmit (+)		
USB_SS1_TX_M	253	AO	USB 3.1 channel 1 superspeed transmit (-)		
USB_SS2_RX_P	152	AI	USB 3.1 channel 2 superspeed receive (+)		
USB_SS2_RX_M	192	AI	USB 3.1 channel 2 superspeed receive (-)		
USB_SS2_TX_P	150	AO	USB 3.1 channel 2 superspeed transmit (+)		
USB_SS2_TX_M	151	AO	USB 3.1 channel 2 superspeed transmit (-)		
USB_CC1	249	AI	USB Type-C detect 1		
USB_CC2	246	AI	USB Type-C detect 2		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	26	PO	(U)SIM1 card power supply	$I_O$max = 67 mA **1.8 V (U)SIM:** Vmax = 1.85 V Vmin = 1.75 V **2.95 V (U)SIM:** Vmax = 3.1 V Vmin = 2.8 V	Either 1.8 V or 2.95 V (U)SIM card is supported.

USIM1_DATA	25	DIO	(U)SIM1 card data	V_{IL}max = 0.2 × USIM1_VDD V_{IH}min = 0.7 × USIM1_VDD V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM1_VDD	Cannot be multiplexed into a generic GPIO.
USIM1_CLK	24	DO	(U)SIM1 card clock	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM1_VDD	
USIM1_RST	23	DO	(U)SIM1 card reset		
USIM1_DET	22	DI	(U)SIM1 card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Active low. Externally pull it up to 1.8 V. If unused, keep it open.
USIM2_VDD	21	PO	(U)SIM2 card power supply	$I_O$max = 67 mA **1.8 V (U)SIM:** Vmax = 1.85 V Vmin = 1.75 V **2.95 V (U)SIM:** Vmax = 3.1 V Vmin = 2.8 V	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM2_DATA	20	DIO	(U)SIM2 card data	V_{IL}max = 0.2 × USIM2_VDD V_{IH}min = 0.7 × USIM2_VDD V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM2_VDD	Cannot be multiplexed into a generic GPIO.
USIM2_CLK	19	DO	(U)SIM2 card clock	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM2_VDD	
USIM2_RST	18	DO	(U)SIM2 card reset		
USIM2_DET	17	DI	(U)SIM2 card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Active low. Externally pull it up to 1.8 V. If unused, keep it open.
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	39	DO	SD card clock		50 Ω characteristic impedance.
SD_CMD	40	DO	SD card command		
SD_DATA0	41	DIO	SDIO data bit 0		
SD_DATA1	42	DIO	SDIO data bit 1		
SD_DATA2	43	DIO	SDIO data bit 2		
SD_DATA3	44	DIO	SDIO data bit 3		
SD_DET	45	DI	SD card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Active low.
SD_LDO21	38	PO	SD card power supply	2.95 V/841 mA	

SD_LDO4	32	PO	1.8/2.95 V output power for SD card pull-up circuits	1.8/2.95 V 22 mA	
Touch Panel Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_RST	31	DO	TP reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Active low.
TP_INT	30	DI	TP interrupt	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	1.8 V power domain.
TP_I2C_SCL	47	OD	TP I2C clock		Need to be pulled up to 1.8 V externally. Can be used for other I2C devices.
TP_I2C_SDA	48	OD	TP I2C data		
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_RST	49	DO	LCD reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
LCD_TE	50	DI	LCD tearing effect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
DSI_CLK_N	52	AO	LCD MIPI clock (-)		
DSI_CLK_P	53	AO	LCD MIPI clock (+)		
DSI_LN0_N	54	AO	LCD MIPI lane 0 data (-)		
DSI_LN0_P	55	AO	LCD MIPI lane 0 data (+)		
DSI_LN1_N	56	AO	LCD MIPI lane 1 data (-)		
DSI_LN1_P	57	AO	LCD MIPI lane 1 data (+)		
DSI_LN2_N	58	AO	LCD MIPI lane 2 data (-)		
DSI_LN2_P	59	AO	LCD MIPI lane 2 data (+)		
DSI_LN3_N	60	AO	LCD MIPI lane 3 data (-)		
DSI_LN3_P	61	AO	LCD MIPI lane 3 data (+)		
PWM	29	DO	PWM output		1.8 V power domain.
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI1_CLK_N	63	AI	MIPI CSI1 clock (-)		
CSI1_CLK_P	64	AI	MIPI CSI1 clock (+)		

CSI1_LN0_N	65	AI	MIPI CSI1 lane 0 data (-)		
CSI1_LN0_P	66	AI	MIPI CSI1 lane 0 data (+)		
CSI1_LN1_N	67	AI	MIPI CSI1 lane 1 data (-)		
CSI1_LN1_P	68	AI	MIPI CSI1 lane 1 data (+)		
CSI1_LN2_N	72	AI	MIPI CSI1 lane 2 data (-)		
CSI1_LN2_P	73	AI	MIPI CSI1 lane 2 data (+)		
CSI1_LN3_N	70	AI	MIPI CSI1 lane 3 data (-)		
CSI1_LN3_P	71	AI	MIPI CSI1 lane 3 data (+)		
CSI0_CLK_N	157	AI	MIPI CSI0 clock (-)		
CSI0_CLK_P	196	AI	MIPI CSI0 clock (+)		
CSI0_LN0_N	158	AI	MIPI CSI0 lane 0 data (-)		
CSI0_LN0_P	197	AI	MIPI CSI0 lane 0 data (+)		
CSI0_LN1_N	159	AI	MIPI CSI0 lane 1 data (-)		
CSI0_LN1_P	198	AI	MIPI CSI0 lane 1 data (+)		
CSI0_LN2_N	160	AI	MIPI CSI0 lane 2 data (-)		
CSI0_LN2_P	199	AI	MIPI CSI0 lane 2 data (+)		
CSI0_LN3_N	161	AI	MIPI CSI0 lane 3 data (-)		
CSI0_LN3_P	200	AI	MIPI CSI0 lane 3 data (+)		
CAM0_I2C_SCL	83	OD	I2C clock of camera 0		Need to be pulled up to 1.8 V externally. Can only be used for camera I2C devices.
CAM0_I2C_SDA	84	OD	I2C data of camera 0		
CAM0_PWDN	80	DO	Power down of camera 0	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
CAM1_PWDN	82	DO	Power down of camera 1		
CAM2_PWDN	163	DO	Power down of camera 2		
CAM0_MCLK	74	DO	Master clock of camera 0		
CAM1_MCLK	75	DO	Master clock of camera 1		

CAM2_MCLK	165	DO	Master clock of camera 2		
CAM0_RST	79	DO	Reset of camera 0		
CAM1_RST	81	DO	Reset of camera 1		
CAM2_RST	164	DO	Reset of camera 2		
CAM1_I2C_SCL	166	OD	I2C clock of camera 1		Need to be pulled up to 1.8 V externally. Can only be used for camera I2C devices.
CAM1_I2C_SDA	205	OD	I2C data of camera 1		
Flash & Torch Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
FLASH_LED	180	AO	Flash/torch driver output	$I_O$max = 1 A	Supports flash and torch modes.
Indication Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CHG_LED	195	AI	Indicate the module's charging status	$I_I$max = 5 mA	
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	114	DI	Turn on/off the module		Pulled up to 1.1 V internally. Active low.
VOL_UP	95	DI	Volume up	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	If unused, keep it open. Cannot be externally pulled up. 1.8 V power domain.
VOL_DOWN	96	DI	Volume down	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
RESET_N	225	DI	Reset the module		Disabled by default and it can be enabled via software configuration.
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	94	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
DBG_RXD	93	DI	Debug UART receive	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
UART0_TXD	34	DO	UART0 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART0_RXD	35	DI	UART0 receive	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	

UART0_RTS	37	DO	DCE request to send signal to DTE	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART0_CTS	36	DI	DCE clear to send signal from DTE	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
UART1_TXD	154	DO	UART1 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART1_RXD	153	DI	UART1 receive	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
Sensor I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SENSOR_I2C_SCL	91	OD	I2C clock for external sensor		Need to be pulled up to 1.8 V externally. Can only be used for sensors.
SENSOR_I2C_SDA	92	OD	I2C data for external sensor		
RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	87	AIO	Main antenna interface		50 Ω impedance.
ANT_GNSS	121	AI	GNSS antenna interface		
ANT_DRX	131	AI	Diversity antenna interface		
ANT_WIFI/BT	77	AIO	Wi-Fi/Bluetooth antenna interface		
Antenna Tuner Control Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC_13	173	DIO	Generic RF controller		Cannot be multiplexed into a generic GPIO. Cannot be pulled up when the module is turning on.
GRFC_14	260	DIO	Generic RF controller		
GRFC_15	262	DIO	Generic RF controller		Cannot be multiplexed into a generic GPIO.
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC	128	AI	General-purpose ADC interface		The maximum input voltage is 1.875 V.
Charging Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BAT_P	133	AI	Battery voltage detect		Cannot be kept open.

			(+)		
BAT_M	183	AI	Battery voltage detect (-)		
BAT_ID	185	AI	Battery type detect	$V_I$min = 0 V $V_I$max = 1.875 V	Internally pulled down with a 100 kΩ resistor. If unused, keep it open.
BAT_THERM	134	AI	Battery temperature detect		Internally pull up by default. Supports 47 kΩ NTC thermistor by default. If unused, connect it to GND with a 47 kΩ resistor.
Vibration Motor Driver Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VIB_DRV_P	28	PO	Vibration motor driver output control	$V_O$min = 1.5 V $V_O$max = 3.3 V $I_O$max = 100 mA	Connect it to the positive pole of the motor.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	46	DI	Force the module into emergency download mode		Force the module to enter emergency download mode by pulling this pin up to LDO15A_1V8 when the module is turning on.
GNSS_LNA_EN	194	DO	GNSS LNA enable control		
NFC_CLK	181	DO	NFC clock		The default output frequency is 38.4 MHz.
CBL_PWR_N	186	DI	Initiate power-on when grounded		The module cannot be turned off when this pin is pulled down. If unused, keep it open.
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_28	33	DIO	General-purpose input/output		
GPIO_31	97	DIO	General-purpose input/output		
GPIO_32	99	DIO	General-purpose		

			input/output		
GPIO_33	108	DIO	General-purpose input/output		
GPIO_34	109	DIO	General-purpose input/output		
GPIO_35	107	DIO	General-purpose input/output		
GPIO_36	110	DIO	General-purpose input/output		
GPIO_55	100	DIO	General-purpose input/output		
GPIO_56	106	DIO	General-purpose input/output		
GPIO_57	112	DIO	General-purpose input/output		Cannot be pulled up when the module is turning on.
GPIO_58	113	DIO	General-purpose input/output		
GPIO_60	123	DIO	General-purpose input/output		
GPIO_86	182	DIO	General-purpose input/output		
GPIO_112	177	DIO	General-purpose input/output		
GPIO_111	267	DIO	General-purpose input/output		
GPIO_98	265	DIO	General-purpose input/output		
GPIO_99	105	DIO	General-purpose input/output		
GPIO_100	264	DIO	General-purpose input/output		
GPIO_101	239	DIO	General-purpose input/output		
GPIO_102	104	DIO	General-purpose input/output		
GPIO_103	103	DIO	General-purpose input/output		
GPIO_104	101	DIO	General-purpose input/output		
GPIO_105	102	DIO	General-purpose input/output		
GPIO_106	90	DIO	General-purpose		

			input/output
GPIO_107	98	DIO	General-purpose input/output
GPIO_14	118	DIO	General-purpose input/output
GPIO_15	119	DIO	General-purpose input/output
GPIO_16	116	DIO	General-purpose input/output
GPIO_17	117	DIO	General-purpose input/output
PMU_GPIO03	124	DIO	General-purpose input/output
PMU_GPIO04	115	DIO	General-purpose input/output
PMU_GPIO08	127	DIO	General-purpose input/output
PMU_GPIO07	201	DIO	General-purpose input/output

GND	
Pin Name	**Pin No.**
GND	3, 7, 12, 15, 27, 51, 62, 69, 76, 78, 85, 86, 88, 89, 120, 122, 130, 132, 135, 140, 143, 144, 162, 171, 172, 176, 187–191, 202–204, 206–224, 226–231, 233–238, 240, 241, 243–245, 247, 248, 250, 251, 255, 256, 258, 259, 261, 266, 268, 269, 271–274

RESERVED	
Pin Name	**Pin No.**
RESERVED	16, 167, 168, 169, 170, 174, 175, 178, 179, 193, 232, 242, 257, 263

NOTE

1. Keep all RESERVED and unused pins unconnected.
2. Connect all GND pins to ground.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides four VBAT pins for connection with external power supply.

3.4.2. Voltage Stability Requirements

The power supply range of the module is 3.5–4.4 V, and the recommended value is 3.8 V. The power supply performance, such as load capacity, voltage ripple, etc. will directly influences the module's performance and stability. Under ultimate conditions, the transient peak current of the module may surge up to 3 A. If the power supply capacity is not sufficient, there will be the risk that the voltage drops below 3.4 V and as a result the module powers off automatically. Therefore, make sure the input voltage never drops below 3.4 V.

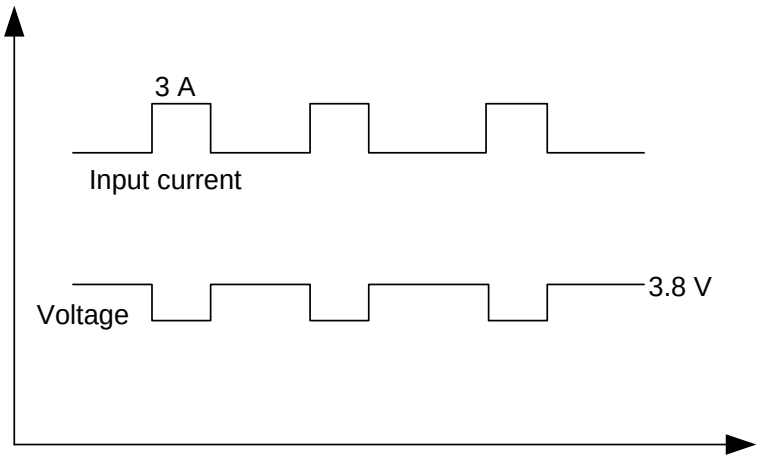


Figure 3: Voltage Drop Sample

To decrease voltage drop, use a bypass capacitor of about 100 µF with low ESR (ESR ≤ 0.7 Ω), and reserve a multi-layer ceramic chip capacitor (MLCC) array due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) to compose the MLCC array and place these capacitors close to VBAT pins. Additionally, add a 4.7 µF capacitor in parallel. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT trace should be no less than 3 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to guarantee the stability of the power source, please use a TVS and place it as close to the VBAT pins as possible to enhance surge protection. The following figure shows the star configuration of the power supply.

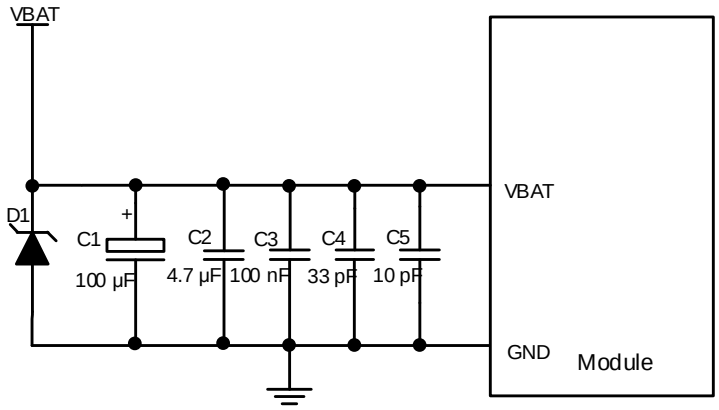


Figure 4: Reference Circuit for the Power Supply

3.4.3. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 3 A at least. If the voltage difference between the input and output is not too big, use an LDO when supplying power to the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure shows a reference design for +5 V input power source. The typical output voltage is 3.8 V and the maximum load current is 5.0 A.

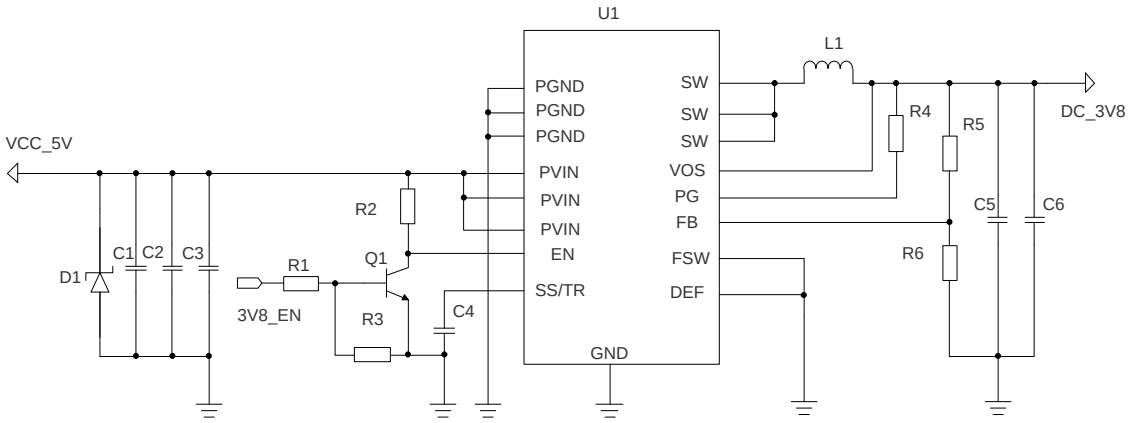


Figure 5: Reference Circuit of Power Supply

NOTE

1. In an abnormal state, it is recommended to restart the module by switching off and then switching back on the power supply.

2. The module supports battery charging by default. If the above power supply design is adopted, disable the charging function by software, or connect VBAT to a Schottky diode in series to avoid the reverse current to the power supply IC.

3.5. Turn On/Off

3.5.1. Turn On with PWRKEY

The module can be turned on by driving the PWRKEY pin low for at least 1.6 s. The PWRKEY pin is pulled up to 1.1 V internally. It is recommended to use an open collector driver to control PWRKEY. A simple reference circuit is illustrated in the following figure.

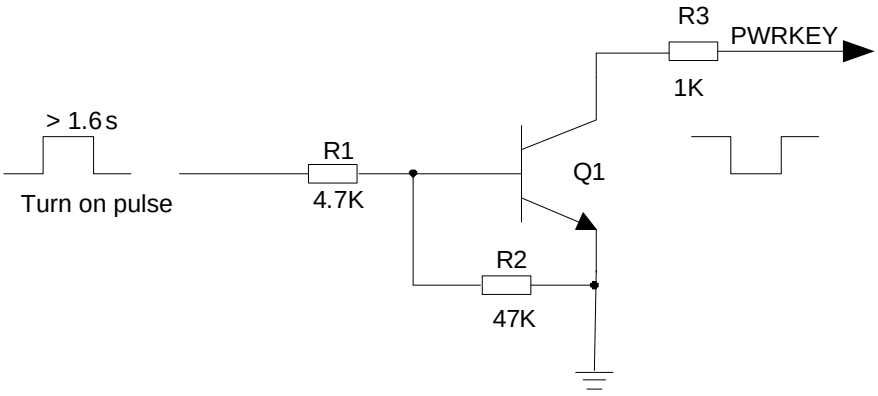


Figure 6: Turn On the Module with Open Collector Driver

Another way to control PWRKEY is by using a button directly. You must place a TVS component nearby the button for ESD protection. A reference circuit is shown by the following figure.

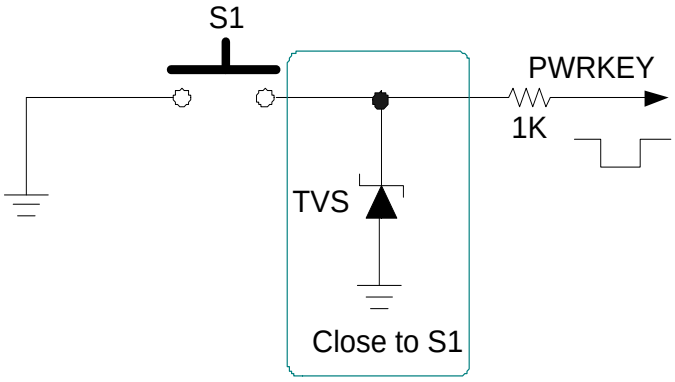


Figure 7: Turn On the Module Using Button

The turning-on scenario is illustrated in the following figure.

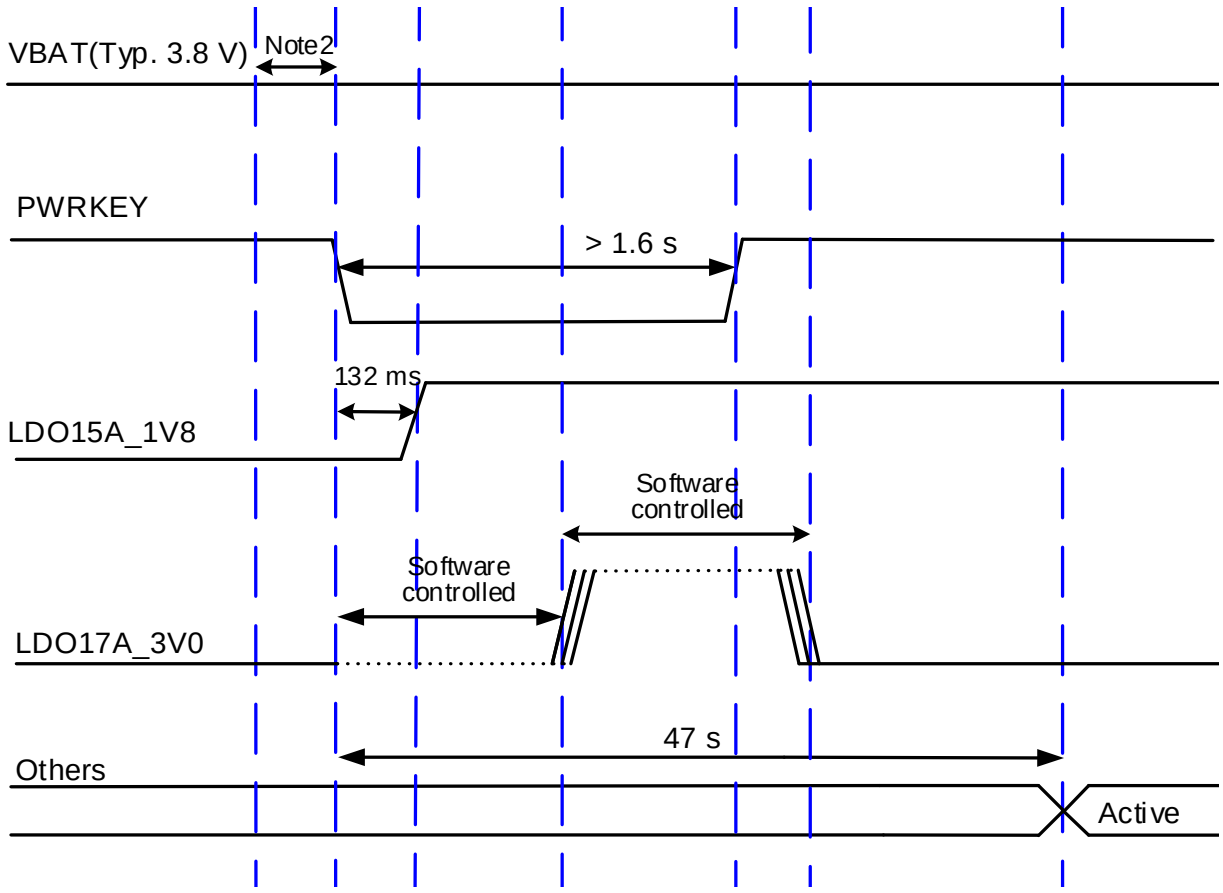


Figure 8: Turn-on Timing

NOTE

1. When the module is turned on for the first time, the turn-on timing may be different from that shown above.
2. Make sure that VBAT is stable before pulling down PWRKEY. It is recommended to wait until VBAT is stable at 3.8 V for at least 30 ms before pulling down PWRKEY. Additionally, do not keep pulling PWRKEY down all the time.

3.5.2. Turn Off

Drive the PWRKEY pin low for at least 1 s, and then choose to turn off the module when the prompt window comes up.

You can also force the module to turn off by driving PWRKEY low for at least 8 s. The force-turn-off timing is illustrated by the following figure.

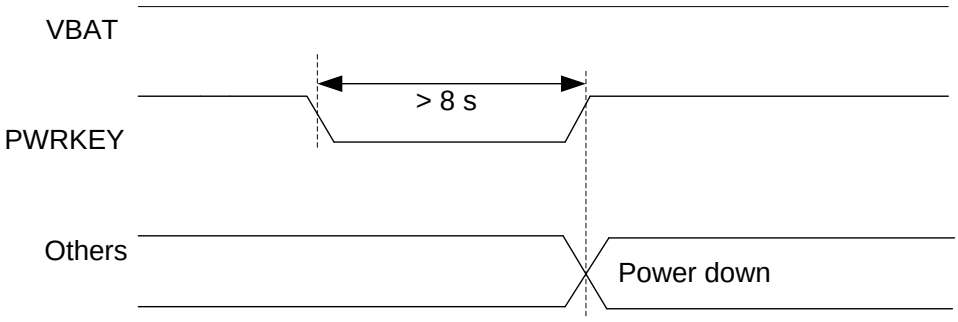


Figure 9: Forced Turn-off Timing

3.6. VRTC

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supplied to VBAT. The external power source can be a rechargeable battery (such as a coin cell) according to application demands. A reference circuit design is shown below.

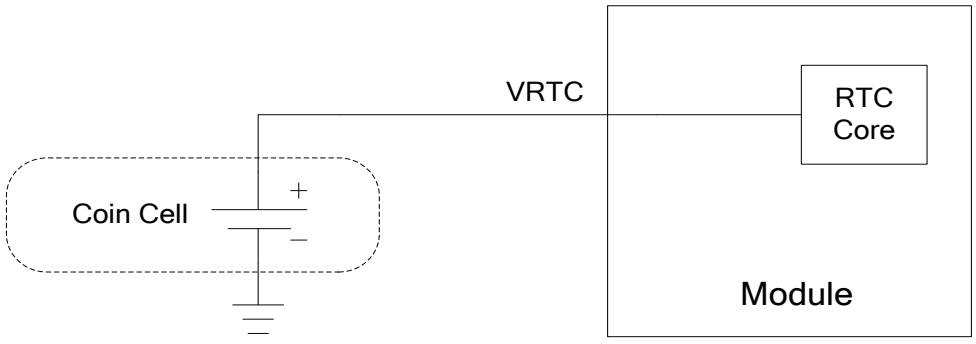


Figure 10: RTC Powered by Coin Cell

If RTC is ineffective, it can be synchronized through the network after the module is turned on. The recommended input voltage range for VRTC is 2.5–3.2 V and the recommended typical value is 3.0 V.

3.7. Power Output

The module supports output of regulated voltages for peripheral circuits. In applications, it is recommended to use a 33 pF and a 10 pF capacitor in parallel in the circuit to suppress high-frequency noise.

Table 8: Power Description

Pin Name	Pin No.	Default Voltage (V)	Driving Current (mA)	@ Idle State
LDO15A_1V8	111	1.8	200	Keeps ON
LDO_IOVDD	125	1.8	300	-
VDD_2V8	129	2.8	500	-
LDO17A_3V0	156	3.0	192	-
SD_LDO21	38	2.95	841	-
SD_LDO4	32	1.8/2.95	22	-
USIM1_VDD	26	1.8/2.95	67	-
USIM2_VDD	21	1.8/2.95	67	-

3.8. Charging Interface

The module supports battery charging. The battery charger IC in the module supports trickle charging, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion batteries.

- Trickle charging: There are two steps in this mode. When the battery voltage is below 2.1 V, a 90 mA trickle charging current is applied to the battery. When the battery voltage is charged up and is between 2.1 V and 3.4 V, the charging current can be set to 400 mA maximally.
- Constant current mode (CC mode): When the battery is increased to 3.4 to 4.2 V, the system will switch to CC mode. The maximum charging current is 1.85 A when an adapter is used for battery charging, and the maximum charging current is 450 mA for USB charging.
- Constant voltage mode (CV mode): When the battery voltage reaches the final value 4.35 V, the system will switch to CV mode and the charging current will decrease gradually. When the battery level reaches 100 %, charging is completed.

Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
BAT_P	133	AI	Battery voltage detect (+)	Cannot be kept open.
BAT_M	183	AI	Battery voltage detect (-)	
BAT_THERM	134	AI	Battery temperature detect	Internal pull up by default. Supports 47 kΩ NTC thermistor by default. If unused, connect it to GND with a 47 kΩ resistor.
BAT_ID	185	AI	Battery type detect	Internally pulled down with a 100 kΩ resistor. If unused, keep it open.

The module supports battery temperature detection in the condition that the battery integrates a thermistor (47 kΩ 1 % NTC thermistor with a B-constant of 4050 K by default) and the thermistor is connected to BAT_THERM pin. If the BAT_THERM pin is not connected, there will be malfunctions such as battery charging failure, battery level display error, etc. The battery charge temperature range varies with different types of batteries.

A reference design for the battery charging circuit is shown below.

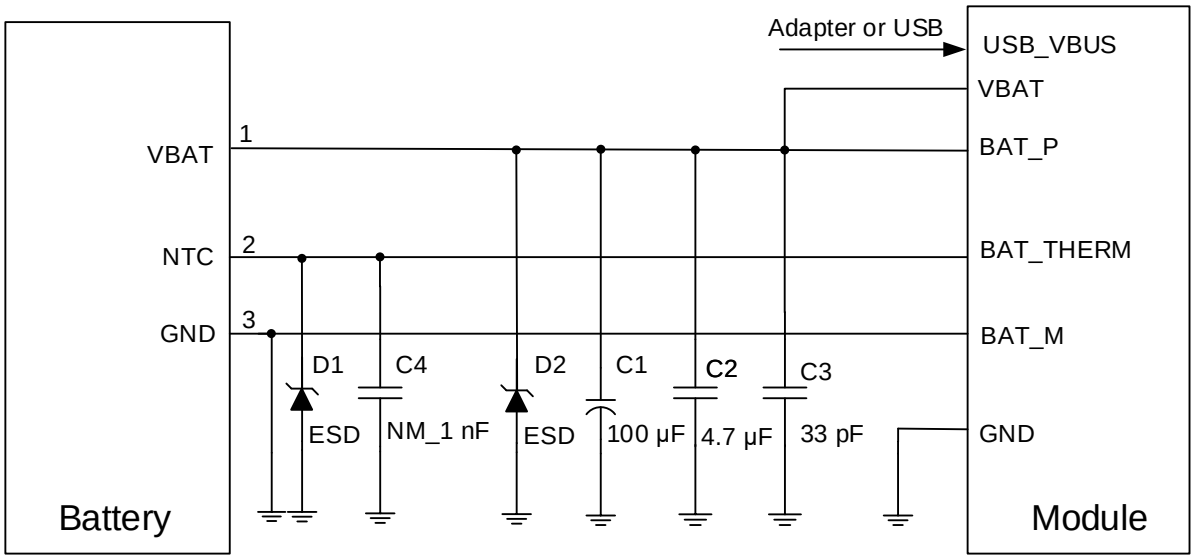


Figure 11: Reference Design for Battery Charging Circuit

Mobile devices such as mobile phones or handheld POS systems are powered by batteries. For different batteries, you should modify the charging and discharging curve correspondingly to achieve the best performance.

If the thermistor is not available in the battery, or an adapter is utilized to power the module, you must connect BAT_THERM to GND via a 47 kΩ resistor. Otherwise, the system may mistakenly judge that the battery temperature is abnormal, and therefore cause battery charging failure.

BAT_P and BAT_M must be connected. Otherwise, exceptions in voltage detection will be caused, with associated problems of turn-on/off and battery charging/discharging.

3.9. USB Interface (Type-C)

The module provides one USB interface which complies with both USB 3.1 and USB 2.0 specifications and supports superspeed (5 Gbps) and high-speed (480 Mbps), and full-speed (12 Mbps) modes. The USB interface supports USB OTG and is used for AT command transmission, data transmission, software debugging and firmware upgrade.

The module only supports USB Type-C. The USB interface has one USB 2.0 compliant high-speed differential channel (USB_DP, USB_DM) and one USB 3.1 compliant superspeed differential channel (USB_SS1_RX_P/M, USB_SS1_TX_P/M and USB_SS2_RX_P/M, USB_SS2_TX_P/M).

When Type-C is plugged in with one side up, the external device is detected by USB_CC1, and the data will be transmitted through USB_SS1; when it is plugged in with the other side up, the external device is detected by USB_CC2, and the data will be transmitted through USB_SS2. The following table shows the pin definition of USB interface.

Table 10: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	141, 142	PIO	Charging power input. Power supply output for OTG device. USB/adaptor insertion detection	Maximum output current is 500 mA.
USB_DM	13	AIO	USB differential data (-)	90 Ω differential impedance. USB 2.0 standard compliant.
USB_DP	14	AIO	USB differential data (+)	
USB_SS1_RX_P	252	AI	USB 3.1 channel 1 superspeed receive (+)	90 Ω differential impedance. USB 3.1 standard compliant.
USB_SS1_RX_M	270	AI	USB 3.1 channel 1 superspeed receive (-)	
USB_SS1_TX_P	254	AO	USB 3.1 channel 1 superspeed transmit (+)	
USB_SS1_TX_M	253	AO	USB 3.1 channel 1 superspeed transmit (-)	

USB_SS2_RX_P	152	AI	USB 3.1 channel 2 superspeed receive (+)	
USB_SS2_RX_M	192	AI	USB 3.1 channel 2 superspeed receive (-)	
USB_SS2_TX_P	150	AO	USB 3.1 channel 2 superspeed transmit (+)	
USB_SS2_TX_M	151	AO	USB 3.1 channel 2 superspeed transmit (-)	
USB_CC1	249	AI	USB Type-C detect 1	-
USB_CC2	246	AI	USB Type-C detect 2	-

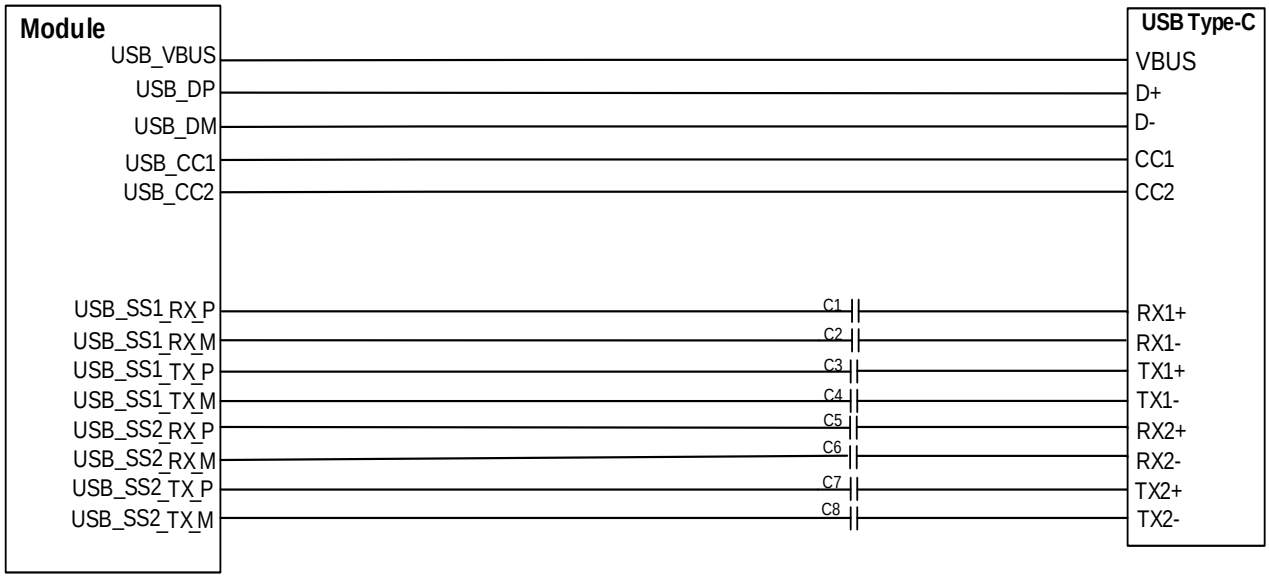


Figure 12: USB Interface Reference Design (OTG Supported)

In order to ensure USB performance, comply with the following principles when designing the USB interface.

- Route the USB signal traces as a differential pair with total grounding. The impedance of USB differential trace should be controlled to 90 Ω.
- Keep the ESD protection component as close as possible to the USB connector. Pay attention to the influence of junction capacitance of ESD protection component on USB data lines. Typically, the capacitance value should be less than 2 pF for USB 2.0 and less than 0.5 pF for USB 3.1.
- Do not route signal traces under crystals, oscillators, magnetic devices or RF signal traces. Route the USB differential traces in inner-layer with ground shielding on not only the upper and lower layers but also the right and left sides.
- Make sure the intra-pair length difference within USB 2.0 differential pair does not exceed 2 mm, and that within USB 3.1 Rx or Tx differential pair does not exceed 0.7 mm.
- The spacing between USB signals and all other signals should be at least 4 times the trace width while the signals between Rx and Tx should be at least 3 times the trace width.

- For USB 3.1, it is suggested to do simulation after the design is completed. If the cable is too long or there are too many vias, a redriver needs to be added to ensure the quality of signal transmission if necessary.

Table 11: USB Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Length Difference (DP - DM)
13	USB_DM	24.13	0.24
14	USB_DP	24.37	
252	USB_SS1_RX_P	16.33	-0.17
270	USB_SS1_RX_M	16.50	
254	USB_SS1_TX_P	10.07	-0.07
253	USB_SS1_TX_M	10.14	
152	USB_SS2_RX_P	17.74	-0.28
192	USB_SS2_RX_M	18.02	
150	USB_SS2_TX_P	20.84	0.3
151	USB_SS2_TX_M	20.54	

3.10. UART Interfaces

The module provides three UART interfaces:

- UART0: four-wire UART interface, supports RTS and CTS hardware flow control
- UART4 (debug UART): two-wire UART interface, used for debugging by default
- UART1: two-wire UART interface

Table 12: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
UART0_TXD	34	DO	UART0 transmit	1.8 V power domain. If unused, keep it open.
UART0_RXD	35	DI	UART0 receive	

UART0_RTS	37	DO	DCE request to send signal to DTE
UART0_CTS	36	DI	DCE clear to send signal from DTE
DBG_TXD	94	DO	Debug UART transmit
DBG_RXD	93	DI	Debug UART receive
UART1_TXD	154	DO	UART1 transmit
UART1_RXD	153	DI	UART1 receive

UART0 is a four-wire UART interface with 1.8 V power domain. You should use a level translator if your application is equipped with a 3.3 V UART interface. The following figure shows a reference design.

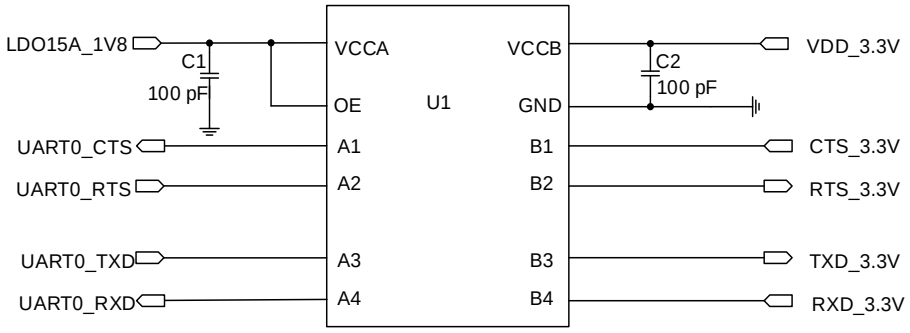


Figure 13: Reference Circuit with Level Translator Chip for UART0

The following figure presents an example of connection between the module and a PC. It is recommended to add a level translator and an RS-232 level translator chip between the module and the PC.

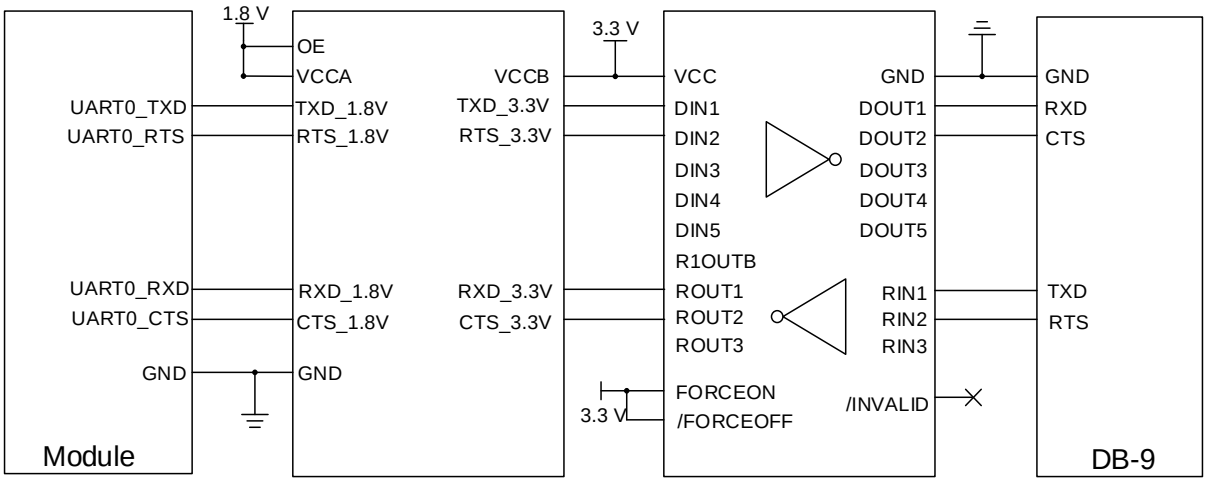


Figure 14: RS-232 Level Match Circuit for UART0

NOTE

UART4 (debug UART) and UART1 are similar to UART0. Please refer to the reference design of UART0 for the designs of the two UARTs.

3.11. (U)SIM Interfaces

The module provides two (U)SIM interfaces that meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby is supported by default. Either 1.8 V or 2.95 V (U)SIM card is supported, and the (U)SIM card is powered by the internal power supply of the module.

Table 13: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	26	PO	(U)SIM1 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM1_DATA	25	DIO	(U)SIM1 card data	Cannot be multiplexed into a generic GPIO.
USIM1_CLK	24	DO	(U)SIM1 card clock	
USIM1_RST	23	DO	(U)SIM1 card reset	
USIM1_DET	22	DI	(U)SIM1 card hot-plug detect	Active low. Externally pull it up to 1.8 V. If unused, keep it open.
USIM2_VDD	21	PO	(U)SIM2 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM2_DATA	20	DIO	(U)SIM2 card data	Cannot be multiplexed into a generic GPIO.
USIM2_CLK	19	DO	(U)SIM2 card clock	
USIM2_RST	18	DO	(U)SIM2 card reset	
USIM2_DET	17	DI	(U)SIM2 card hot-plug detect	Active low. Externally pull it up to 1.8 V. If unused, keep it open.

The module supports (U)SIM card hot-plug via the USIM_DET pins. This function is disabled by default via software. To enable it, contact Quectel Technical Support to change the software configuration. A reference circuit for (U)SIM interface with an 8-pin (U)SIM card connector is shown below.

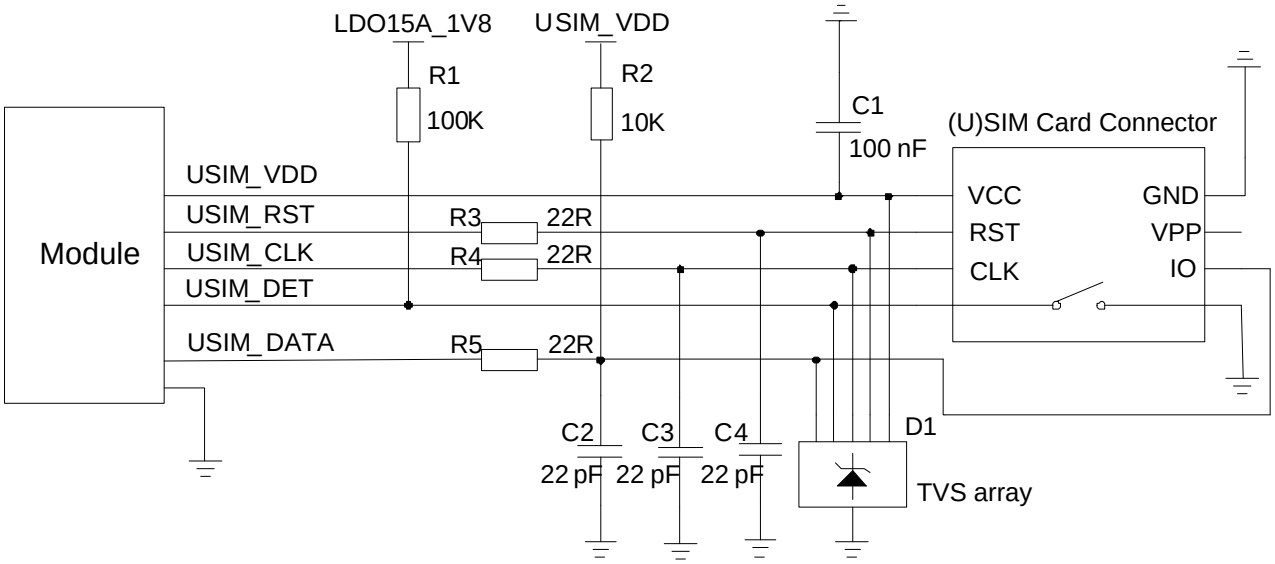


Figure 15: Reference Circuit for (U)SIM Interface with an 8-pin (U)SIM Card Connector

If you do not need hot-plug detection, keep USIM1_DET and USIM2_DET pins open. The following is a reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector when hot-plug detection is not needed.

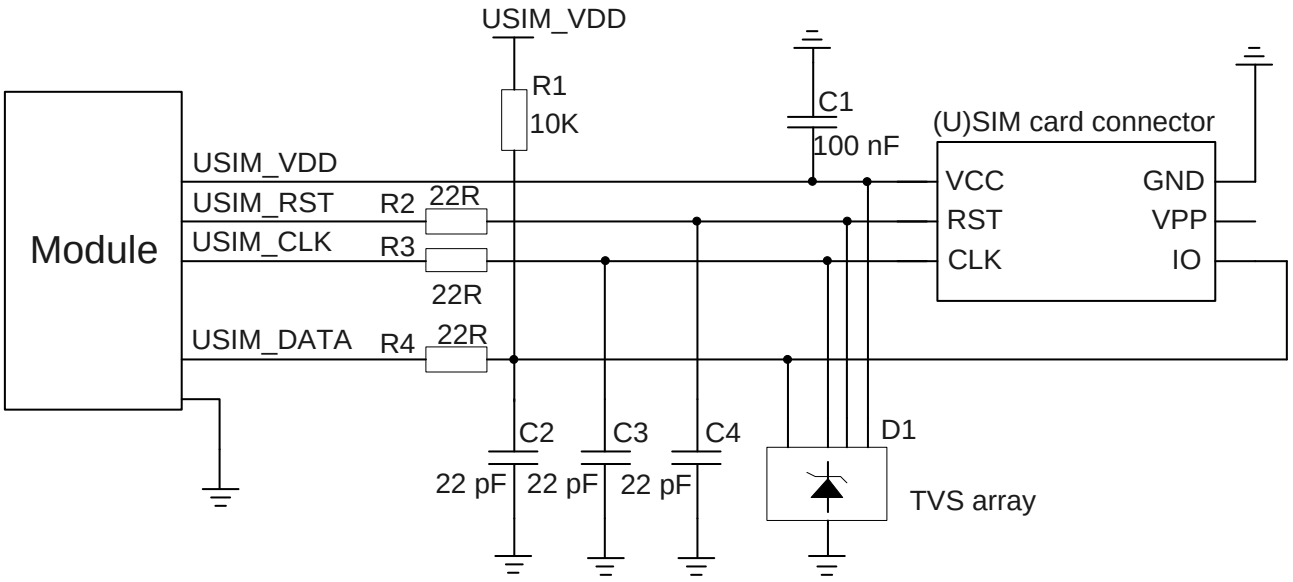


Figure 16: Reference Circuit for (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design:

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Reserve a filter capacitor for USIM_VDD, and its maximum capacitance should not exceed 1 μF. Additionally, place the capacitor near the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground. USIM_RST also needs ground protection.
- To ensure better ESD protection, it is recommended to add a TVS array with a parasitic capacitance not exceeding 10 pF. Add 22 Ω resistors in series between the module and (U)SIM card to suppress EMI such as spurious transmission. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- Add 22 pF capacitors in parallel on USIM_DATA, USIM_CLK and USIM_RST signal lines to filter RF interference, and place them as close to the (U)SIM card connector as possible.

3.12. SD Card Interface

SD Card interface of the module supports SD 3.0 protocol. The pin definition of SD card interface is shown below.

Table 14: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	39	DO	SD card clock	50 Ω characteristic impedance.
SD_CMD	40	DO	SD card command	
SD_DATA0	41	DIO	SDIO data bit 0	
SD_DATA1	42	DIO	SDIO data bit 1	
SD_DATA2	43	DIO	SDIO data bit 2	
SD_DATA3	44	DIO	SDIO data bit 3	
SD_DET	45	DI	SD card hot-plug detect	Active low.
SD_LDO21	38	PO	SD card power supply	-
SD_LDO4	32	PO	1.8/2.95 V output power for SD card pull-up circuits	-

A reference circuit for the SD card interface is shown below.

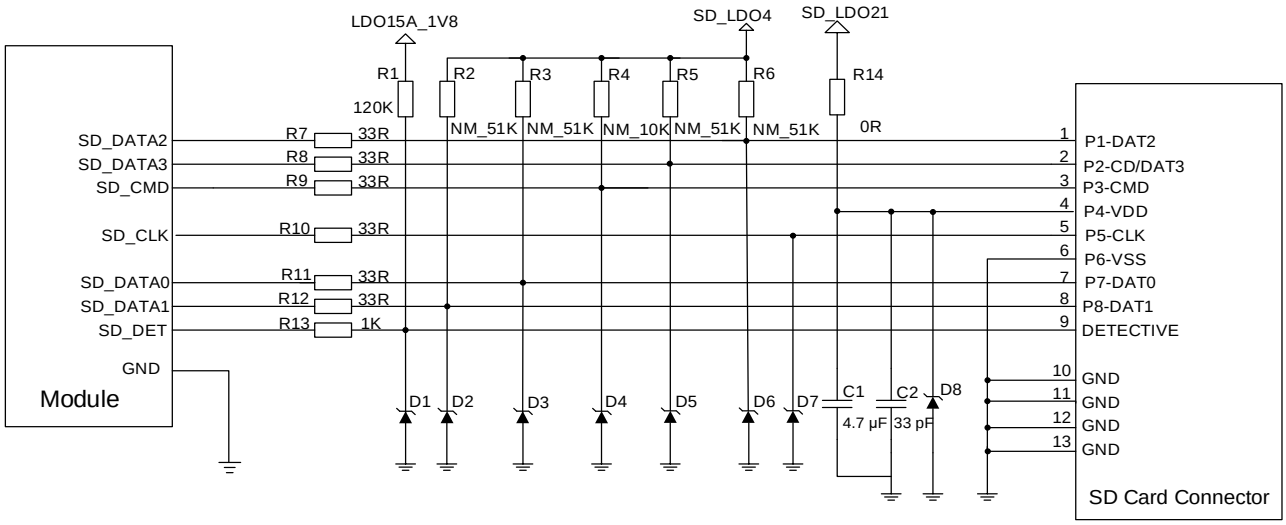


Figure 17: Reference Circuit for the SD Card Interface

SD_LDO21 is the power supply for the SD card and can provide up to 841 mA output current. Due to the high output current, it is recommended that the trace width should be at least 0.8 mm. To ensure output current stability, add a 4.7 µF and a 33 pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK, SD_DATA0, SD_DATA1, SD_DATA2, and SD_DATA3 are all high-speed signal lines. In PCB design, control the characteristic impedance of them to 50 Ω, and do not cross them with other traces. It is recommended to route the traces on the inner layer of the PCB and keep them of the same length. Additionally, SD_CLK needs ground shielding separately.

Trace length requirements:

- Control the impedance to 50 Ω ±10 % and add ground shielding.
- Keep the trace length difference among SD_CLK, SD_CMD and SD_DATA less than 2 mm.

Table 15: SD Card Trace Length Inside the Module

Pin No.	Signal	Length (mm)
39	SD_CLK	35.01
40	SD_CMD	35.12
41	SD_DATA0	34.98
42	SD_DATA1	35.04
43	SD_DATA2	34.98

44	SD_DATA3	35.10

3.13. GPIO Interfaces

The module has abundant GPIO interfaces with a power domain of 1.8 V. The pin definition is listed below.

Table 16: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GPIO_28	33	DIO	General-purpose input/output	
GPIO_31	97	DIO	General-purpose input/output	
GPIO_32	99	DIO	General-purpose input/output	
GPIO_33	108	DIO	General-purpose input/output	
GPIO_34	109	DIO	General-purpose input/output	
GPIO_35	107	DIO	General-purpose input/output	
GPIO_36	110	DIO	General-purpose input/output	
GPIO_55	100	DIO	General-purpose input/output	
GPIO_56	106	DIO	General-purpose input/output	
GPIO_57	112	DIO	General-purpose input/output	Cannot be pulled up when the module is turning on.
GPIO_58	113	DIO	General-purpose input/output	
GPIO_60	123	DIO	General-purpose input/output	
GPIO_86	182	DIO	General-purpose input/output	
GPIO_112	177	DIO	General-purpose input/output	
GPIO_111	267	DIO	General-purpose input/output	
GPIO_98	265	DIO	General-purpose input/output	
GPIO_99	105	DIO	General-purpose input/output	
GPIO_100	264	DIO	General-purpose input/output	
GPIO_101	239	DIO	General-purpose input/output	

GPIO_102	104	DIO	General-purpose input/output
GPIO_103	103	DIO	General-purpose input/output
GPIO_104	101	DIO	General-purpose input/output
GPIO_105	102	DIO	General-purpose input/output
GPIO_106	90	DIO	General-purpose input/output
GPIO_107	98	DIO	General-purpose input/output
GPIO_14	118	DIO	General-purpose input/output
GPIO_15	119	DIO	General-purpose input/output
GPIO_16	116	DIO	General-purpose input/output
GPIO_17	117	DIO	General-purpose input/output
PMU_GPIO03	124	DIO	General-purpose input/output
PMU_GPIO04	115	DIO	General-purpose input/output
PMU_GPIO08	127	DIO	General-purpose input/output
PMU_GPIO07	201	DIO	General-purpose input/output

NOTE

For more details about GPIO configuration, see ***document [2]***.

3.14. I2C Interfaces

The module provides four I2C interfaces. All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V. The sensor I2C interface only supports sensors of ADSP architecture. CAM0 I2C and CAM1 I2C signals are controlled by the Kernel code and support connection to radio-output-related devices.

Table 17: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
TP_I2C_SCL	47	OD	TP I2C clock	Need to be pulled up to

TP_I2C_SDA	48	OD	TP I2C data	1.8 V externally. Can be used for other I2C devices.
CAM0_I2C_SCL	83	OD	I2C clock of camera 0	Can only be used for camera I2C devices.
CAM0_I2C_SDA	84	OD	I2C data of camera 0	
CAM1_I2C_SCL	166	OD	I2C clock of camera 1	
CAM1_I2C_SDA	205	OD	I2C data of camera 1	
SENSOR_I2C_SCL	91	OD	I2C clock for external sensor	Can only be used to for sensors.
SENSOR_I2C_SDA	92	OD	I2C data for external sensor	

3.15. ADC Interface

The module supports one Analog-to-Digital Converter (ADC) interface. The ADC interface supports resolution of up to 15 bits. The pin definition is shown below.

Table 18: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC	128	AI	General-purpose ADC interface	The maximum input voltage is 1.875 V.

3.16. Motor Drive Interface

The pin definition of the motor drive interface is listed below.

Table 19: Pin Definition of Motor Drive Interface

Pin Name	Pin No.	I/O	Description	Comment
VIB_DRV_P	28	PO	Vibration motor driver output control	Connect it to the positive pole of the motor.

The motor is driven by an exclusive circuit, and a reference circuit is shown below.

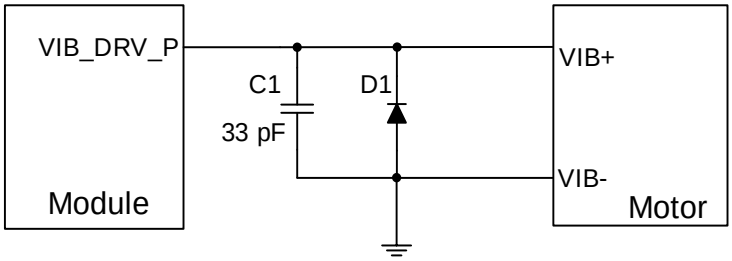


Figure 18: Reference Circuit for Motor Connection

When the motor stops working and the VIB_DRV_P is disconnected, the redundant electricity on the motor can be discharged from the circuit loop formed by diodes, thus avoiding damage to components.

3.17. LCM Interface

The module provides one LCM interface, which is MIPI DSI standard compliant. The interface supports high-speed differential data transmission and supports HD+ display (1680 × 720 @ 60 fps). The pin definition of the LCM interface is shown below.

Table 20: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_RST	49	DO	LCD reset	1.8 V power domain.
LCD_TE	50	DI	LCD tearing effect	
DSI_CLK_N	52	AO	LCD MIPI clock (-)	-
DSI_CLK_P	53	AO	LCD MIPI clock (+)	-
DSI_LN0_N	54	AO	LCD MIPI lane 0 data (-)	-
DSI_LN0_P	55	AO	LCD MIPI lane 0 data (+)	-
DSI_LN1_N	56	AO	LCD MIPI lane 1 data (-)	-
DSI_LN1_P	57	AO	LCD MIPI lane 1 data (+)	-
DSI_LN2_N	58	AO	LCD MIPI lane 2 data (-)	-

DSI_LN2_P	59	AO	LCD MIPI lane 2 data (+)	-
DSI_LN3_N	60	AO	LCD MIPI lane 3 data (-)	-
DSI_LN3_P	61	AO	LCD MIPI lane 3 data (+)	-
PWM	29	DO	PWM output	1.8 V power domain.

A reference circuit for the LCM interface is shown below.

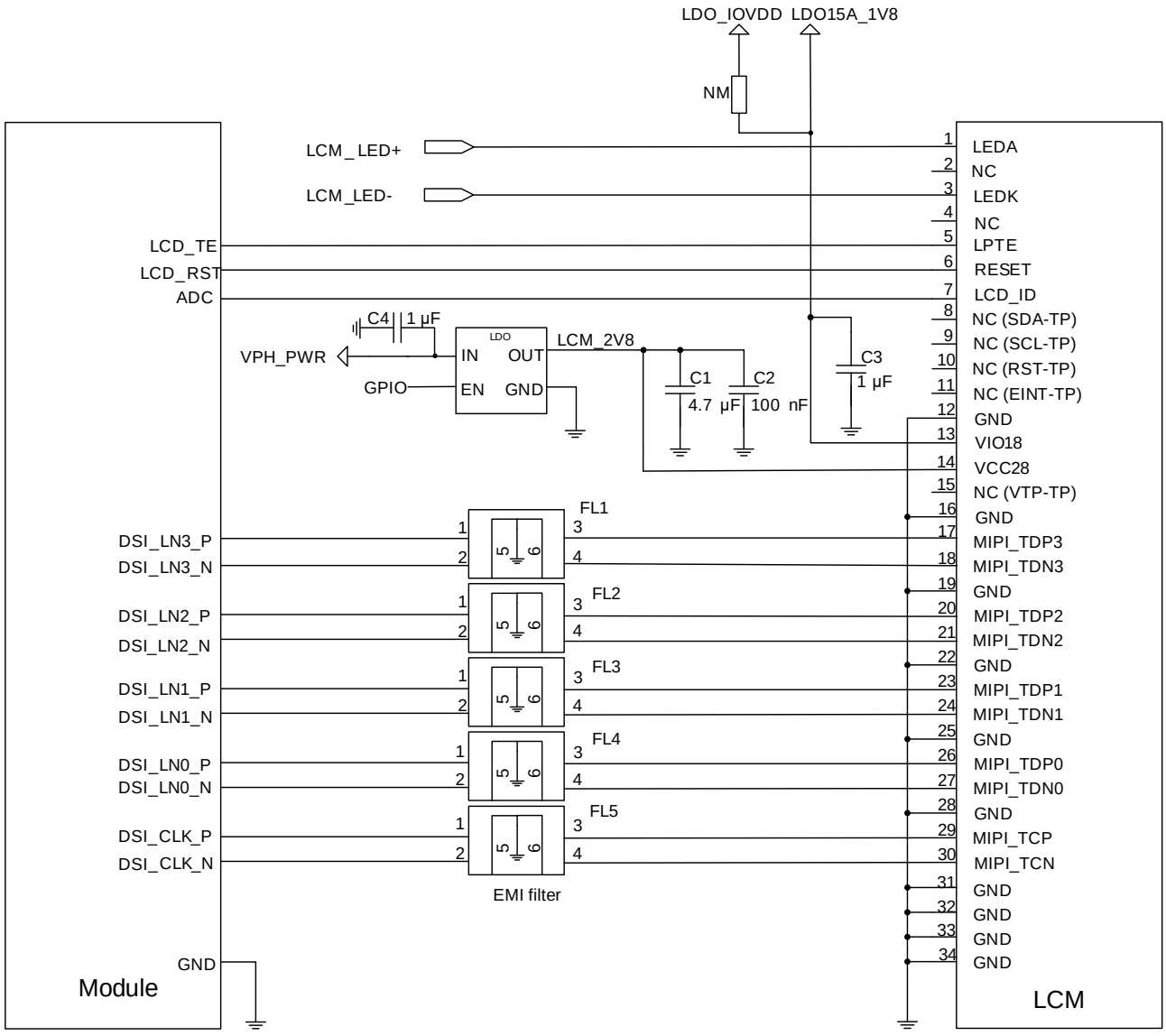


Figure 19: Reference Circuit Design for LCM Interface

MIPI are high-speed signal lines. It is recommended to add common-mode filters in series near the LCM connector, to improve protection against electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that the LCM factory should burn an OTP register to distinguish different screens. You can also connect the LCD_ID pin of LCM to the ADC pin of the module, but you need to make sure that the output voltage of LCD_ID should not exceed the voltage range of the ADC pin.

You can design the external backlight driving circuit for LCM according to actual requirements. A reference circuit design is shown in the following figure, in which the PWM pin is used to adjust the backlight brightness.

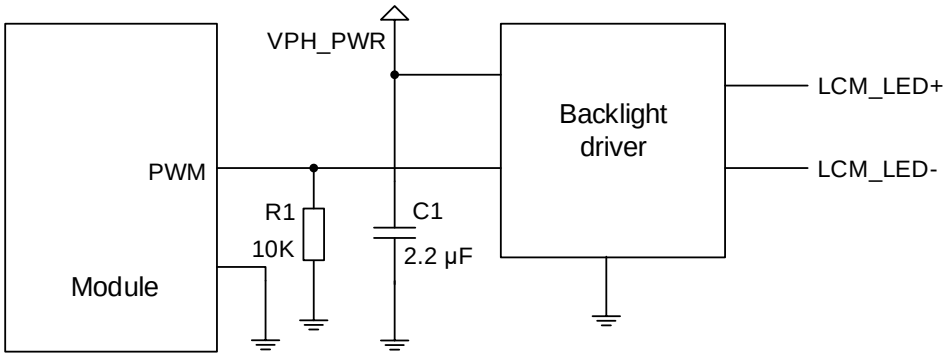


Figure 20: Reference Design for LCM External Backlight Driving Circuit

3.18. Flash Interface

The module supports one flash LED driver, with maximum output current up to 1 A.

Table 21: Pin Definition of Flash Interface

Pin Name	Pin No.	I/O	Description	Comment
FLASH_LED	180	AO	Flash/torch driver output	Supports flash and torch modes.

NOTE

Flash current is programmable in step 12.5 mA (max. 1 A) or 5 mA (max. 640 mA).

3.19. Touch Panel Interface

The module provides one I2C interface for the connection to a Touch Panel (TP), and also provides the corresponding power supply and interrupt pins. The definition of TP interface pin is illustrated below.

Table 22: Pin Definition of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
TP_RST	31	DO	TP reset	1.8 V voltage domain. Active low.
TP_INT	30	DI	TP interrupt	1.8 V voltage domain.
TP_I2C_SCL	47	OD	TP I2C clock	Need to be pulled up to 1.8 V externally. Can be used for other I2C devices.
TP_I2C_SDA	48	OD	TP I2C data	

A reference circuit for the TP interface is shown below.

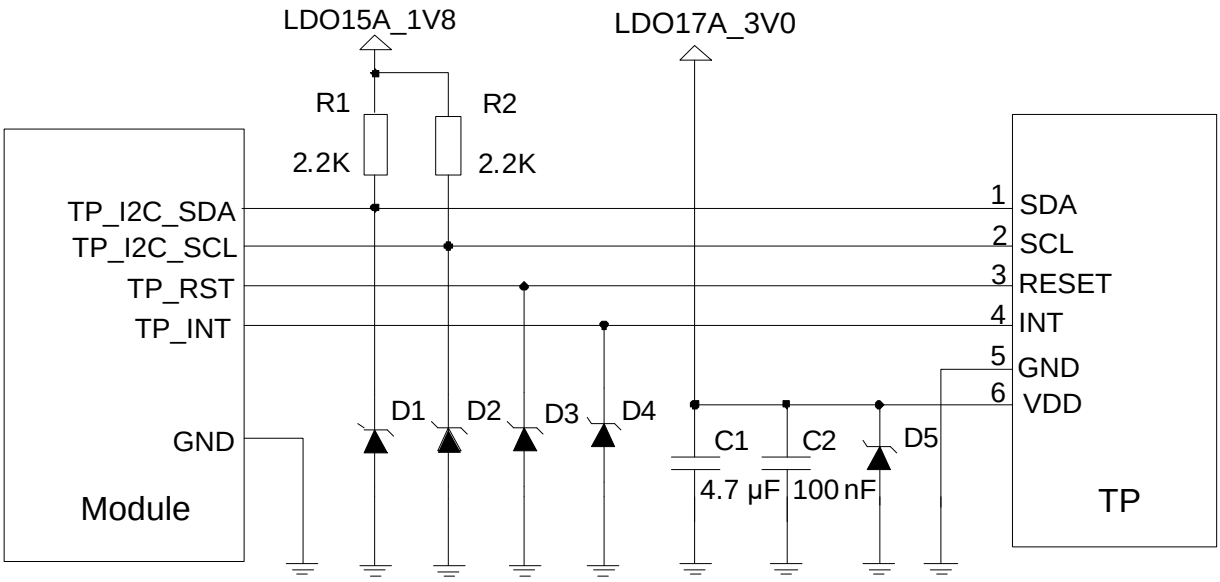


Figure 21: Reference Circuit Design for the Touch Panel Interface

3.20. Camera Interfaces

Based on MIPI CSI standard, the module supports two cameras (4-lane + 4-lane) or three cameras (4-lane + 2-lane + 1-lane), and the maximum pixel of the camera can be up to 25 MP. The video and photo quality are determined by various factors such as the camera sensor and camera lens specifications.

Table 23: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
CSI1_CLK_N	63	AI	MIPI CSI1 clock (-)	-
CSI1_CLK_P	64	AI	MIPI CSI1 clock (+)	-
CSI1_LN0_N	65	AI	MIPI CSI1 lane 0 data (-)	-
CSI1_LN0_P	66	AI	MIPI CSI1 lane 0 data (+)	-
CSI1_LN1_N	67	AI	MIPI CSI1 lane 1 data (-)	-
CSI1_LN1_P	68	AI	MIPI CSI1 lane 1 data (+)	-
CSI1_LN2_N	72	AI	MIPI CSI1 lane 2 data (-)	-
CSI1_LN2_P	73	AI	MIPI CSI1 lane 2 data (+)	-
CSI1_LN3_N	70	AI	MIPI CSI1 lane 3 data (-)	-
CSI1_LN3_P	71	AI	MIPI CSI1 lane 3 data (+)	-
CSI0_CLK_N	157	AI	MIPI CSI0 clock (-)	-
CSI0_CLK_P	196	AI	MIPI CSI0 clock (+)	-
CSI0_LN0_N	158	AI	MIPI CSI0 lane 0 data (-)	-
CSI0_LN0_P	197	AI	MIPI CSI0 lane 0 data (+)	-
CSI0_LN1_N	159	AI	MIPI CSI0 lane 1 data (-)	-
CSI0_LN1_P	198	AI	MIPI CSI0 lane 1 data (+)	-
CSI0_LN2_N	160	AI	MIPI CSI0 lane 2 data (-)	-
CSI0_LN2_P	199	AI	MIPI CSI0 lane 2 data (+)	-
CSI0_LN3_N	161	AI	MIPI CSI0 lane 3 data (-)	-

CSI0_LN3_P	200	AI	MIPI CSI0 lane 3 data (+)	-
CAM0_I2C_SCL	83	OD	I2C clock of camera 0	Need to be pulled up to 1.8 V externally. Can only be used for camera I2C devices.
CAM0_I2C_SDA	84	OD	I2C data of camera 0	
CAM0_PWDN	80	DO	Power down of camera 0	1.8 V power domain.
CAM1_PWDN	82	DO	Power down of camera 1	
CAM2_PWDN	163	DO	Power down of camera 2	
CAM0_MCLK	74	DO	Master clock of camera 0	
CAM1_MCLK	75	DO	Master clock of camera 1	
CAM2_MCLK	165	DO	Master clock of camera 2	
CAM0_RST	79	DO	Reset of camera 0	
CAM1_RST	81	DO	Reset of camera 1	
CAM2_RST	164	DO	Reset of camera 2	
CAM1_I2C_SCL	166	OD	I2C clock of camera 1	Need to be pulled up to 1.8 V externally. Can only be used for camera I2C devices.
CAM1_I2C_SDA	205	OD	I2C data of camera 1	

The following is a reference circuit design for 3-camera applications.

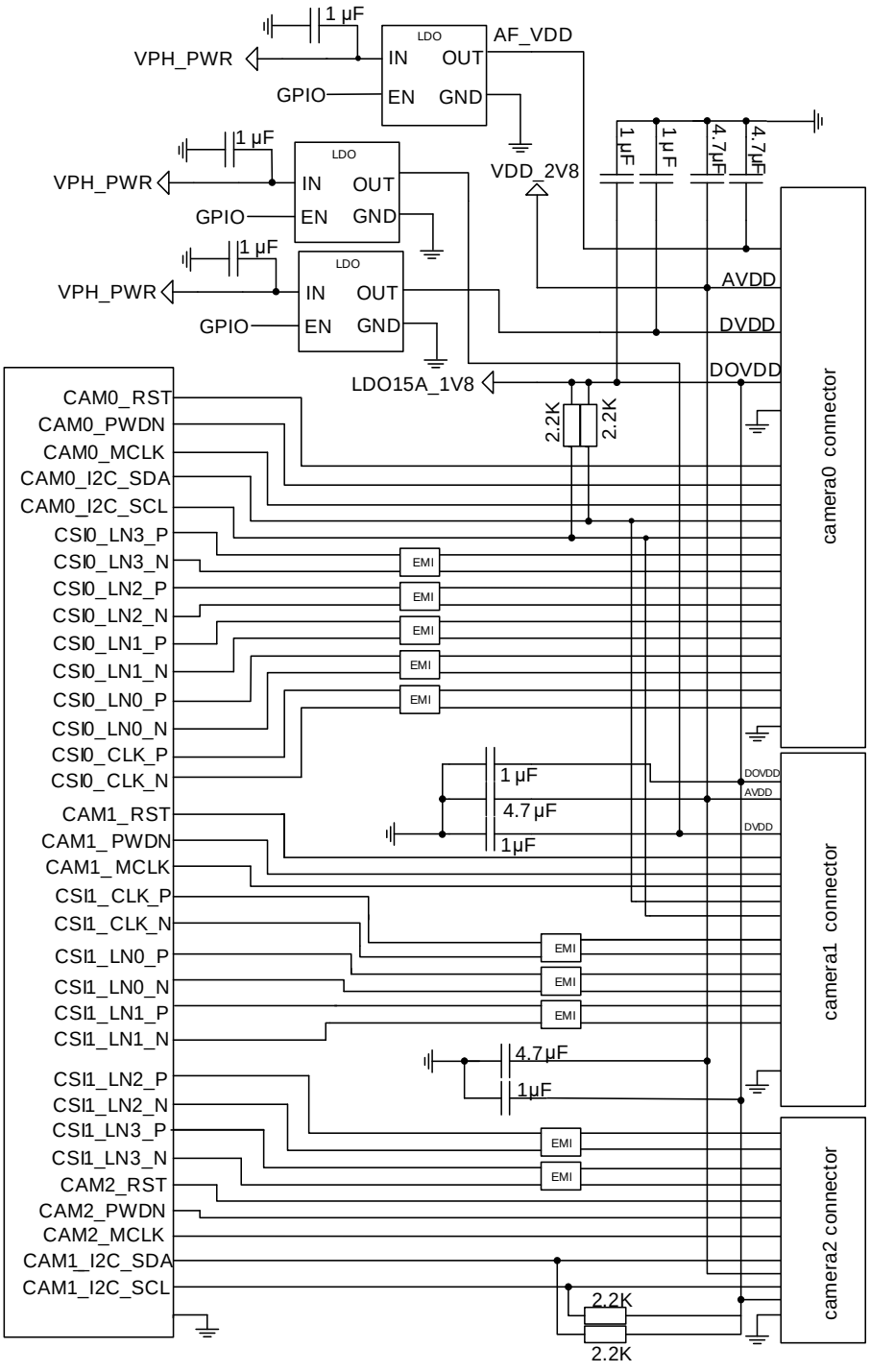


Figure 22: Reference Circuit Design for 3-Camera Applications

NOTE

In 3-camera applications, CSI1_LN3_P and CSI1_LN3_N are used as MIPI clock signals of camera 2. CSI1_LN2_P and CSI1_LN2_N are used as MIPI data signals of camera 2.

3.20.1. MIPI Design Considerations

- Special attention should be paid to the pin definition of LCM and camera connectors. Make sure the module and the connectors are correctly connected.
- MIPI lines are high-speed signal lines for DSI-supported maximum data rate of up to 1.5 Gbps and CSI-supported maximum data rate of up to 2.5 Gbps. The differential impedance should be controlled to 100 Ω. Additionally, it is recommended to route the trace on the inner layer of PCB, and do not cross it with other traces. For the same group of DSI or CSI signals, keep all the MIPI traces of the same length. In order to avoid crosstalk, keep a distance of 1.5 times the trace width among MIPI signal lines. During impedance matching, do not connect GND on different planes to ensure impedance consistency.
- It is recommended to select a low-capacitance TVS for ESD protection and the recommended parasitic capacitance should be below 1 pF.
- Route MIPI traces according to the following rules:
  a) The total trace length should not exceed 240 mm;
  b) Control the differential impedance to 100 Ω ± 10 %;
  c) Control intra-lane length difference within 0.7 mm;
  d) Control inter-lane length difference within 1.4 mm.

Table 24: MIPI Trace Length Inside the Module

Pin Name	Pin No.	Length (mm)	Length Difference (P - N)
DSI_CLK_N	52	38.53	0.23
DSI_CLK_P	53	38.30	
DSI_LN0_N	54	38.59	0.16
DSI_LN0_P	55	38.43	
DSI_LN1_N	56	38.22	-0.25
DSI_LN1_P	57	38.47	
DSI_LN2_N	58	38.84	0.28
DSI_LN2_P	59	38.56	
DSI_LN3_N	60	38.74	0.26
DSI_LN3_P	61	38.48	
CSI1_CLK_N	63	18.87	-0.03
CSI1_CLK_P	64	18.84	
CSI1_LN0_N	65	19.42	0.24

CSI1_LN0_P	66	19.18		
CSI1_LN1_N	67	19.02	-0.26	
CSI1_LN1_P	68	19.28		
CSI1_LN2_N	72	19.53	0.3	
CSI1_LN2_P	73	19.23		
CSI1_LN3_N	70	18.93	0.11	
CSI1_LN3_P	71	18.82		
CSI0_CLK_N	157	20.94	0.21	
CSI0_CLK_P	196	20.73		
CSI0_LN0_N	158	18.74	0.34	
CSI0_LN0_P	197	18.40		
CSI0_LN1_N	159	17.18	-0.19	
CSI0_LN1_P	198	17.37		
CSI0_LN2_N	160	8.28	0.13	
CSI0_LN2_P	199	8.15		
CSI0_LN3_N	161	4.97	0.27	
CSI0_LN3_P	200	4.70		

3.21. Sensor Interface

The module supports communication with sensors via I2C interfaces, and it supports ALS/PS, BDS, accelerometer, gyroscope, etc.

Table 25: Pin Definition of Sensor Interface

Pin Name	Pin No.	I/O	Description	Comment
SENSOR_I2C_SCL	91	OD	I2C clock for external sensor	Need to be pulled up to 1.8 V externally.
SENSOR_I2C_SDA	92	OD	I2C data for external sensor	Can only be used to connect sensor devices.

3.22. Audio Interfaces

The module provides three analog input channels and three analog output channels. The following table shows the pin definition.

Table 26: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC_BIAS1	147	PO	Bias voltage 1 output for microphone	The rated output current is 3 mA.
MIC1_P	4	AI	Microphone input for channel 1 (+)	-
MIC1_M	5	AI	Microphone input for channel 1 (-)	-
MIC2_P	6	AI	Microphone input for headset (+)	-
MIC3_P	148	AI	Microphone input for channel 3 (+)	-
MIC3_M	149	AI	Microphone input for channel 3 (-)	-
MIC_BIAS3	155	PO	Bias voltage 3 output for microphone	The rated output current is 3 mA. The output voltage is fixed to 1.8 V and cannot be adjusted.
EAR_P	8	AO	Earpiece output (+)	-
EAR_M	9	AO	Earpiece output (-)	-
LINEOUT_P	10	AO	Audio line differential output (+)	The typical output voltage is 2 Vrms.
LINEOUT_M	11	AO	Audio line differential output (-)	-
HPH_R	136	AO	Headphone right channel output	-
HPH_GND	137	AO	Headphone reference ground	-
HPH_L	138	AO	Headphone left channel output	-
HS_DET	139	AI	Headset hot-plug detect	High level by default.

- The module offers three audio input channels.
- The output voltage range of MIC_BIAS1 is programmable between 1.6 V and 2.85 V, and the maximum output current is 3 mA. MIC_BIAS3 supports 1.8 V pull-up output only and is not programmable.
- The earpiece interface uses differential output.

- The lineout interface uses differential output, lineout is used as audio PA input.
- The headphone interface features stereo left and right channel output, and supports headphone insertion detection.

3.22.1. Reference Circuit Design for Microphone Interfaces

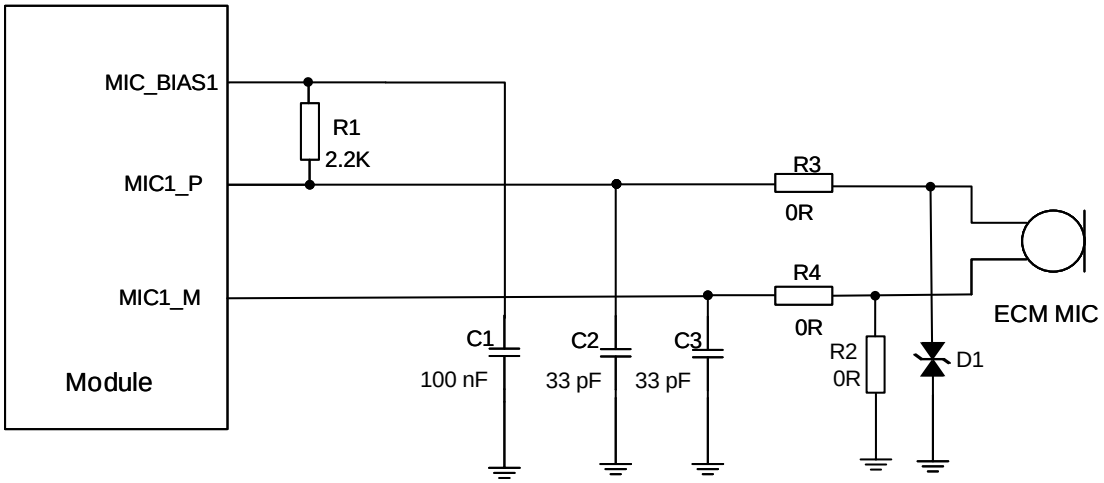


Figure 23: Reference Circuit Design for ECM Microphone Interface

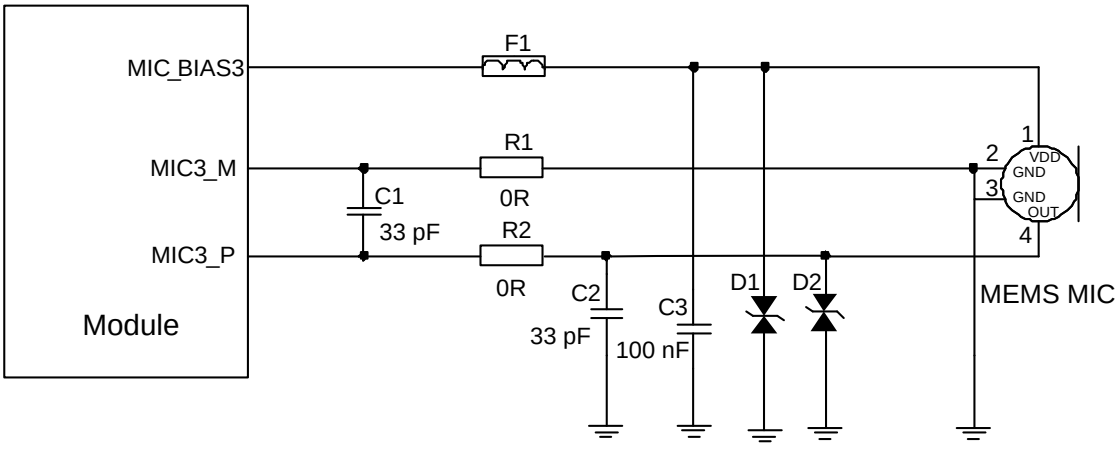


Figure 24: Reference Circuit Design for MEMS Microphone Interface

3.22.2. Reference Circuit Design for Earpiece Interface

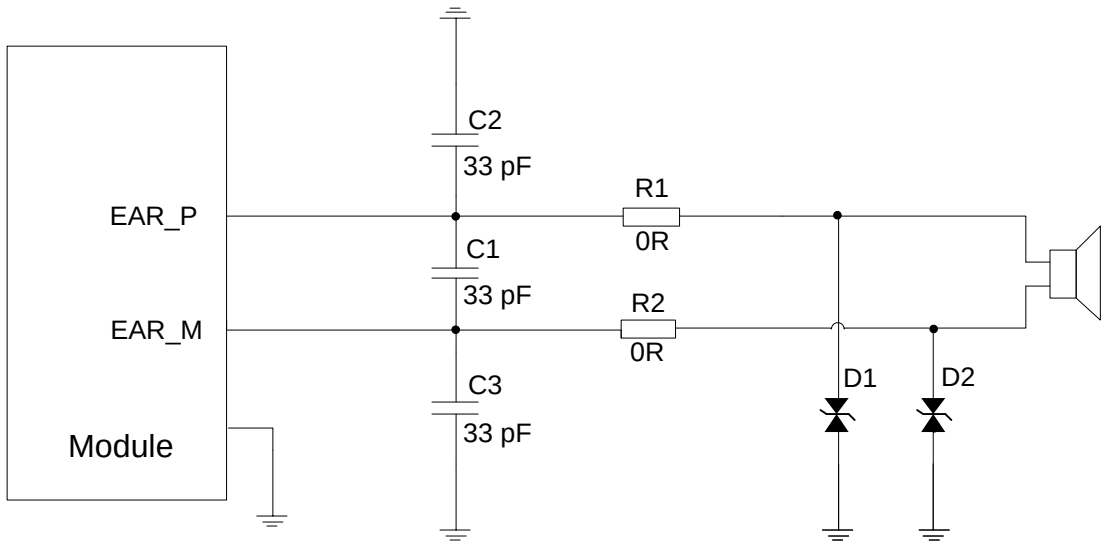


Figure 25: Reference Circuit Design for Earpiece Interface

3.22.3. Reference Circuit Design for Headset Interface

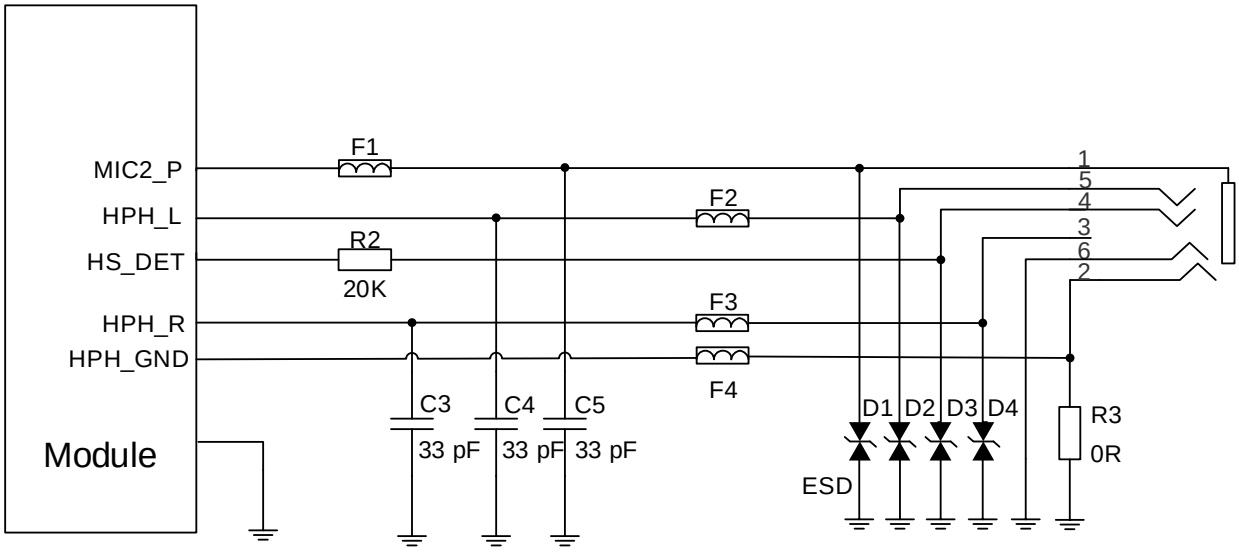


Figure 26: Reference Circuit Design for Headset Interface

3.22.4. Reference Circuit Design for Lineout Interface

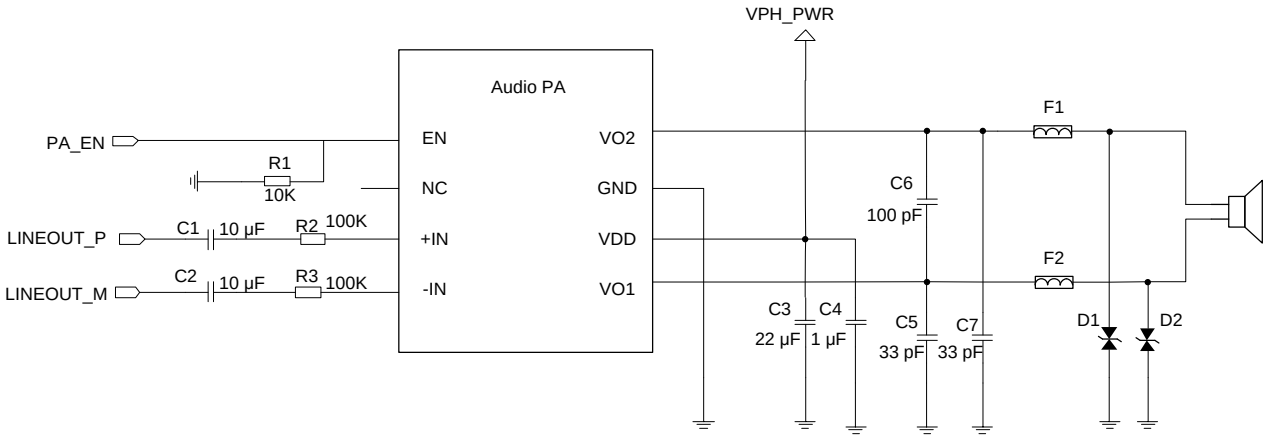


Figure 27: Reference Circuit Design for Lineout Interface

3.22.5. Audio Signal Design Considerations

It is recommended to use the ECM microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied to filter out RF interference when the module is transmitting at EGSM900. The 10 pF capacitor is used to filter out RF interference at DCS1800. Without this capacitor, TDD noise could be heard during voice calls. Please note that the resonant frequency point of a capacitor largely depends on its material and manufacturing technique. Therefore, you should consult the capacitor vendors to choose the most suitable capacitor to filter out the high-frequency noises.

The severity of RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, you should select a suitable capacitor according to the test results. Sometimes, even no RF filtering capacitor is required.

In order to decrease radio or other signal interference, place RF antennas away from audio interfaces and audio traces. Additionally, keep power traces far away from the audio traces and do not route them in parallel.

Route the differential audio traces according to the differential signal layout rule.

3.23. USB_BOOT

USB_BOOT is an emergency download interface. You can force the module to enter emergency download mode by pulling it up to LDO15A_1V8 when the module is turning on. This is an emergency option when failures such as abnormal start-up or running occur. For firmware upgrade and debugging in the future, reserve the following reference design.

Table 27: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	46	DI	Force the module into emergency download mode	Force the module to enter emergency download mode by pulling this pin up to LDO15A_1V8 when the module is turning on.

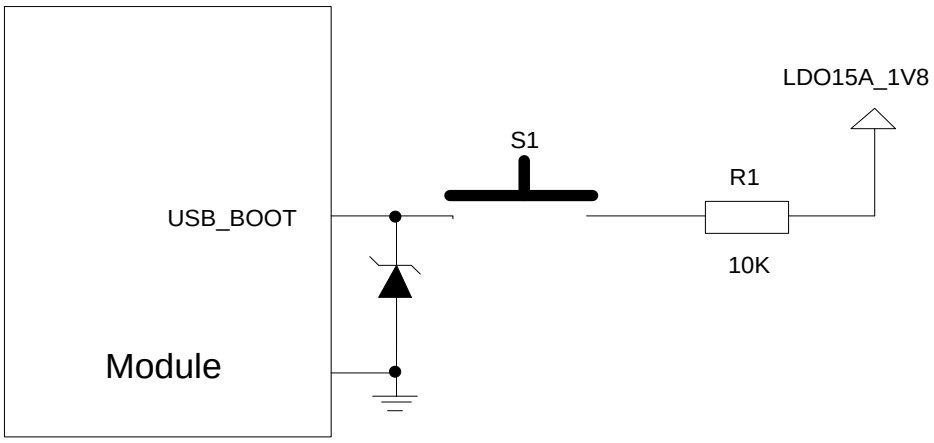


Figure 28: Reference Circuit Design for Emergency Download Interface

4 Wi-Fi/Bluetooth

The module provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth functions. The interface impedance should be controlled to 50 Ω. You can connect external antennas such as PCB antenna, sucker antenna, and ceramic antenna to the module via the interface to achieve Wi-Fi and Bluetooth functions. Bluetooth and WLAN (both 5G and 2.4 G) are operating in TDD under coex mode.

4.1. Wi-Fi

The module supports 2.4 GHz and 5 GHz dual-band WLAN based on IEEE 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 150 Mbps in 2.4 GHz bands, and 433 Mbps in 5 GHz bands. The features are as below:

- Supports Wake-on-WLAN (WoWLAN)
- Supports ad hoc mode
- Supports WAPI SMS4 hardware encryption
- Supports AP and STA mode
- Supports Wi-Fi Direct
- Supports MCS 0–7 for HT20 and HT40
- Supports MCS 0–8 for VHT20
- Supports MCS 0–9 for VHT40 and VHT80

4.2. Bluetooth

The module supports Bluetooth 5.0 (BR/EDR + BLE) specification, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally supports up to 7 wireless connections.
- Maximally supports up to 3.5 piconets at the same time.
- Support one SCO or eSCO connection.

5 GNSS

The module integrates a IZat™ GNSS engine (GEN 8C) which supports multiple positioning and navigation systems including GPS, GLONASS, Galileo, BDS, QZSS, SBAS and NavIC [5]. With an embedded LNA, the positioning accuracy of the module has been significantly improved.

5.1. GNSS Performance

The following table lists the GNSS performance of the module in conduction mode.

Table 32: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity	Acquisition	-147	dBm
	Reacquisition	-159	dBm
	Tracking	-159	dBm
TTFF	Cold start	31.2	s
	Warm start	24.7	s
	Hot start	1.32	s
Accuracy	CEP-50	1.95	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2. GNSS RF Design Guidelines

Bad design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. In order to avoid this, follow the reference design rules as below:

- Maximize the distance between the GNSS RF part and the GPRS RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, place GNSS RF signal lines and RF components far away from high-speed circuits, switch-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with harsh electromagnetic environment or high ESD-protection requirements, it is recommended to add ESD protective diodes for the antenna interface. The junction capacitance of the diodes should be less than 0.5 pF. Otherwise, it will influence the impedance characteristic of RF circuit loop, or cause attenuation of bypass RF signals.
- Control the impedance of feeder lines and PCB traces to 50 Ω, and keep the trace as short as possible.

6 Antenna Interfaces

SC200E-CE/EM/NA provides four antenna interfaces for the main, Rx-diversity, Wi-Fi/Bluetooth, and GNSS antennas respectively, while SC200E-WF provides one antenna interface for Wi-Fi/Bluetooth antenna only. The impedance of the antenna ports should be controlled to 50 Ω.

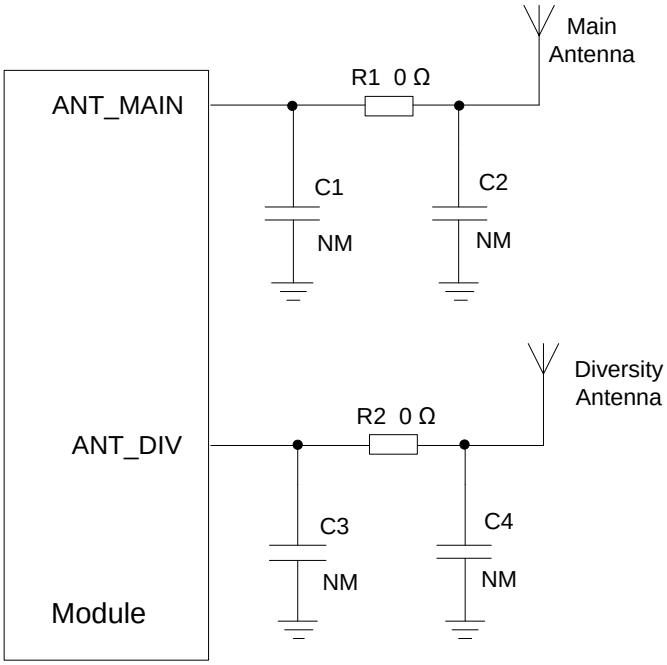
6.1. Main Antenna and Rx-diversity Antenna Interfaces

Pin Definition of Main/Rx -diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	87	AIO	Main antenna interface	50 Ω impedance
ANT_DRX	131	AI	Diversity antenna interface	

6.1.1. Reference Design

A reference circuit design for the main and Rx-diversity antenna interfaces is shown below. Reserve a π-type matching circuit for each antenna to achieve better RF performance, and place the π-type matching components (R1/C1/C2 and R2/C3/C4) as close to the antennas as possible. The capacitors are not mounted by default and the resistors are 0 Ω.



Reference Circuit Design for Main and Rx-diversity Antenna Interfaces

6.2. Wi-Fi/Bluetooth Antenna Interface

The following tables show the pin definition and frequency specification of the Wi-Fi/Bluetooth antenna interface.

Pin Definition of Wi -Fi/Bluetooth Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	77	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω impedance

A reference circuit design for Wi-Fi/Bluetooth antenna interface is shown as below. C1 and C2 are not mounted by default and the resistor is 0 Ω.

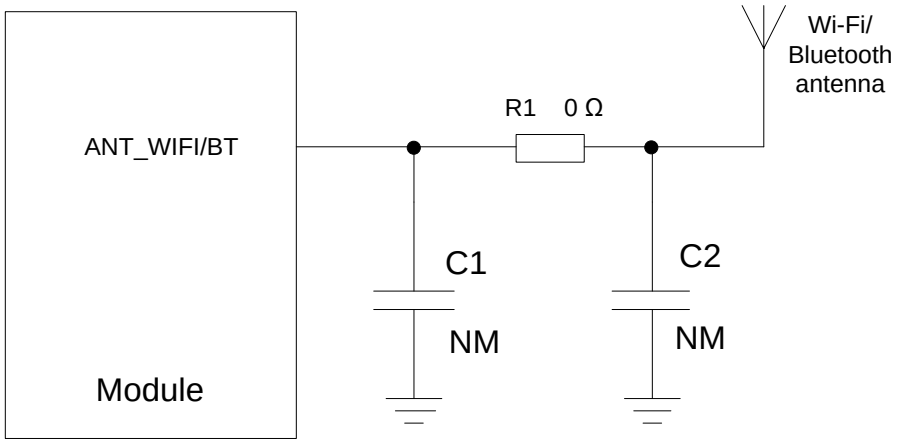


Figure 30: Reference Circuit Design for Wi-Fi/Bluetooth Antenna

6.3. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 39: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	121	AI	GNSS antenna interface	50 Ω impedance

6.3.1. Reference Circuit Design for Passive GNSS Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference circuit design is given below.

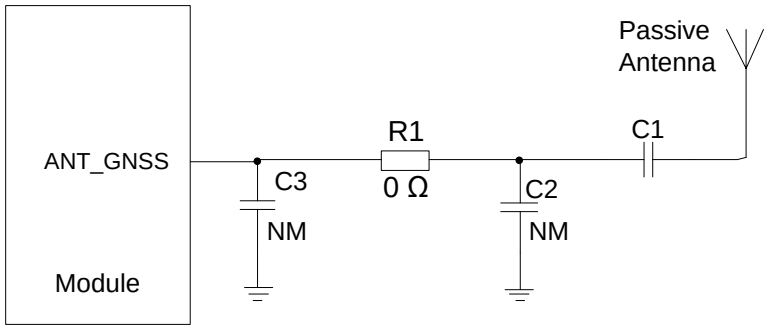


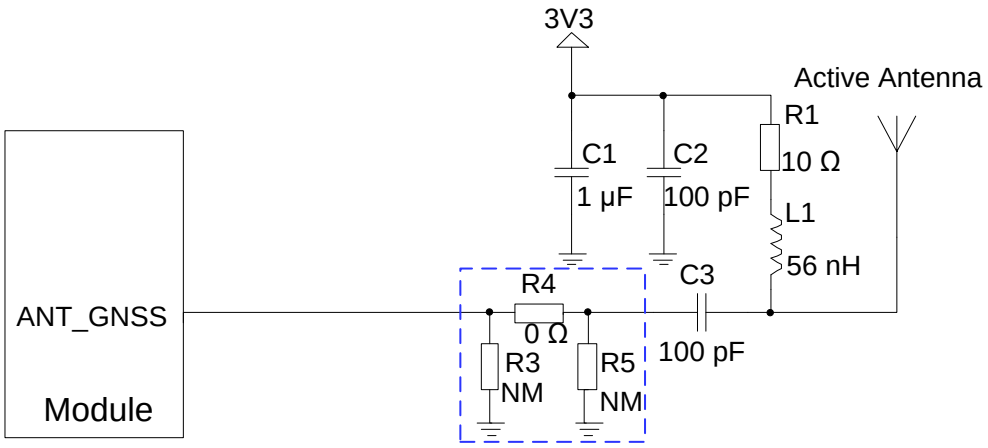
Figure 31: Reference Circuit Design for Passive GNSS Antenna

NOTE

It is not recommended to add an external LNA when using a passive GNSS antenna.

6.3.2. Reference Circuit Design for Active GNSS Antenna

The active antenna is powered by a 56 nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3 V to 5.0 V. Despite its low power consumption, the active antenna still requires stable and clean power supplies. Therefore, it is recommended to use high-performance LDO as the power supply. A reference design for active GNSS antenna is shown below.



Reference Circuit Design for Active GNSS Antenna

NOTE

It is recommended to use a passive antenna. If active antennas are required, it is strongly recommended to reserve a π-type attenuation and ensure that the total gain of the external GNSS RF path of the module is not greater than 0 dB. At the same time, this may compromise the GNSS performance, depending on the performance of the active antenna.

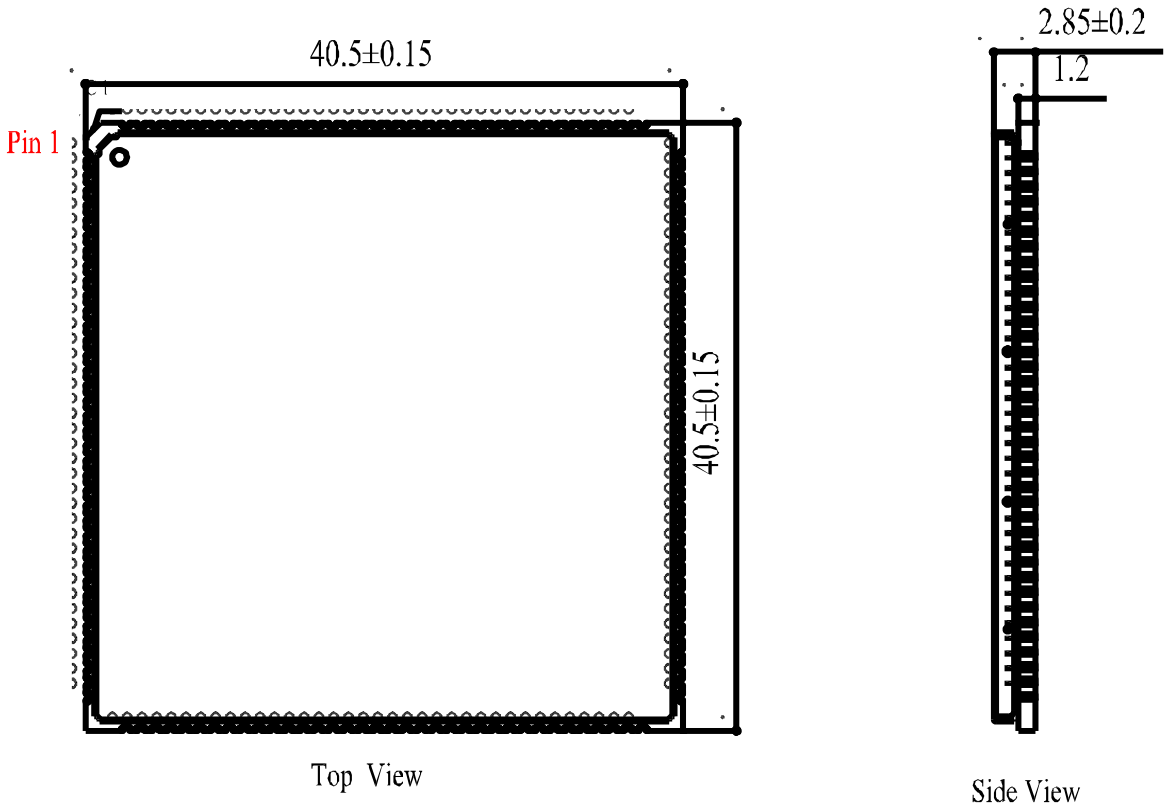
6.4. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions



Module Top and Side Dimensions