Theory of Operation/Technical Description

Term	Description
PCI Express*	**PCI-Express interface signals.** These signals are compatible with PCI Express 1.1 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
DMI	**Direct Media Interface signals.** These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
CMOS	**CMOS buffers.** 1.5 V tolerant.
COD	**CMOS Open Drain buffers.** 3.3 V tolerant.
HCSL	**Host Clock Signal Level buffers.** Current mode differential pair. Differential typical swing = (|D+ - D-|) * 2 = 1.4V. Single ended input tolerant from -0.35 V to 1.2 V. Typical crossing voltage 0.35 V.
HVCMOS	**High Voltage CMOS buffers.** 3.3 V tolerant.
HVIN	**High Voltage CMOS input-only buffers.** 3.3 V tolerant.
SSTL-1.8	**Stub Series Termination Logic.** These are 1.8 V output capable buffers. 1.8 V tolerant.
A	**Analog reference or output.** May be used as a threshold voltage or for buffer compensation.
GTL+	**Gunning Transceiver Logic signaling technology.** Implements a voltage level as defined by VTT of 1.2 V.