ElECTRIC CIRCUIT DESCRIPTION

1.FREQUENCY CONSTITUTION

The receiver utilizes double conversion. The first IF is 45.05MHz and the second IF is 455kHz. The first local oscillator signal is supplied from the PLL circuit.

The PLL circuit in the transmitter generates the necessary frequencies. Chart 1 shows the frequencies

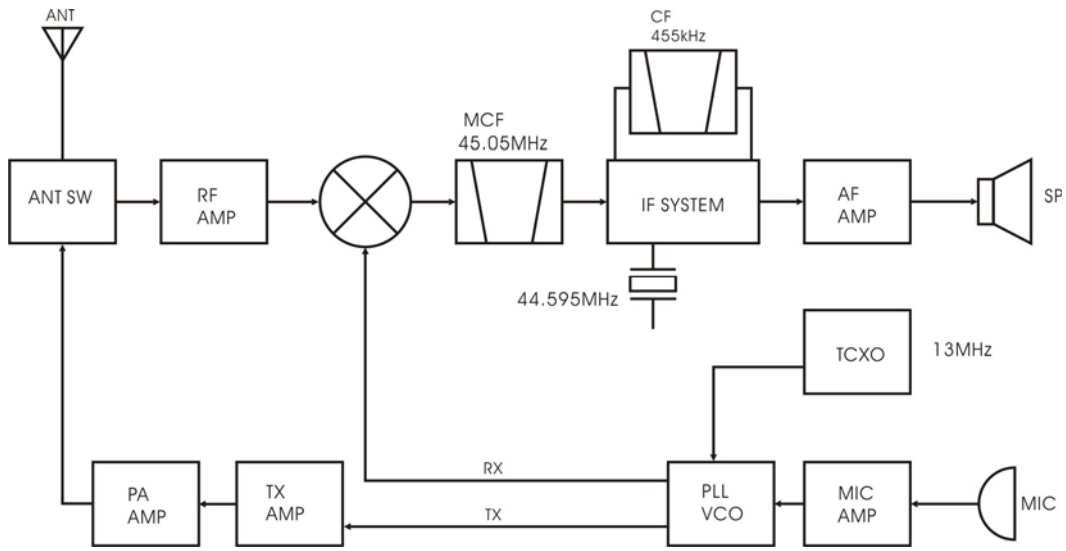

Chart 1 frequency constitution

2. RECEIVE PART

Chart 2 displaies the receive part constitution.

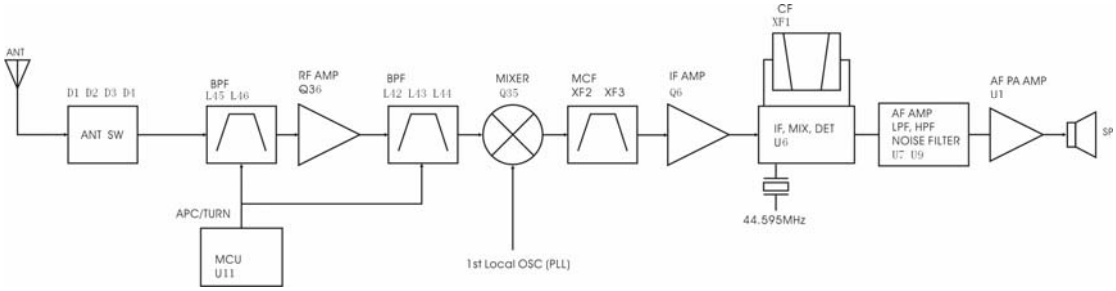

Chart 2 the receive part constitution

1) First level (radio frequency amplifier)

Comes from to the antenna signal after the launch receive& transformation diode circuit (D1, D2, D3, D4) to pass through BPF(L45, L46), and (Q35) is enlarged through the amplifier. Obtains thesignal after BPF (L42, L43, L44) and enters the mixer. These BPF is changed allows the diode (D21, D22, D23, D24, D25) to adjust,

enters changes accommodates the diode the input voltage the voltage regulation which (U11) outputs from the microprocessor chip.

2) First mixer

Comes first which produces in Q35 and in the phase-lock link electriccircuit to inspire the signal mixing from the front end signal and toproduce 45.05MHz the first intermediate frequency signal. Produces theintermediate frequency signal after the crystal filter (XF2, XF3)filters the neighbour clutter signal, guarantees neighbour selectivelyand so on the essential technical specification.

3) Intermediate frequency amplifier electric circuit

The first intermediate frequency signal after the crystal filter (XF2,XF3) filters the neighbour clutter signal. (Q6) is enlarged after thefilter first intermediate frequency signal by the first intermediatefrequency amplifier, then enters the intermediate frequency integratedcircuit chip (U6). The intermediate frequency integrated circuit chipprovides the second mixer, second inspires the signal, secondintermediate frequency amplifier, discriminator and RISS (receivesignal strength display).

The second mixer inspires with second the signal output (XF1) the44.595MHz mixing and produces the first intermediate frequency signal455KHz the second intermediate frequency signal. The secondintermediate frequency signal (XF1) filters the neighbour cluttersignal after the earthenware filter. Is enlarged after the filtersecond intermediate frequency signal through the second intermediatefrequency amplifier and (CD1) is demodulated through the earthenwarediscriminator, produces the tonic train signalling to the tonecircuit.

4) Audio frequency amplification circuit

Comes (U6) the signal which demodulates through chip U9 (3/4) toenlarge from the chip, through U9 (4/4) the low pass filter, U9 (1/4and 2/4) high passes the filter, U5 (3/4) high passes the filter andaggravates. Then the signal after noise filter U7, the audio frequencyvolume control (VR4), to the audioamplifier chip (U1), outputs thespeaker after the enlargement.

5） Squelch

Reenters the frequency modulation integrated circuit chip from afrequency modulation integrated circuit chip output tonic trainsignalling part (U6), and produces through the filter and theamplifier the noise enlargement and the rectification to correspond tothe noise component DC voltage. The direct current signal enters themicroprocessor chip (U11) simulation port, microprocessor chip throughcomparison input voltage whether is higher than or is lower thansupposes the value to control in advance whether closes or turns onthe speaker to output.Must turn on the speaker to output, the chip (U11) launches a highlevel signal to the speaker static sound pilot wire, and through Q19,Q24, Q11, Q9 and Q10 leads passes the chip (U1). (Sees also chart 3)

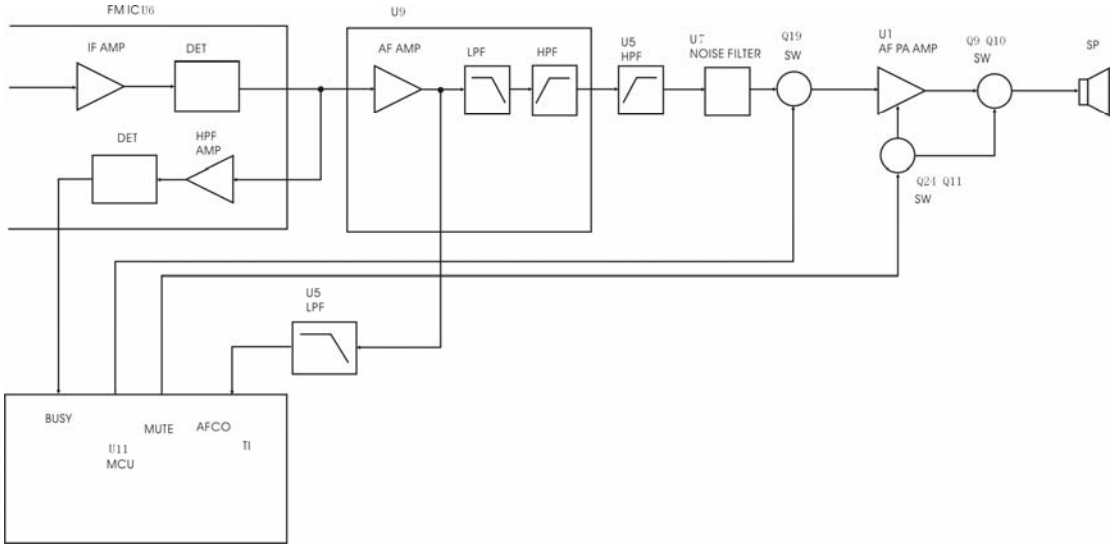

Chart 3 the audio amplifier and squelch circuit

6) QT&DQT

From the intermediate frequency integrated circuit chip output signal,above the 300Hz tonic train signalling (4/4 and 1/4) filters by lowpass filter U5, obtained signal input the microprocessor chip (U11),microprocessor chip according to internal each kind of processingjudgement receive QT or DQT whether with do suppose the value to beconsistent in advance, and acts according to calmly chirp suppressesthe electric circuit the judgement result control speaker static soundagreement speaker output sound.

3、Phase-lock link frequency synthesizer

The phase-lock link electric circuit produces receiver first thelaunch intelligence signal which inspires the signal and uses in tolaunch.

1）Phase-lock link electric circuit

The phase-lock link electric circuit cloth enters the frequency is 5 or 6.25KHz. The 13MHz reference oscillation signal is produced througha mix counter in chip U3 by the frequency division 5 or the 6.25KHz reference frequency. The pressure controls the signal which theoscillator (VCO) outputs, enlarges through the Q2 cushion, then inchip U3 by double modules programmable counter frequency division. Has 5 or 6.25KHz by the frequency division signal in reference signal phase comparator chip U3 is compared the signal which outputs after thephase comparator to enter a low pass filter, controls the oscillator through the voltage control pressure (VCO) the output frequency. (Sees also chart 4)

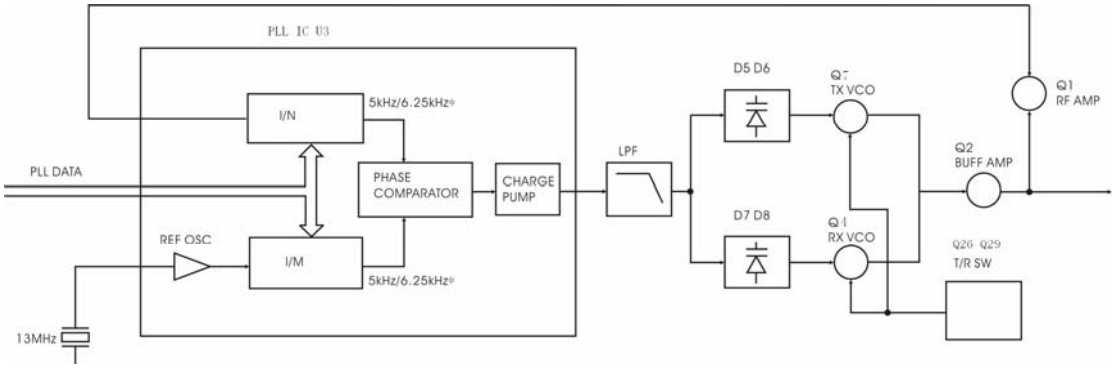

Chart 5 phase-lock link electric circuit

2） VCO

Has the operating frequency in the launch pattern through Q7, has theoperating frequency in the receive pattern through Q4. The controlsignal to changes through the phase comparator accommodates the diode(in launch pattern is D5 and D6, in receive pattern is D7 and D8),uses the pressure to control the oscillator control voltage to controlthe output frequency. In receive pattern, because Q26 and Q29 shut offQ7 and to lead passes Q4, therefore the reflection/receives the basepin to establish as the high level. In the transmit mode, transmit&receive base pin establish for the low level, Q7 and the Q4 output through the Q2 enlargement and transmit to the buffer amplifier.

3）Lose lock detector

If on the chip U3 LD base pin appears the high level, then producesloses locks the condition, and produces the DC voltage also C115produces provides the microprocessor UL base pin stepping down ofvoltage. When the microprocessor examination reaches this point thesituation, cannot carry on the launch, disregards the telephoneconversation change-over switch input signal.

4、Transmit part system

1）Transmitter amplifier

Comes from (1/2) to enlarge to the microphone modulation signal afterchip U2, and through a preemphasis circuit and another amplifier U2 (2/2) therestriction, the signal (Q20 and Q21) filters above 3KHz after the lowpass filter the frequency, the signal passes through the greatestfrequency to adjust, and enters the VCO modulation input.

2）QT/DQT code

The QT/DQT data outputs from the chip U11 TO base pin, signal afterlow pass filter filter, and delivers TCXO (X1) the balance adjustment, then with the tonic train signalling mix, inputs to VCO carries on themodulation. (Sees also chart 5)

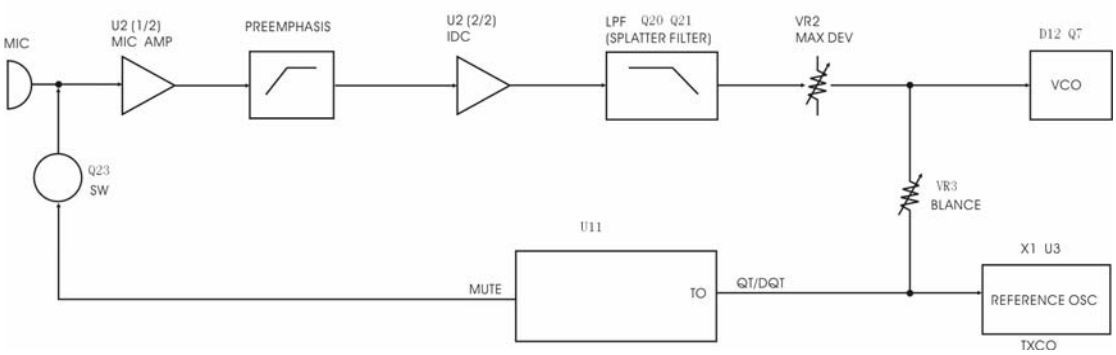

Chart 5 transmitter amplifier

3）Drive and Final Amplifier

Comes from (D9 leads to the T/R switch passes) the signal through thepretage actuation amplifier (Q8 and Q12) and the actuation amplifier(Q13) enlarges 500mW. Actuates the amplifier the output (Q14) toenlarge by the RF power amplifier to 3W (works as when low power is1W). The RF power amplifier constitutes by 2 MOSFET. The RF poweramplifier output (LPF) and the antenna switch (D1 and D2 leads throughthe harmonic filter passes) and delivers the antenna terminal. (Seesalso chart 6)

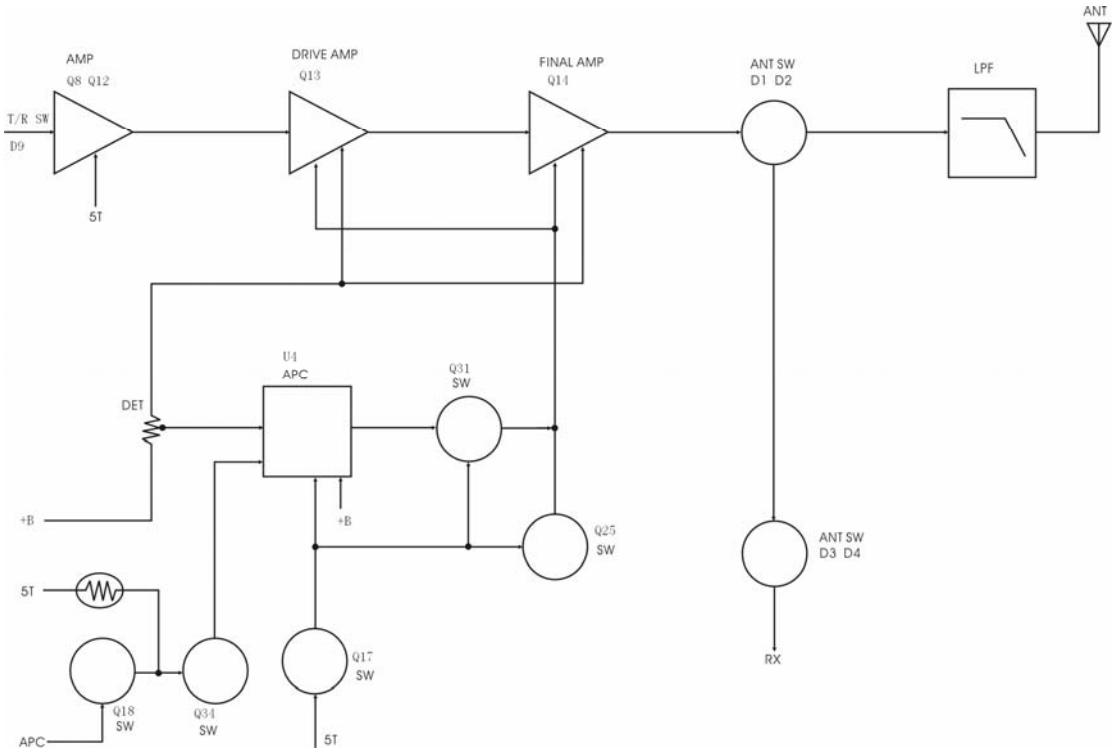

Chart 6 drive, final amplifier and APC circuit

4) Automatic power control (APC) electric circuit

The APC electric circuit continuously monitors through the RF poweramplifier (Q14) electric current and maintenance electric currentstability. Can cause R233, R234 and R235 stepping down of voltageafter the RF power amplifier electric current change, this voltagedelivers differential amplifier U4 (1/2), U4 (2/2) U4 (1/2) the outputvoltage with comes carries on the comparison from the chip U11reference voltage, U4 (2/2) the output voltage to control the RF poweramplifier, actuates the amplifier, actuates the amplifier in advanceVG, causes the voltage maintenance to be consistent. The powerhigh/low change is realizes through the change reference voltage.

5、Power source

The transceiver provides with 4 pieces of 5V power source to the microprocessor:+5V, 5C, 5R, and 5T. When the power source puts through, +5V continuously maintains the output, but when closes the power source also is switched off, prevented the microprocessor appears the break down. 5C is public 5V, when non- province electricity condition maintainsthe output. 5R is 5V which for receive, in receptive period maintenance output. 5T is 5V which the transmit uses, in start-up period maintenance output.