CIRCUIT DESCRIPTION

1. Frequency configuration

The receiver utilizes double conversion. The first IF is 45.05MHz and the second IF is 455kHz. The first local oscillator signal is supplied from the PLL circuit.

The PLL circuit in the transmitter generates the necessary frequencies. Fig. 1 shows the frequencies

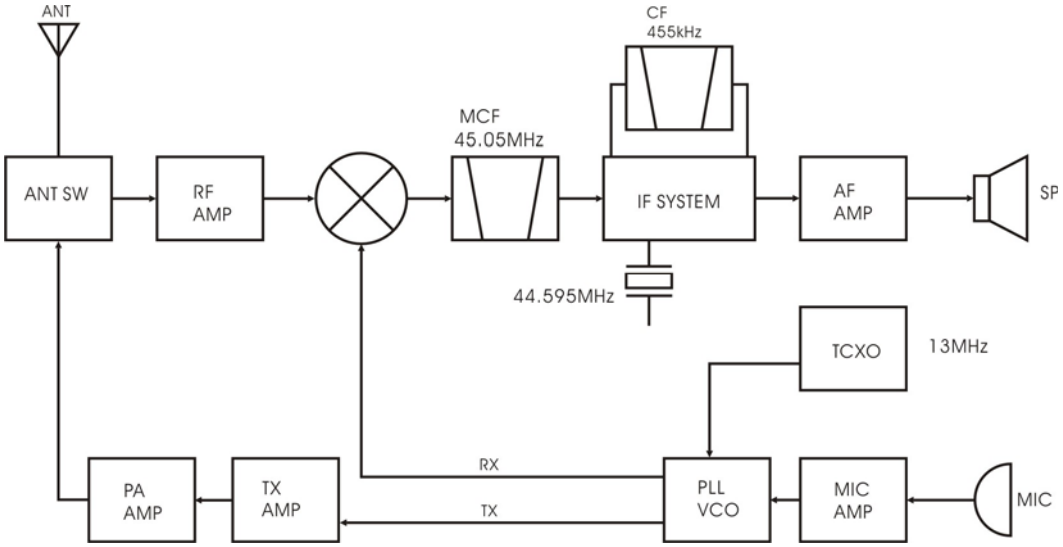

Fig. 1 Frequency configuration

2. Receiver

The receiver is double conversion superheterodyne, designed to operate in the frequency range of 430 to 470MHz.

The frequency configuration is shown in Fig. 1.

1) Front-end RF amplifier

The signal coming from the antenna passed through the transmit/receive switching diode circuit, (D1, D2, D3 and D4), passed through a BPF (L44 and L45), and is amplified by the RF amplifier (Q34).

The resulting signal passed through a BPF (L41, L42 and L43) and goes to the mixer. These BPFs are adjusted by variable capacitors (D13, D14, D15, D16 and D17). The input voltage to the variable capacitor is regulated by voltage output from the microprocessor (U9). (See Fig.2)

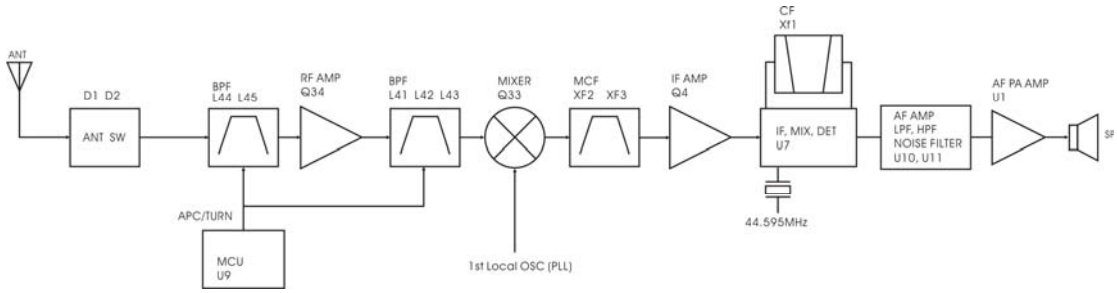

Fig. 2 Receiver section configuration

2) First Mixer

The signal from the front-end is mixed with the first local oscillator signal generated in the PLL circuit by Q33 to produce a first IF frequency of 45.05MHz.

The resulting signal passed through the MCF (XF2 and XF2) to cut the adjacent spurious and provide the optimum characteristics, such as adjacent frequency selectivity.

3) IF Amplifier Circuit

The first IF signal is passed through a four-pole crystal filter (XF2 and XF3) to remove the adjacent channel signal. The filtered first IF signal is amplified by the first IF amplifier (Q4) and then applied to the IF system IC (U7). The IF system IC provides a second mixer, second local oscillator, limiting amplifier and quadrature detector. The second mixer mixes the first IF signal with the 45.05MHz of the second local oscillator (44.595MHz) and produces the second IF signal of 455kHz.

The second IF signal is passed through the ceramic filter (XF1) to remove the adjacent channel signal. The filtered second IF signal is amplified by the limiting amplifier and demodulated by the quadrature detector with the ceramic discriminator (CD1).The demodulated signal is routed to the audio circuit.

4) Audio Amplifier Circuit

The demodulated signal form U7 is amplified by U10 (1/4), low-pass filtered by U10 (2/4), high-pass filtered by U10 (3/4 and 4/4), high-pass filtered by U5 (4/4), and de-emphasized.

The signal then goes through an noise filter U11,an AF volume control (VR1), and is routed to an audio power amplifier (U1) where it is amplified and output to the speaker.

5) Squelch

Part of the AF signal from the IC enters the FM IC (U7) again, and the noise component is amplified and rectified by a filter and an amplifier to produce a DC voltage corresponding to the noise level.

The DC signal from the FM IC goes to the analog port of the microprocessor U9. U9 determines whether to output sounds from the speaker by checking wheter the input voltage is higher or lower than the preset value.

To output sounds from the speaker, U9 sends a high signal to the MUTE and AFCO lines and turns U1 on through Q30, Q17, Q7, Q21, Q43 and Q44. (See Fig. 3)

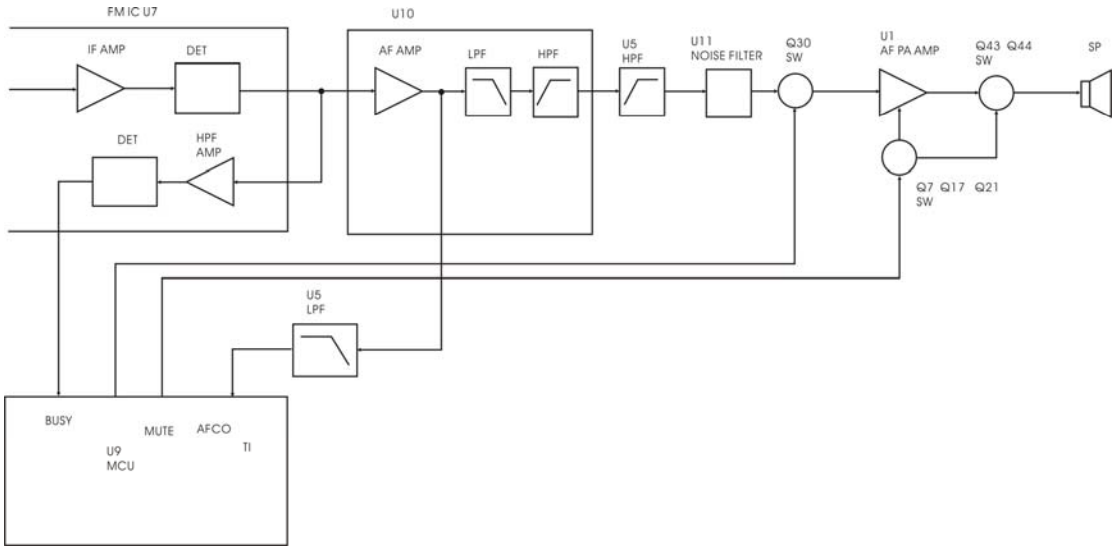

Fig. 3 AF Amplifier and squelch

6) Receive Signalling (QT/DQT)

300Hz and higher audio frequencies of the output signal from IF IC are cut by a low-pass filter U5 (1/4 and 2/4). The resulting signal enters the microprocessor (U9). U9 determines whether the QT or DQT matches the preset value, and controls the MUTE and AFCO and the speaker output sounds according to the squelch results.

3. PLL frequency synthesizer

The PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission.

1) PLL

The frequency step of the PLL circuit is 5 or 6.25kHz. A 13MHz reference oscillator signal is divided at U3 by a fixed counter to produce the 5 of 6.25kHz reference frequency. The voltage controlled oscillator (VCO) output signal is buffer amplified by Q2,then divided in U3 by a dual-module programmable counter. The divided signal is compared in phase with the 5 of 6.25kHz reference signal in the phase comparator in U3. The output signal from the phase comparator is filtered through a low-pass filter and passé to the VCO to control the oscillator frequency.

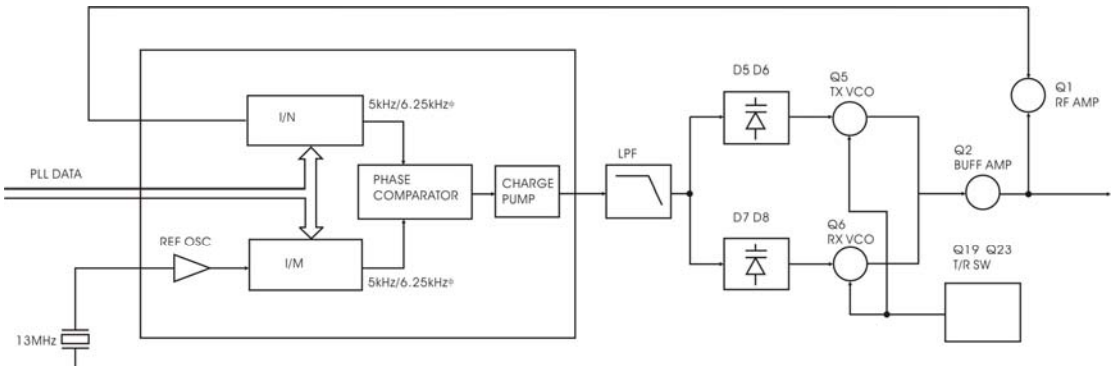

Fig. 4 PLL circuit

2) VCO

The operating frequency is generated by Q5 in transmit mode and Q6 in receive mode. The oscillator frequency is controlled by applying the VCO control voltage, obtained from the phase comparator, to the varactor diodes (D5 and D6 in transmit mode and D7and D8 in receive mode). The T/R pin is set high in transmit mode causing Q19 and Q23 to turn Q6 off, and turn Q5 on. The T/R pin is set low in receive mode. The outputs from Q5 and Q6 are amplified by Q2 and sent to the buffer amplifiers.

3) Unlock Detector

If a pulse signal appears at the LD pin of U3, an unlock condition occurs, and the DC voltage obtained from U3 cause the voltage applied to the microprocessor to go low. When the microprocessor detects this condition, the transmitter is disabled, ignoring the push-to-talk switch input signal.

4. Transmitter

1) Microphone Amplifier

The modulation signal from the microphone is amplified by U2 (1/2),passed through a preemphasis circuit, and amplified by the other U2 (2/2) to perform IDC operation. The signal then passed through a low-pass filter (splatter filter) (Q13 and Q14) and cuts 3kHz and higher frequencies. The resulting signal goes to the VCO through the VCO modulation terminal for direct FM modulation. (See Fig. 5)

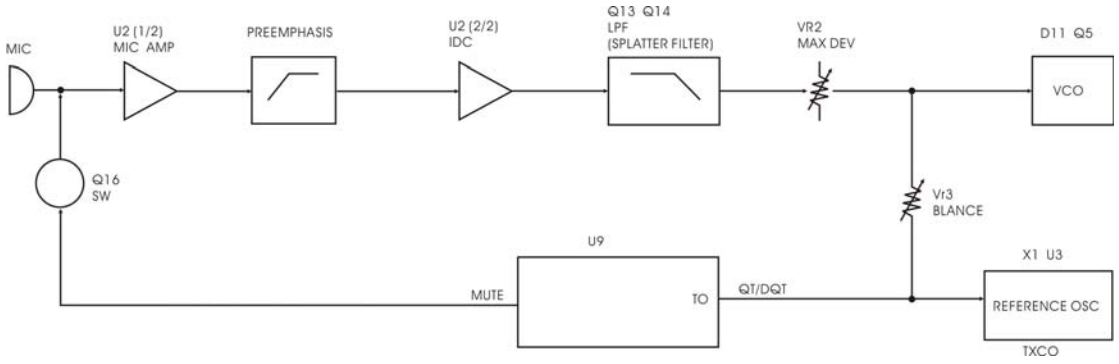

Fig. 5 Transmit audio QT/DQT

2) QT/DQT encoder

A necessary signal for QT/DQT encoding is generated by U9 and FM-modulated to the PLL reference signal. Since the reference OSC does not modulate the loop characteristic frequency of higher, modulation is performed at the VCO side by adjusting the balance.

3) Drive and Final Amplifier

The signal form the T/R switch (D101 is on) is amplified by the pre-drive (Q12 and Q9) and drive amplifier (Q10) to 500mW. The output of the drive amplifier is amplified by the RF power

amplifier (Q11) to 3.13W. The RF power amplifier consists of two
MOS FET stages. The output of the RF power amplifier is then passed through the harmonic filter (LPF) and antenna switch (D1 and D2) and applied to the antenna terminal. (See Fig. 6)

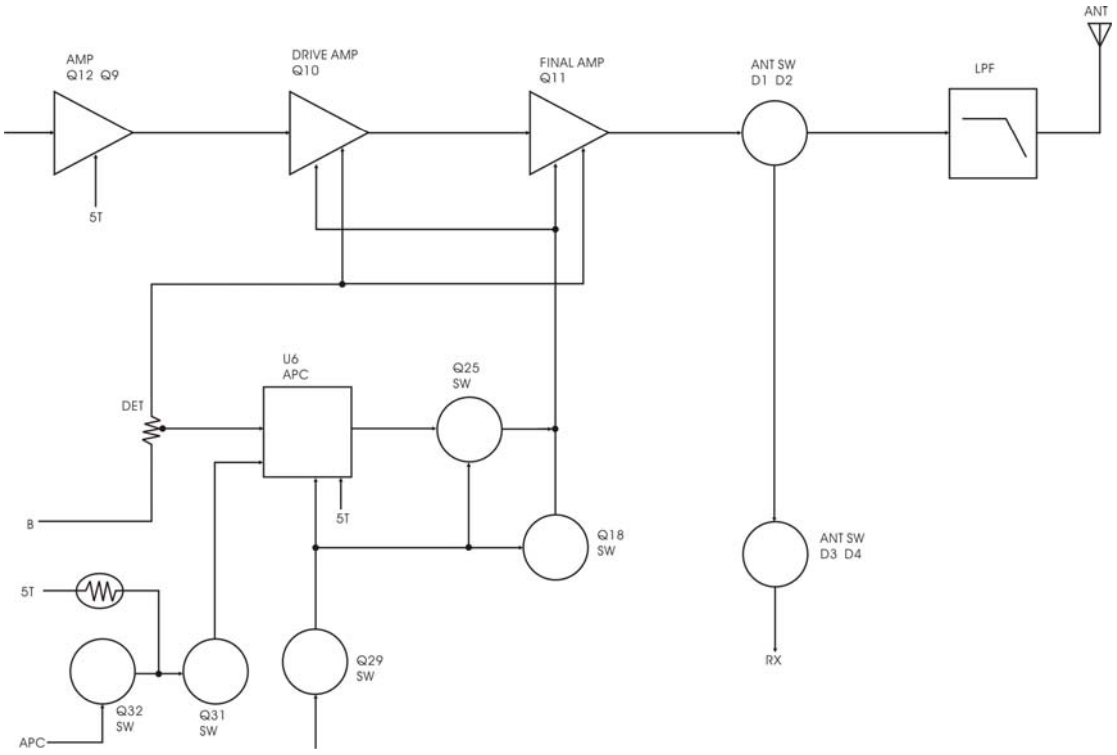

Fig. 6 APC system

4) APC Circuit

The APC circuit always monitors the current flowing through the RF power amplifier (Q11) and keeps a constant current. The voltage drop at R203, R204 and R205 is caused by the current flowing through the RF power amplifier and this voltage is applied to the differential amplifier U6 (1/2). U6 (2/2) compares the output voltage of U6 (1/2) with the reference voltage from U9. The output of U6 (2/2) controls the VG of the RF power amplifier, Drive amplifier and Pre-Drive amplifier to make both voltages the same. The change of power high/low is carried out by the change of the reference voltage.

5. Power Supply

There are four 5V power supplies for the microprocessor: +5V, 5C, 5R, and 5T. +5V for microprocessor is always output while the power is on. +5V is always output, but turns off when the power is turned off to prevent malfunction of the microprocessor.

5C is a common 5V and is output when SAVE is not set to OFF.

5R is 5V for reception and output during reception.

5T is 5V for transmission and output during transmission.