CIRCUIT DESCRIPTION

1. Frequency configuration

The receiver utilizes double conversion. The first IF is 38.85MHz and the second IF is 450kHz.The first local oscillator signal is supplied from the PLL circuit.

The PLL circuit in the transmitter generates the necessary frequencies. Fig.1 shows the frequencies.

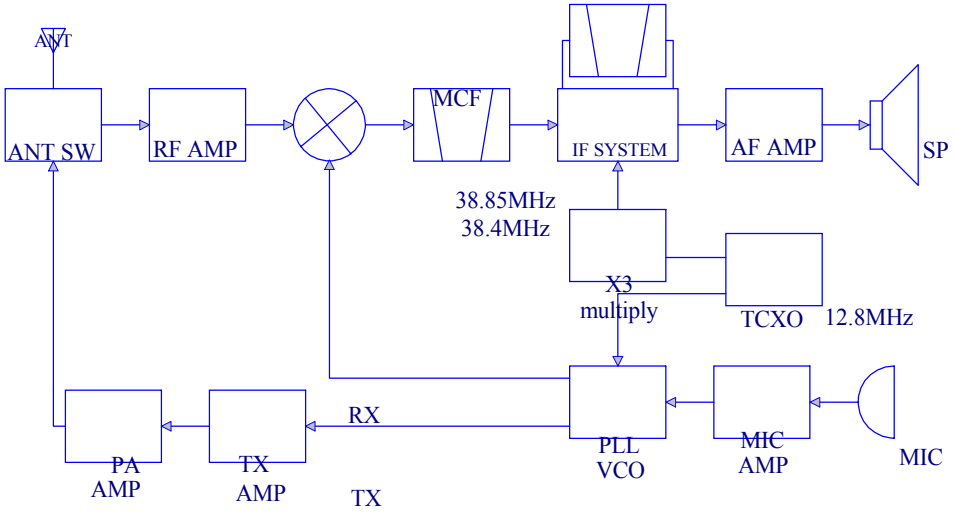

Fig. 1 Frequency configuration

2. Receiver

The receiver is double conversion superheterodyne, designed to operate in the frequency range of 400 to 470MHz (F6U) The frequency configuration is shown in Fig.1.

①. Front-end RF amplifier

An incoming signal from the antenna is applied to an RF amplifier (Q203) after passing through a transmit/receive switch circuit (D102 an D103 are off) and a 3-pole LC filter. After the signal is amplified (Q203),the signal is filtered by a band pass filter (a 3-pole LC filter) to eliminate unwanted signals before it is passed to the first mixer.

The voltage of these diode are controlled by to track the MPU

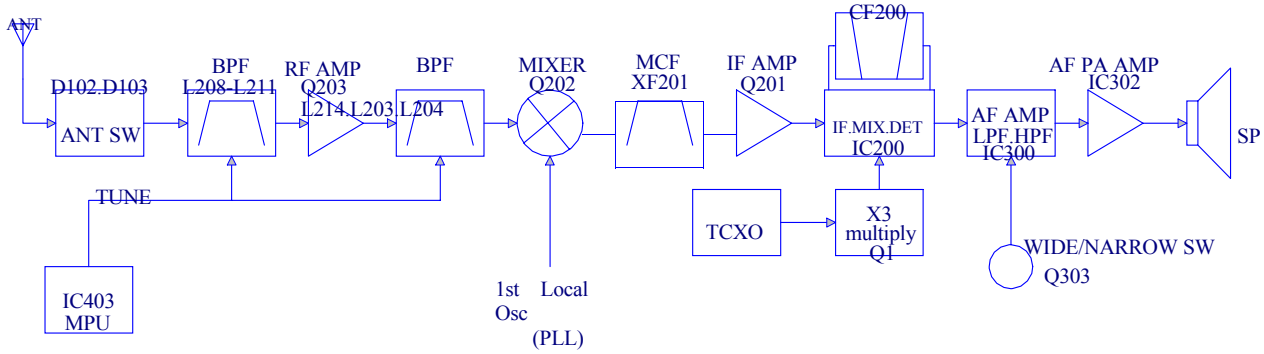

Fig.2 Receiver n configuration

②. First Mixer

The signal from the RF amplifier is heterodyned with the first local oscillator signal from the PLL frequency synthesizer circuit at the first mixer (Q202) to create a 38.85MHz first then fed through two monolithic crystal filters (MCFs:XF1 and XF2) to further remove spurious signals.

③. IF amplifier

The first IF signal is amplified by Q201,and then enters IC200 (FM processing IC).The signal is heterodyned again 450kHz second IF signal. The second IF signal is then fed through a 450kHz ceramic filter (CF200) to further eliminate unwanted signals before it is amplified and FM detected in IC200.

④. AF amplifier

The recovered AF signal obtained from IC200 is amplified by IC300 (1/4) ,Filtered by the IC300 low-pass filter (2/4) and IC300 high-pass filter (3/4) and (4/4),and de-emphasized by R303 and C306.The AF signal is then passed through a Wide/Narrow switch (Q303). The processed AF signal passes through an AF volume control and is amplified to a sufficient level to drive a loud speaker by an AF power amplifier (IC302).

⑤. Squelch

Part of the AF signal from the IC enters the FM IC again, and the nose component is amplified and rectified by a filter and an amplifier to produce a DC voltage corresponding to the noise level.

The DC signal from the FM IC goes to the analog port of the microprocessor (IC101).IC101 determines whether to output sounds from the speaker by checking whether the input voltage is higher or lower than the preset value.

To output sounds from the speaker,IC101 sends a high signal to the MUTE and AFCO lines and turns IC302 on through Q403,Q304,Q10 and Q9.(See Fig.3)

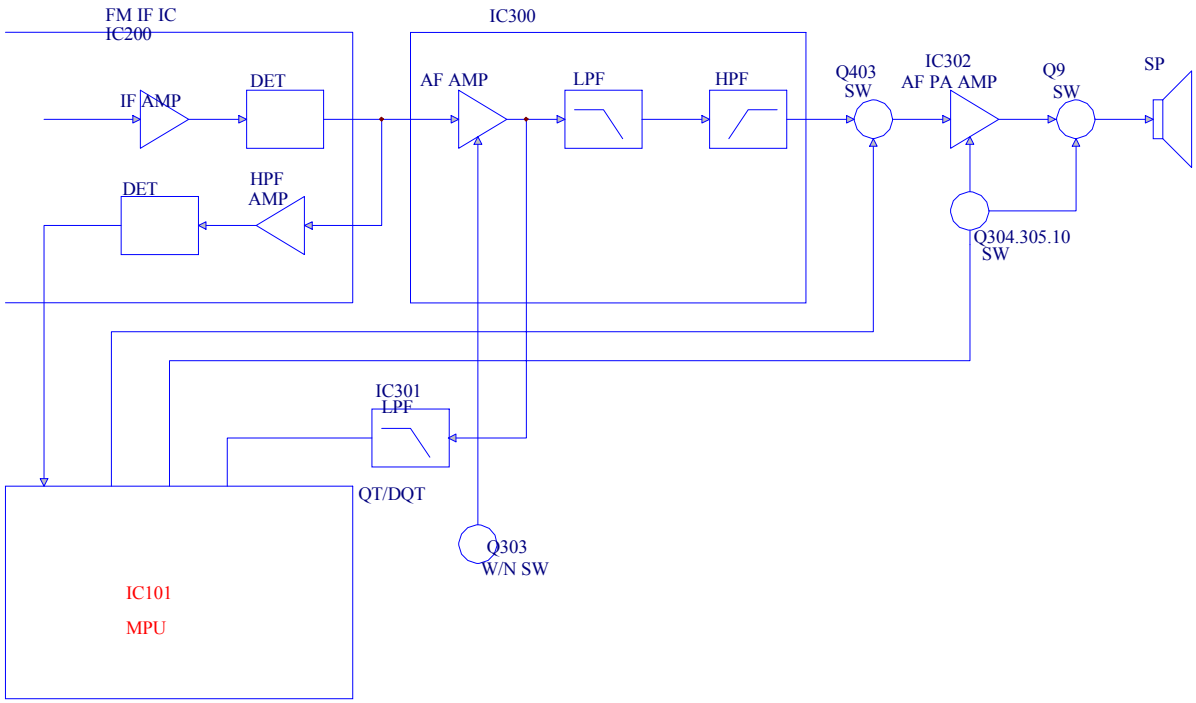

Fig.3 AF Amplifier and squelch

⑥. Receive signaling

CTCSS/CDCSS

300Hz and higher audio frequencies of the output signal from IF IC are cut by a low-pass filter

(IC300).The resulting signal enters the microprocessor (IC101). IC101 determines whether the CTCSS or CDCSS matches the preset value, and controls the MUTE and AFPAC and the speaker out sounds according to the squelch results.

3. PLL Frequency synthesizer

The PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission.

①. PLL

The frequency step of the PLL circuit is 5 of 6.25kHz.

A 12.8MHz reference oscillator signal is divided at IC1 by a fixed counter to produce the 5 or 6.25kHz reference frequency. The voltage controlled oscillator (VCO) output signal is buffer amplified by Q6.thendivided in IC1 by a dual-module programmable counter. The divided signal in the phase comparator in IC1. The output signal from the phase comparator is filtered through a low-pass filter and passed to the VCO to control the oscillator frequency. (See Fig.4)

②. VCO

The operating frequency is generated by Q4 in transmit mode and Q3 in receive mode. The oscillator frequency is controlled by applying the VCO control voltage, obtained from the phase comparator, to the varactor diodes (D1,D2 and D3,D4 in transmit mode and D901,D902 and D903,D904 in receive mode). The T/R pin is set high in receive mode causing Q5 and Q7 to turn Q4 off, and turn Q3 on. The T/R pin is set low in transmit mode. The outputs from Q3 and Q4 are amplified by Q6 and sent to the buffer amplifiers.

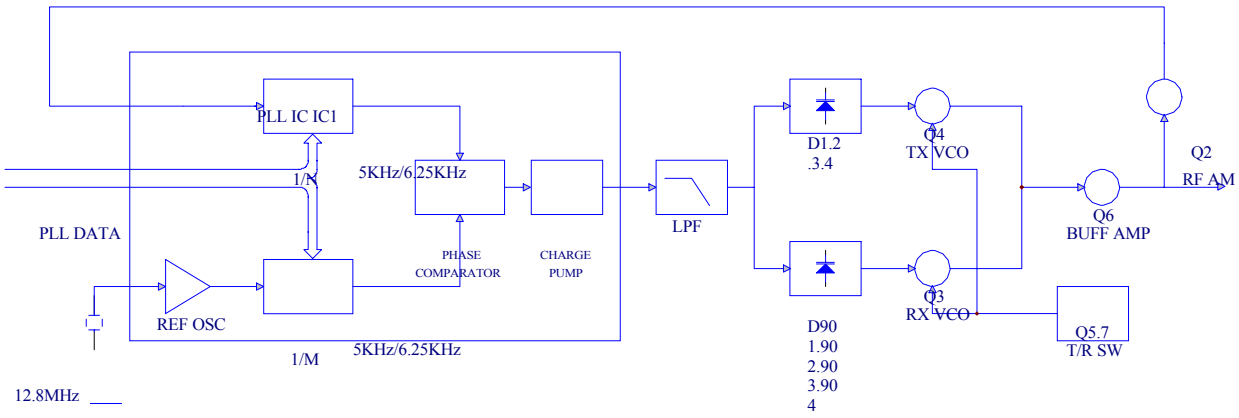

Fig.4 PLL circuit

③. UNLOCK DETECTOR

If a pulse signal appears at the LD pin of IC1, an unlock condition occurs, and the DC voltage obtained from D7,R6, and C914 causes the voltage applied to the UL pin of the microprocessor to go low. When the microprocessor detects this condition, The transmitter is disabled, ignoring the push-to-talk switch input signal. (See Fig.5)

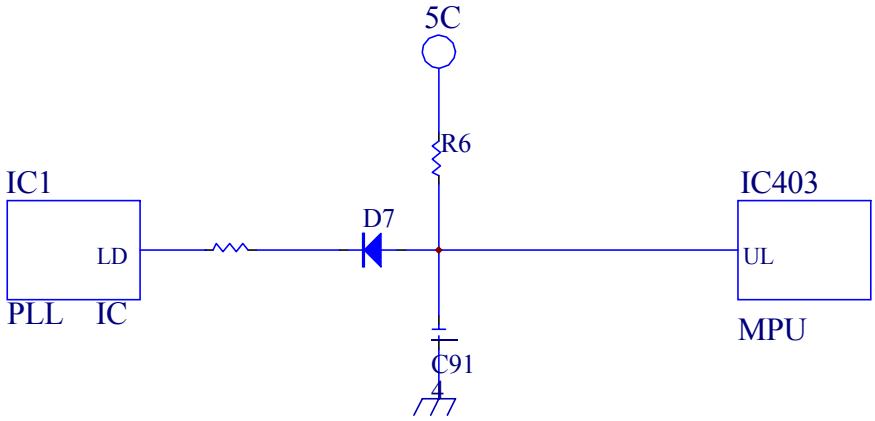

Fig.5 Unlock detector circuit

4. Transmitter

①. Transmit audio

The modulation signal from the microphone is amplified by IC500(1/2),passes through a preemphasis circuit, and amplified by the other IC500(1/2) to perform IDC operation. The signal then passes through a low-pass filter (splatter filter) (Q501 and Q502) and cuts 3kHz and higher frequencies. The resulting signal goes to the VCO through the VCO modulation terminal for direct FM modulation.(See Fig.6)

②. CTCSS/CDCSS encoder

A necessary signal for CTCSS/CDCSS encoding is generated by IC101 and FM-modulated to the PLL reference signal. Since the reference OSC does not modulate the loop characteristic frequency or higher, modulation is preformed at the VCO side by adjusting the balance.(See Fig.6)

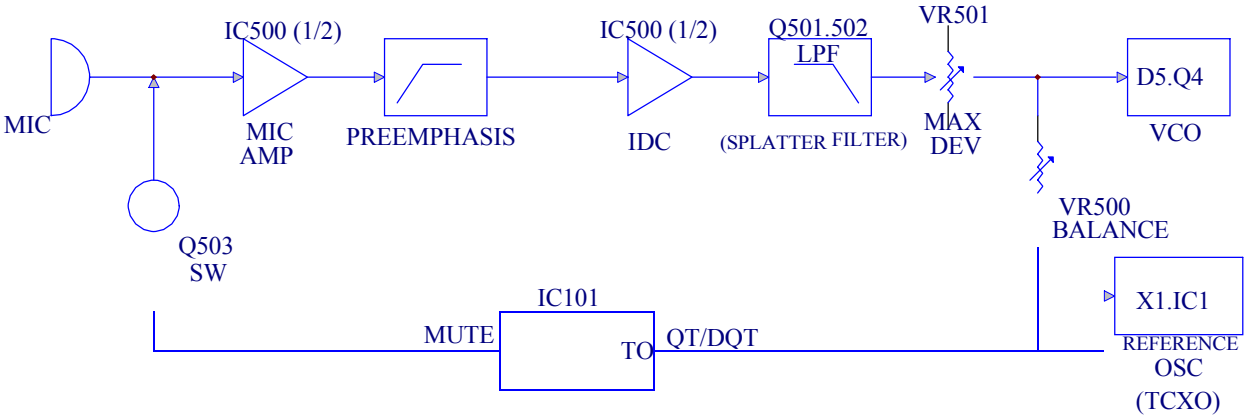

Fig.6 Transmit audio CTCSS/CDCSS

③. VCO and RF amplifier

The transmit signal obtained from the VCO buffer amplifier Q100,is amplified by Q101 and Q102. This amplified signal is passed to the power amplifier,Q105 and Q107,which consists of a 2-stage FET amplifier and is capable of producing up to 4W of RF power.(See fig .7)

④. ANT switch and LPF

The RF amplifier output signal is passed through a low pass filter network and a transmit/receive switching circuit before it is passed to the antenna terminal .The transmit/receive switching circuit is comprised of D101, D102 and D103. D102 and D103 are turned on (conductive) in transmit mode and off(isolated) in receive mode.

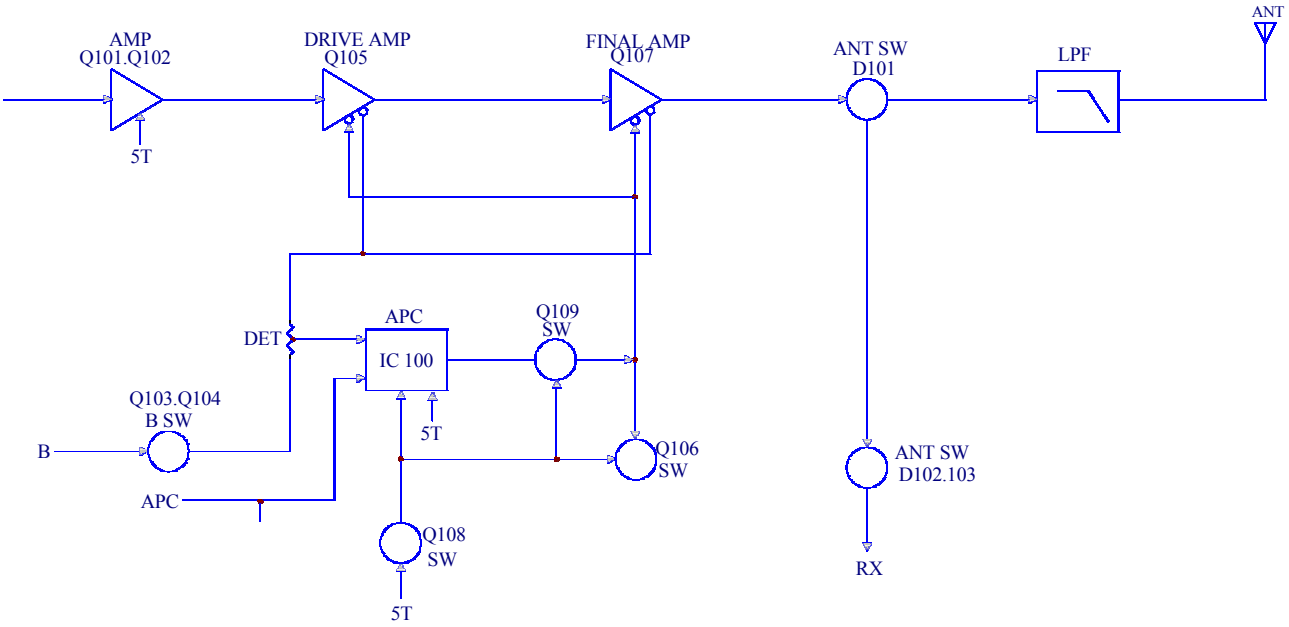

Fig. 7 APC system

⑤.
APC

The automatic power control (APC) circuit stabilizes the transmitter output power at a predetermined level by sensing the drain current of the final amplifier Field Effect Transistor (FET).The voltage comparator, IC100(2/2),compares the voltage obtained form the above drain current with a reference voltage which is set using the microprocessor .An APC voltage proportional to the difference between the sensed voltage and the reference voltage appears at the output of IC100(1/2).This output voltage controls the gate of the FET power amplifier, which keeps the transmitter output power constant. The transmitter output power can be varied by the microprocessor which in turn changes the reference voltage and hence ,the output power.

5. Power supply

A 5V reference power supply [5M] for the control circuits is derived from internal battery. This reference is used to provide a 5V supply in transmit mode [5T], a 5V supply in receive mode[5R], and a 5V supply common in both modes[5C] based on the control signal sent from the microprocessor.

6. Control system

The IC101 CPU operates at 7.3728MHz.This oscillator has a circuit that shifts the frequency according to the EEPROM data.