CIRCUIT DESCRIPTION

1. Frequency Configuration

The receiver utilizes double conversion. The first IF is 38.85MHz and the second IF is 450 kHz. The first local oscillator signal is supplied from the PLL circuit. The PLL circuit in the transmitter generates the necessary frequencies. Fig. 1 shows the frequencies.

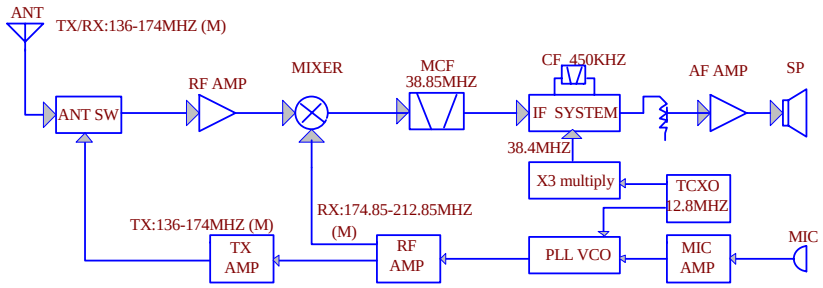

Fig. 1 Frequency configuration

2. Receiver

The frequency configuration of the receiver is shown in Fig. 2.

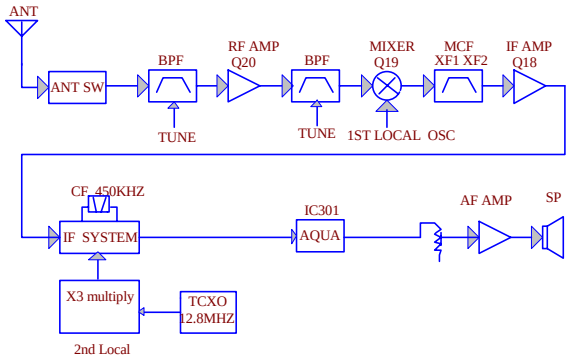

Fig. 2 Receiver section

1) Front End (RF AMP)

The signal coming from the antenna passes through the transmit/receive switching diode circuit, (D15,D10,D11 and D12) passes through a BPF (L47,L45 and L46), and is amplified by the RF amplifier (Q20).The resulting signal passes through a BPF (L19) and goes to the mixer. These BPFs are adjusted by variable capacitors (TC4 and TC5). The input voltage to the variable capacitor is regulated by voltage output from the microprocessor (IC7).

2) First Mixer

The signal from the front end is mixed with the first local oscillator signal generated in the PLL circuit by Q19 to produce a first IF frequency of 38.85 MHz.The resulting signal passes through the XF1,XF2 MCF to cut the adjacent spurious and provide the Opitimun characteristics, such as adjacent frequency selectivity

CIRCUIT DESCRIPTION

3) IF Amplifier Circuit

The first IF signal is passed through a four-pole monolithic crystal filter (XF1,XF2) to remove the adjacent channel signal. The filtered first IF signal is amplified by the first IF amplifier (Q18) and then applied to the IF system IC (IC4). The IF system IC provides a second mixer, second local oscillator, limiting amplifier, quadrature detector and RSSI (Received Signal Strength Indicator). The second mixer mixes the first IF signal with the 38.4MHz of the second local oscillator output (TCXO X3) and produces the second IF signal of 450kHz.The second IF signal is passed through the ceramic filter (CF200) to remove the adjacent channel signal. The filtered second IF signal is amplified by the limiting amplifier and demodulated by the quadrature detector with the ceramic discriminator (CD1). The demodulated signal is routed to the audio circuit.

4) Wide/Narrow Switching Circuit

Narrow and Wide settings can be made for each channel by switching the demodulation level.The WIDE (low level) and NARROW (high level) data is output from IC7, pin 6.When a WIDE (low level) data is received, Q301 turn on. When a NARROW (high level) data is received,Q301 turn off. Q301 turns on/off with the Wide/Narrow data and the IC300 detector output level is switched to maintain a constant output level during wide or narrow signals.

5) Audio Amplifier Circuit

The demodulated signal from IC4 goes to AF amplifier through IC301.The signal then goes through an AF volume control , and is routed to an audio power amplifier (IC5) where it is amplified and output to the speaker.

6) Squelch

Part of the AF signal from the IC enters the FM IC (IC4) again, and the noise component is amplified and rectified by a filter and an amplifier to produce a DC voltage corresponding to the noise level.The DC signal from the FM IC goes to the analog port of the microprocessor (IC7). IC405 determines whether to output sounds from the speaker by checking whether the input voltage is higher or lower than the preset value. To output sounds from the speaker, IC7 sends a high signal to the SP MUTE line and turns IC302 on through Q39,Q23,Q22,andQ38 . (See Fig. 3)

7) Receive Signalling

(1) QT/DQT

The output signal from FM IC(IC4) enters the microprocessor(IC7) through IC300. IC7 determines whether the QT or DQT matches the preset value, and controls the SP MUTE and the speaker output sounds according to the squelch results.

2) MSK (Fleet Sync)

The MSK input signal from the FM IC goes to pin 10 of IC 300. The signal is demodulated by MSK demodulator in IC 300.

The demodulated data goes to the CPU for processing.

(3) DTMF

The DTMF input signal from the FM IC (IC4) goes to IC300. The decoded information is then processed by the CPU.

CIRCUIT DESCRIPTION

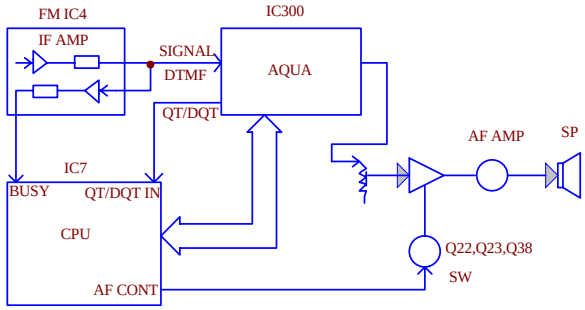

Fig. 3 AF amplifier and squelch

3. PLL Frequency Synthesizer

The PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission.

1) PLL

The frequency step of the PLL circuit is 2.5, 5, 6.25 or7.5kHz.

A 12.8MHz reference oscillator signal is divided at IC1 by a fixed counter to produce an oscillator (VCO) output signal which is buffer amplified by Q2 then divided in IC1 by a programmable counter. The divided signal is compared in phase with the 5 or 6.25kHz reference signal from the phase comparator in IC1. The output signal from the phase comparator is filtered through a low-pass filter and passed to the VCO to control the oscillator frequency. (See Fig. 4)

2) VCO

The operating frequency is generated by Q4 in transmit mode and Q3 in receive mode. The oscillator frequency is controlled by applying the VCO control voltage, obtained from the phase comparator, to the varactor diodes (D2 and D4 in transmit mode and D1 and D3 in receive mode). The RX pin is set high in receive mode causing Q7 turn on.The TX pin is set high in transmit mode. The outputs from Q3 and Q4 are amplified by Q6,Q100 and sent to the RF amplifiers.

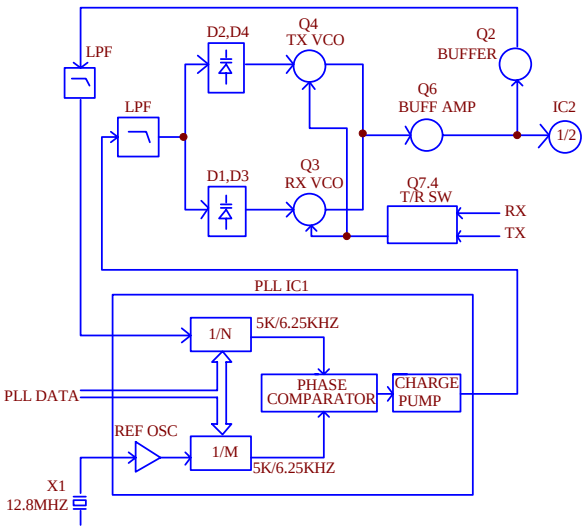

Fig. 4 PLL circuit

3) Unlock Detector

CIRCUIT DESCRIPTION

If a pulse signal appears at the LD pin of IC1, an unlock condition occurs, and the DC voltage obtained from C1,R6 and D7 causes the voltage applied to the microprocessor to go low. When the microprocessor detects this condition, the transmitter is disabled, ignoring the push-to-talk switch input signal.

4. Transmitter System

1) Microphone Amplifier

The signal from the microphone passes through the IC301. When encoding DTMF, it is turned OFF for muting the microphone input signal by IC301.The signal passes through the Audio processor (IC301) for the maximum deviation adjustment, and goes to the VCO modulation input.(see Fig 5)

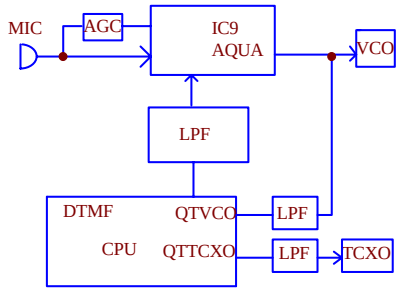

Fig. 5 Microphone amplifier

2) Drive and Final Amplifier

The signal from the T/R switch (D9 is on) is amplified by the pre-drive (Q13) and the drive amplifier (Q14) to 50mW. The output of the drive amplifier is amplified by the RF power amplifier (Q15) to 5.0W (1W when the power is low). The RF power amplifier consists of two MOS FET stages. The output of the RF power amplifier is then passed through the harmonic filter (LPF) and antenna switch (D15) and applied to the antenna terminal.

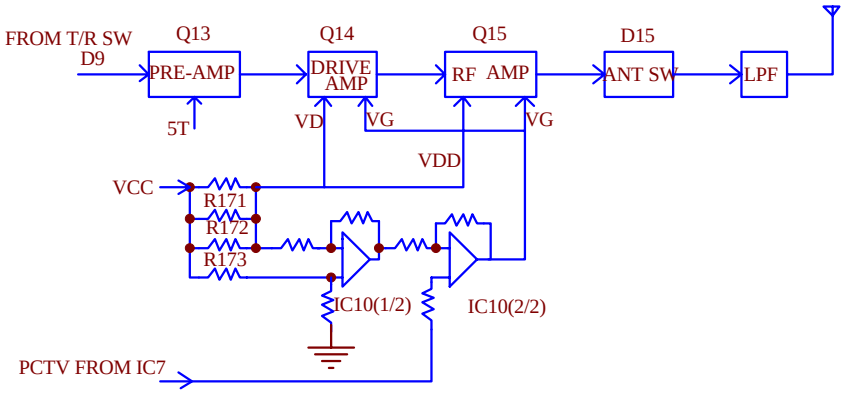

Fig. 6 Drive and final amplifier and APC circuit

3) APC Circuit

The APC circuit always monitors the current flowing through the RF power amplifier (Q15) and keeps a constant current. The

voltage drop at R171, R172 and R173 is caused by the current flowing through the RF power amplifier and this voltage is applied to the differential amplifier IC10 (1/2). IC10 (2/2) compares the output voltage of IC10 (1/2) with the reference voltage from IC7. The output of IC10 (2/2) controls the VG of the RF power amplifier, drive amplifier and pre-drive amplifier to make both voltages the same. The change of power high/low is carried out by the change of the reference voltage.(see Fig.6)

4) Encode Signalling

(1) QT/DQT

QT,DQT data of the QTTCXO Line is output from pin 27of the CPU. The signal passes through a low-pass CR filter and goes to the TCXO(X1).The QT,DQT data of the QTVCO Line is output from pin 10 of the CPU. The signal passes through a low pass CR filter, mixes with the audio signal, and goes to the VCO modulation input. TX deviation is adjusted by the CPU.

(2) DTMF

High-speed data is output from pin 2 of the CPU. The signal passes through a low-pass CR filter, and provides a TX and SP out tone, and is then applied to the audio processor (IC9). The signal is mixed with the audio signal and goes to the VCO. TX deviation is adjusted by the CPU.

(3) MSK (Fleet Sync)

Fleet Sync utilizes 1200bps and 2400bps MSK signal is output from pin 7of IC9. And is routed to the VCO. When encoding MSK, the microphone input signal is muted.

5. Power Supply

There are four 5V power supplies for the microprocessor:

5M,5C, 5R, and 5T. 5M for microprocessor is always output while the power is on. 5M is always output, but turns off when the power is turned off to prevent malfunction of the microprocessor.

5C is a common 5V and is output when SAVE is not set to OFF.

5R is 5V for reception and output during reception.

5T is 5V for transmission and output during transmission]

6. Control Circuit

The control circuit consists of a microprocessor (IC7) and its peripheral circuits. It controls the TX-RX unit. IC7 mainly performs the following:

(1) Switching between transmission and reception by the PTT signal input.

(2) Reading system, group, frequency, and program data from the memory circuit.

(3) Sending frequency program data to the PLL.

(4) Controlling squelch on/off by the DC voltage from the squelch circuit.

(5) Controlling the audio mute circuit by the decode data input.

(6) Transmitting tone and encode data.

1) Frequency Shift Circuit

The microprocessor (IC7) operates at a clock of 7.3728MHz. This oscillator has a circuit that shifts the frequency by BEAT SHIFT SW (Q40,Q41). A beat sound may be able to be evaded from generation if “Beat Shift” is set to ON when it is generated in the internal spurious transmission modulated sound of a transceiver.(see Fig.7)

CIRCUIT DESCRIPTION

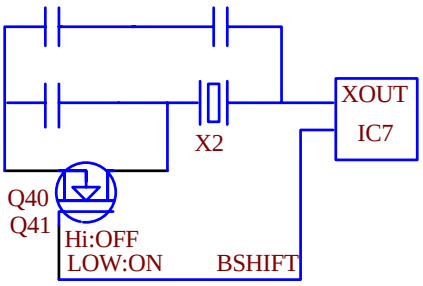

Fig. 7 Frequency shift circuit

2) Memory Circuit

Memory circuit consists of the CPU (IC7) and an EEPROM (IC6). An EEPROM has a capacity of 64k bits that contains the transceiver control program for the CPU and data such as transceiver channels and operating features.

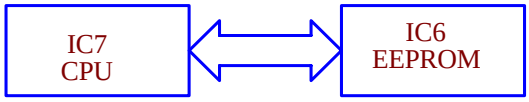

Fig. 8 Memory circuit

3) Low Battery Warning

The battery voltage is checked using by the microprocessor. The transceiver generates a warning tone when it falls below the warning voltage shown in the table.

(1) The red LED blinks when the battery voltage falls below the voltage (1) shown in the table during transmission.

Note:

The transceiver checks the battery voltage during reception even when, in the FPU, the Battery Warning status function is set to “On TX” (default setting).However, the LED does not blink during reception. During transmission, the LED blinks to generate the warning tone of a low battery voltage.

(2) The transceiver immediately stops transmission when the battery voltage falls below the voltage (2) shown in the table. A message tone beeps while the PTT switch is released

.

	Ni-Cd Battery	Ni-MH Battery
(1)	6.2[V]	6.2[V]
(2)	5.9[V]	5.9[V]

CIRCUIT DESCRIPTION

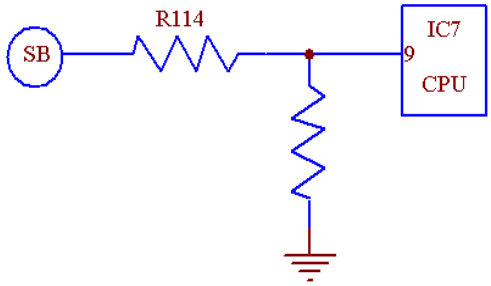

Fig. 10 Low battery warning

7. Control System

Keys and channel selector circuit.

The signal from the keys and channel selector are directly input to the microprocessor, as shown in fig. 10.

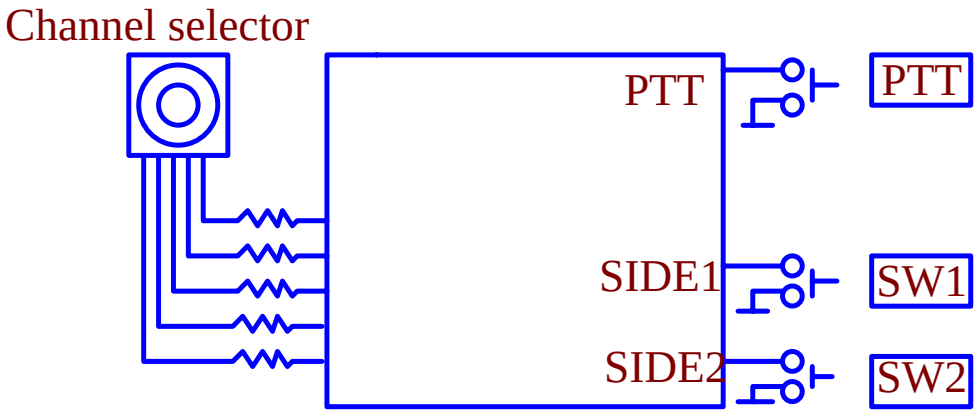

Fig. 11 Control system