Azalea MSR 2000 hardware functional specification

Modification history

Revision	Department	Authors/Reviewer	Date	Description
0.1	Engineering	David Sun	10/31/2005	Initial draft
0.2	Engineering	David Sun	12/16/2005	Added software design
1.0	Engineering	David Sun	05/20/2006	Release
1.1	Engineering	David Sun	03/31/2007	Change Format

Review History

Revision	Department	Authors/Reviewer	Date	Description
	Engineering	Engineering Project Manager (reviewer)		
	Engineering	Reviewer1		
	Engineering	Reviewer2		
	QA	Reviewer3		
	Product marketing	Reviewer4		
	Product Management	Engineering Product manager(reviewer)		

Table of Contents

1 Overview

This documentation is the Hardware Design Function Specification for MSR 2000, it is a 802,11 mesh router. It has two wireless channel, one 802.11 a for back haul, and 802.11 b/g for access. It have two 10/100M Ethernet port. The primary application of MSR 2000 is for WLAN, This hardware design is based on current protocol version.

1.1 Design Considerations

This is a outdoor module, need to meet special requirement.
Try to keep all feature's of old MSR 50, to make it software compatible with old design.

2 High-Level Description

2.1 Design Goal.

One Back haul radio operates at 5G Hz, able to support 4.9 Ghz. Support software programmable radio frequency. Require 500m back haul distance at minimum of 24Mbps throughput, with transmission power software programmable.

One access radio operates on 2.4GHz, for backward compatible with 802.11b.
Require transmission power at 200mw, at distance of 260m radius coverage on omni-direction antenna,
260m@6Mbps.

Two 100 base T Ethernet interface for gateway.
One console port, serial port .

(from tropos)

Environmental Specifications

• Operating temperature range: -40°C to 55°C
• Storage temperature range: -40°C to 85°C
• Weather rating: IP67 weathertight
• Wind survivability: >165 mph
• Wind loading (165 mph): <1024 Newtons
• MIL-STD-810F 509.4 Salt Fog rust resistance compliant
• Shock & vibration: ETSI 300-19-2-4 spec T41.E class 4M3
• Transportation: ISTA 2A

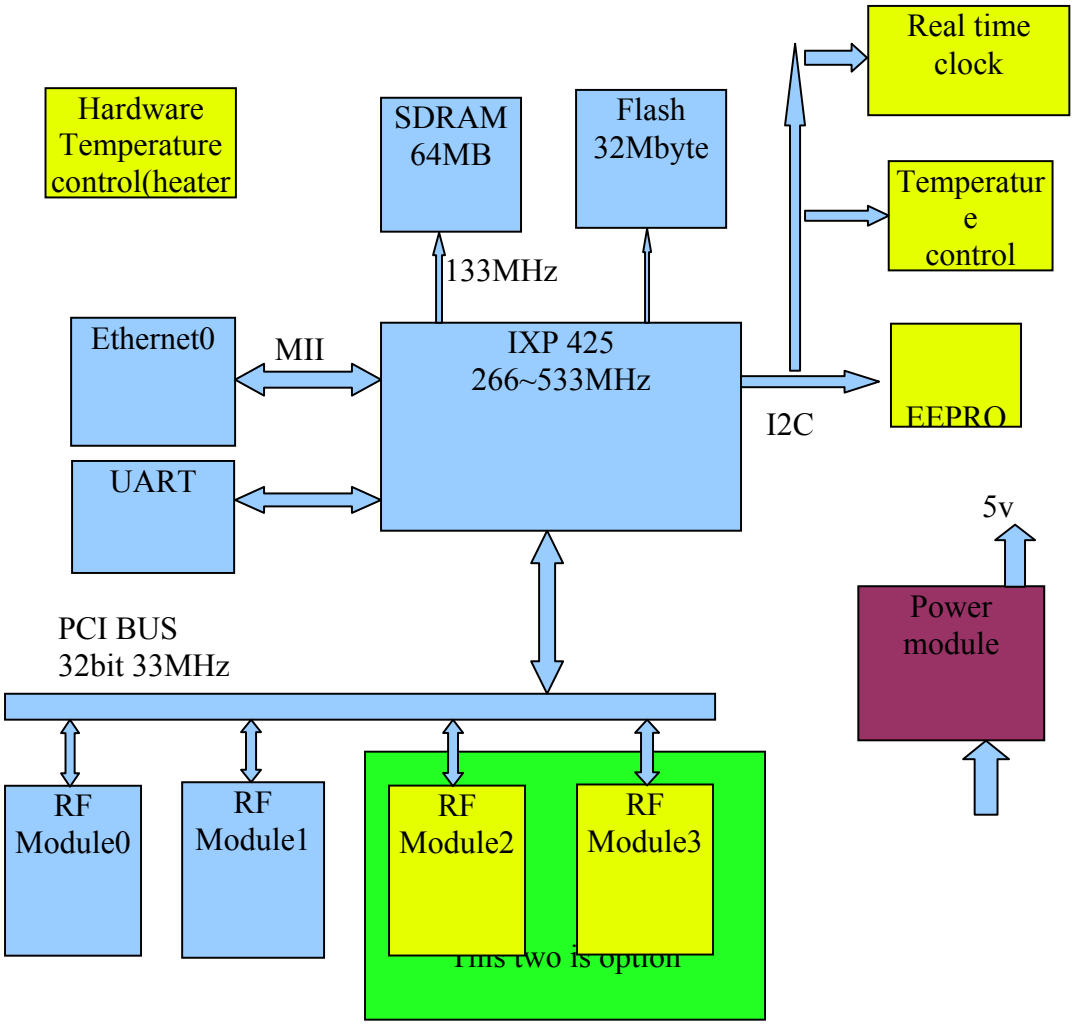
Hardware Specifications

• 10/100Base T Ethernet
• Power input:
- 90-260VAC 50/60Hz
category C3 integrated branch circuit protection
- AC power consumption: 10 W typical, 30 MAX (with heat circuit on)
• Power-on and network status lamp: Green/Red
• Dimensions (w/o mounting brackets or antennas): 13.00 in (33.02 cm) wide x 8.00 in (20.32 cm) deep x 5.3 in (13.50 cm) high
• Weight: 14 lbs (6.40 kg) max., with mounting brackets,

Protection Circuits

• Antenna Protection: ≤ 0.5μJ for 6kV/3kA @ 8/20μS Waveform
• Electrical Protection:
- ANSI/IEEE C62.41, UL 1449-2nd ed., 10kA @ 8/20 μS Wave form, 36kA per phase, L-L, L-N, L-PE
- EN61000-4-5 Level 4 AC Surge Immunity
- EN61000-4-4 Level 4 Electrical Fast Transient Burst Immunity
- EN61000-4-3 EMC Field Immunity
• Data Protection:
  - EN61000-4-2 Level 4 ESD Immunity
  -

System Block Diagram



Yellow box is new.
Purple box is changed

3 detailed description

3.1 IXP425

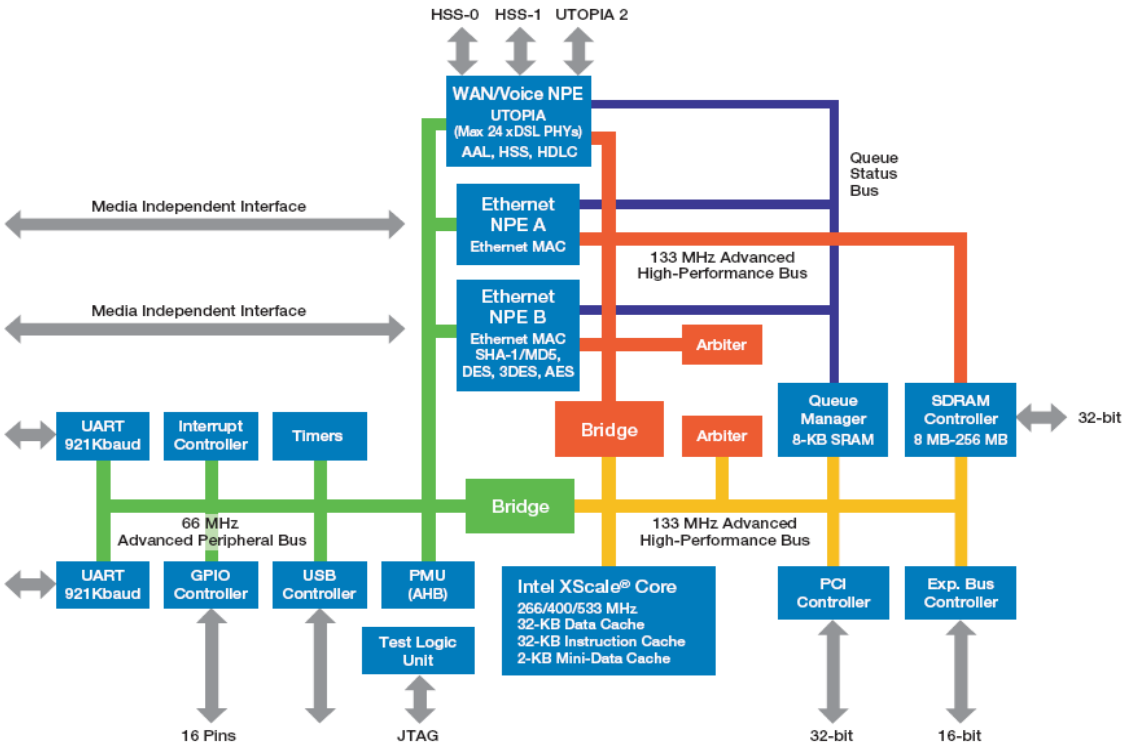
The Intel® IXP425 Product Line of Network Processors is compliant with the ARM* Version 5TE instruction-set architecture (ISA). The Intel® IXP425 product line is designed with Intel 0.18-µ production semiconductor process technology. This process technology — along with the compactness of the Intel XScale core, the ability to simultaneously process up to three integrated network processing engines (NPEs), and numerous dedicated-function peripheral interfaces — enables the IXP42X product line to operate over a wide range of low-cost networking applications, with industry-leading performance.

Intel XScale® Core — Up to 533 MHz
- PCI Interface
- USB v1.1 Device Controller
- SDRAM Interface
- High-Speed UART
- Console UART
- Internal Bus Performance Monitoring Unit
- 16 GPIOs
- Four Internal Timers
- Packaging

—492-pin PBGA
- Commercial(533)/Extended Temperature(266/400)

3.3v i/o, Max current 0.26A
1.3v core, Max current 1.0A

IXP425 block diagram



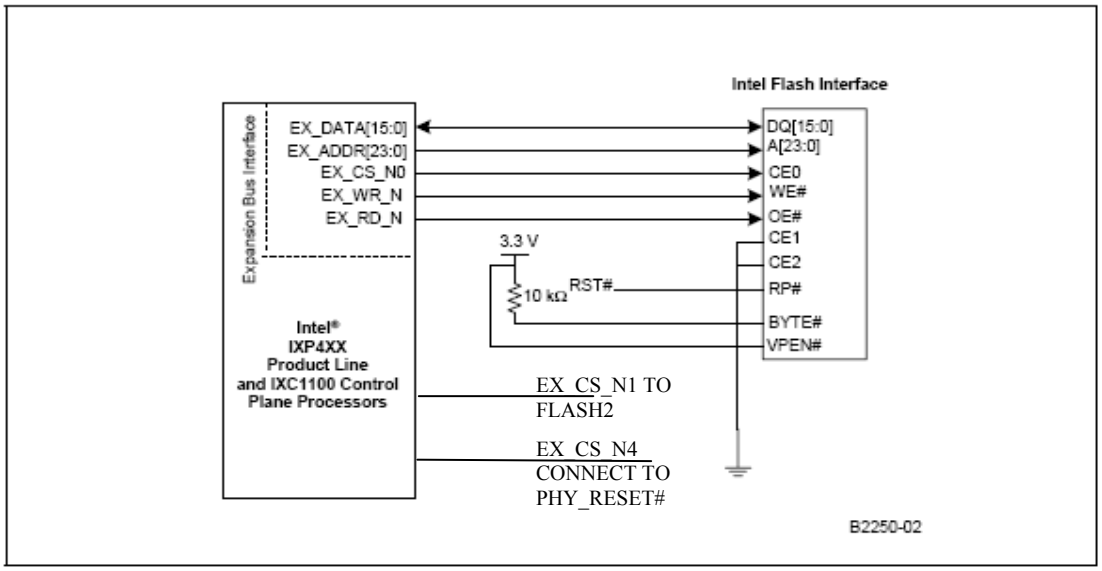
Intel® IXP425 Network Processor

3.2 Flash

The boot flash Memory is intel's strataflash memory (j3) TE28F128J3C120
performance
--110/115/120/150 ns initial access speed.
--25ns Asynchronous page mode reads.
--32byte write buffer, 6.8us per byte
software
--program and erase suspend support
--flash data integrator (FDI), common flash interface(CFI) compatible.
security
--128bit protection register
--Absolute protection with VPEN = gnd
--individuate block locking
--block erase/program lockout during power transitions.
IccMax = 80 mA

Boot code will be load to flash through ICE for the first time.

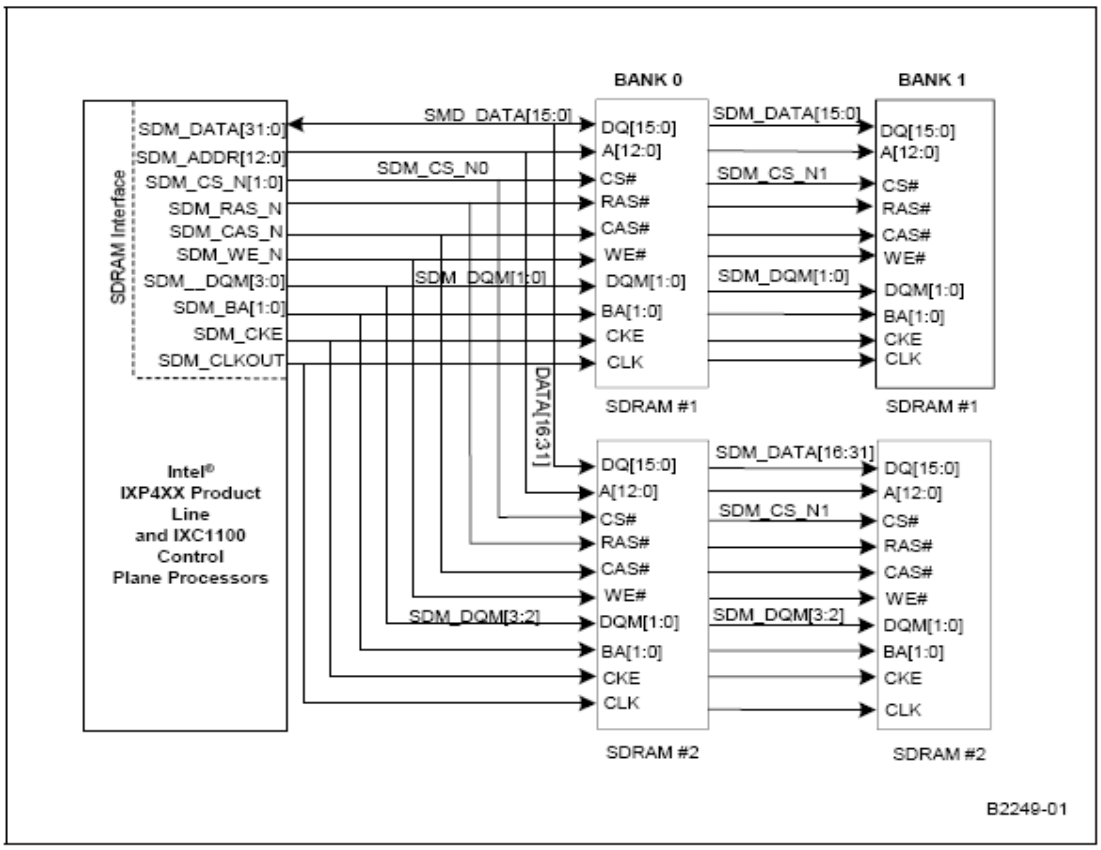
Expansion Bus Flash Interface



3.3 SDRAM

The SDRAM memory controller, integrated into the IXP425 processors, supports a 32-bit data bus interface operating at 133 MHz, eight open pages, two external banks with memory configuration from 8 to 256 Mbytes.

Dual Bank SDRAM System Block Diagram (x16 Devices)

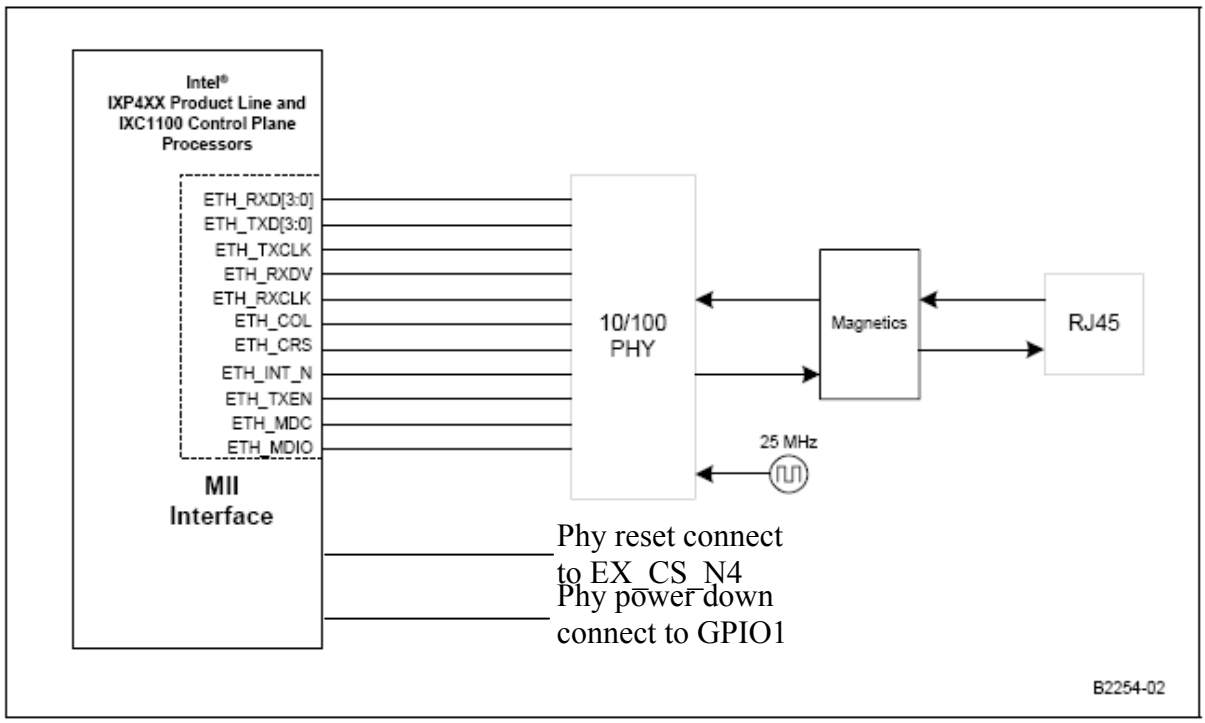


3.4 100 Base T Phy

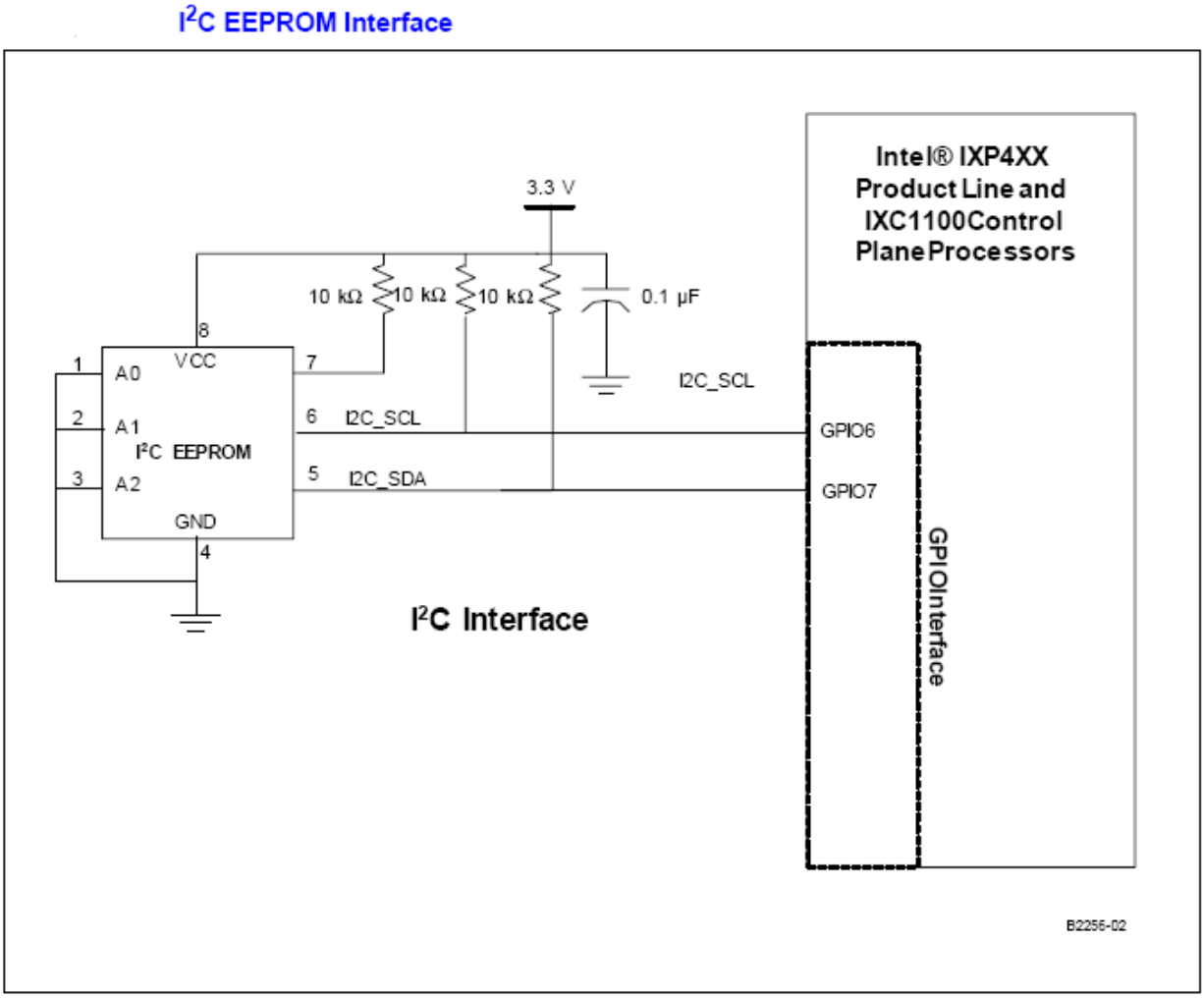
eth0 define as phy addr3,
eth1 define as phy addr1,
(same as lanready).

** need pay attention to input port surge protection and lightning protection
• Data Protection:
- EN61000-4-2 Level 4 ESD Immunity.

MII Block Diagram



3.5 EEPROM



3.6 RF Module

RF module interfaces with IXP425 through pci bus, We can use mini pci bus socket, and use off the shelf module, or we can design our own RF module on the board(may have some RF lay out challenge).

Need pay attention to lightning protection.

3.7 Power supply.

We use off the shelf AC to DC converter, Input 90 to 230, 50/60, output 5v, 6A.
We use on board DC to DC Switch Regulator to convert 5v to 3.3v,4 A, 1.3v, 1A.

This is a outdoor device, need follow these protection standard.

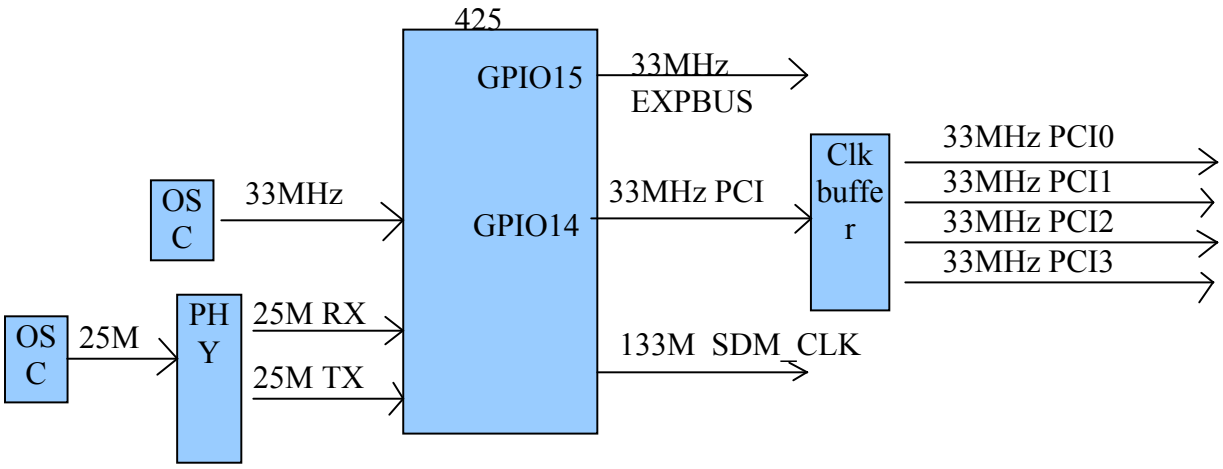
• Electrical Protection:
- ANSI/IEEE C62.41, UL 1449-2nd ed., 10kA @ 8/20 μS Wave form, 36kA per phase, L-L, L-N, L-PE

- EN61000-4-5 Level 4 AC Surge Immunity
- EN61000-4-4 Level 4 Electrical Fast Transient Burst Immunity
- EN61000-4-3 EMC Field Immunity

3.8 Clock

The IXP42X product line processors require a 33.33-MHz reference clock that generates all core and most internal peripheral clocks. The 33.33-MHz reference clock may be generated using on board crystal, oscillator, or PLL chip. This clock is multiplied internally by the processors to 133 MHz and driven to the PC133 SDRAM interface.
The interfaces require oscillators or crystals on the board.

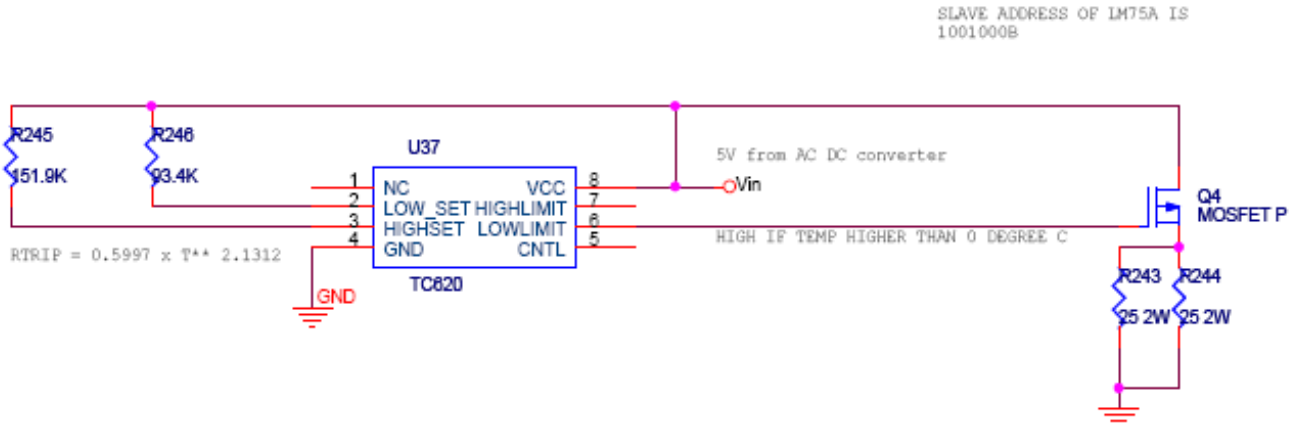
- Processors' system clock - 33.33 MHz
- PCI host clock - 33 MHz and 66 MHz selectable
- Expansion bus clock - This expansion bus clock may be driven through GPIO15 or using an external oscillator.
- Each Ethernet phy need a 25Mhz clock.



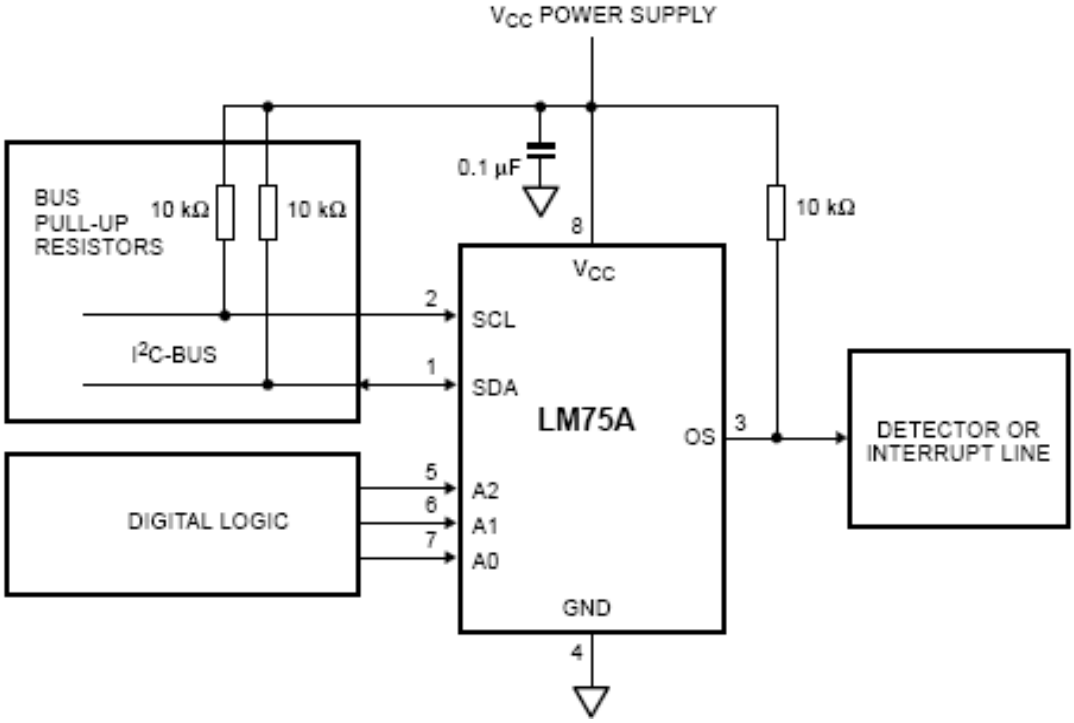
3.9 Temperature control

We have two level Temperature control, for hardware control we use TC620
Dual Trip Point Temperature Sensors, when ambient temperature is lower than 0 degree C, it will start heat circuit, this design is to prevent some components malfunction when system power on in very cold environment. For software control we use LM75A Digital temperature sensor and thermal Watchdog, processor can check this sensor through I2C bus, if system to hot, software can lower the load by stop some processing. The address of LM75A is 1001000B.

3.9.1. Circuit for hardware temperature controller.

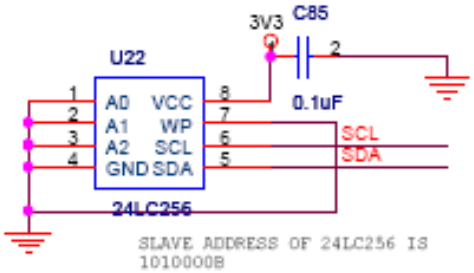


3.9.2. Software temperature controller circuit



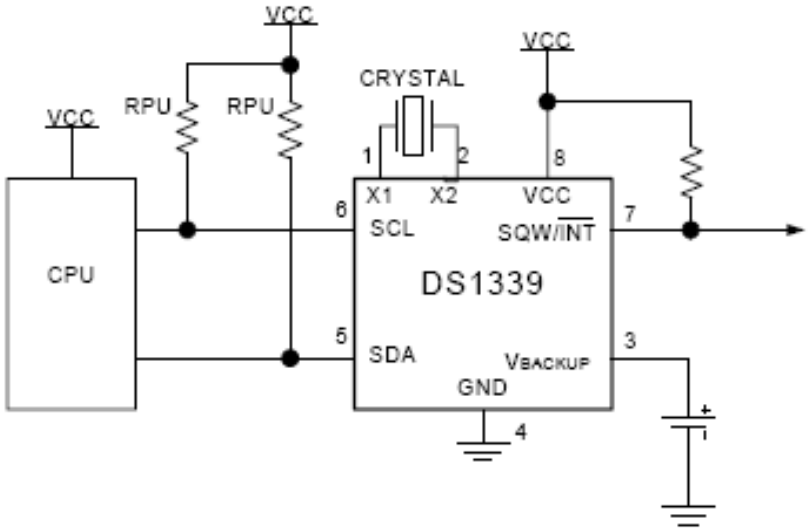
3.10 EEPROM interfaces

EEPROM is 16Kbits organized in 8 blocks of 256X8bits memory. The slave address of the device is 1010000B



3.11 Real Time Clock

The DS1339 serial real-time clock (RTC) is a low power clock/date device with two programmable time of day alarms and a programmable square-wave output. Address and data are transferred serially through an I2C* bus. The clock/date provides seconds, minutes, hours, day, date, month, and year information, slave address of this chip is 1101000B



3.12 PCI bus interface

The IXP425 processors' PCI controller is an industry standard, 32-bit interface, high-performance, low-latency system bus that operates at either 33 or 66 MHz. It is compliant with the *PCI Local Bus Specification*, Rev. 2.2. The PCI Controller supports operation as a PCI host and implements a PCI arbiter for a system containing up to four external PCI devices.
When IXP425 processor is host, it may interface to four PCI slots at 33 MHz or two PCI slots at 66 MHz. The limitation to two slots at 66 MHz is due to load requirements to maintain signal integrity at the higher frequency.

3.12.1. A PCI startup sequence could be as follows:

1. Power-on reset occurs to the IXP425 processor, theIntel XScale core starts execution (internal PLL assumed locked and internal clocks stable).
2. Software configures PCI reset and PCI clock GPIOs as outputs driving 0. A pull-down on the GPIO pin chosen to drive the PCI reset signal is required. This pull-down is required because the GPIO are at a tristated value until the device comes completely out of reset and the PCI reset needs to be low from the start.
3. Wait 1ms to satisfy minimum reset assertion time of the PCI specification.
4. Configure the PCI clock GPIO for the proper PCI bus frequency (defined in the section GPIO).
5. Enable the PCI clock GPIO to drive the PCI clock
6. Wait 100 μs to satisfy the "minimum reset assertion time from clock stable" requirement of the PCI specification.

7. Set the PCI reset GPIO output to drive a 1.
   This releases the PCI bus.

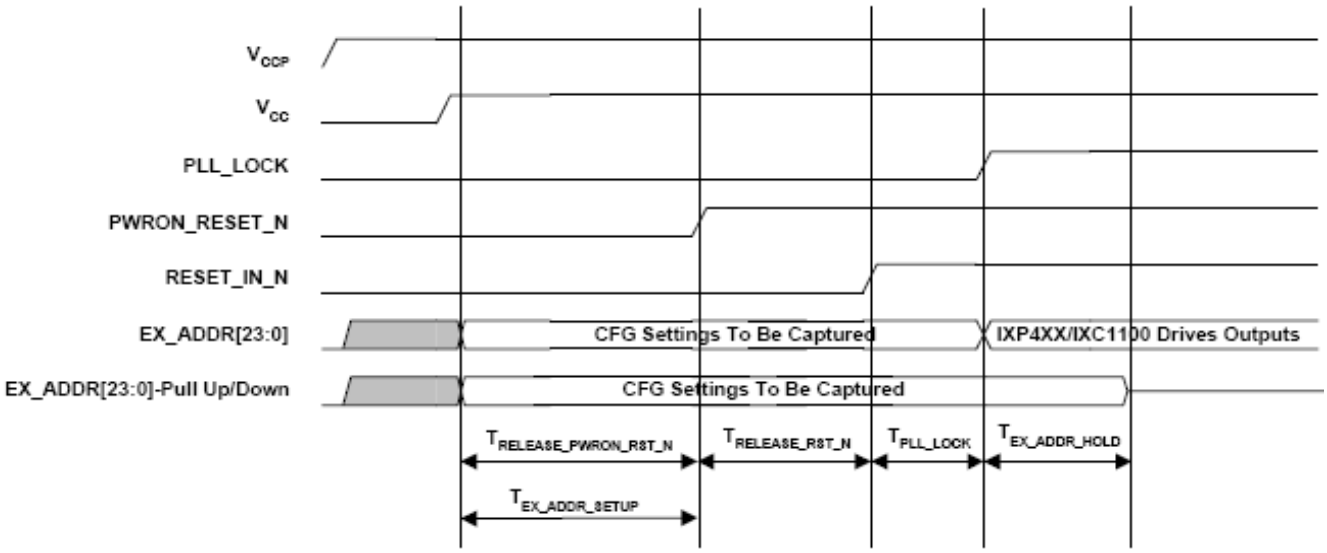
3.12.2. PCI Device and Interrupt table

pci slot 0 idsel use ad31, interrupt use PCI_INTA(GPIO11, int28). on up side of the board

pci slot 1 idsel use ad29, interrupt use PCI_INTC(GPIO9, int26). on up side of the board
pci slot 2 idsel use ad30, interrupt use PCI_INTB(GPIO10, int27). on bottom side of the board.
pci slot 3 idsel use ad28, interrupt use PCI_INTD(GPIO8, int25). on bottom side of the board.

3.13 System Power-On and reset sequence

The 3.3-V I/O voltage (VCCP) must be powered up 1 μs before the core voltage (VCC). The IXP425 processors' core voltage (VCC) must never become stable prior to the 3.3-V I/O voltage (VCCP). The VCCOSC, VCCPLL1, and VCCPLL2 voltages follow the VCC power-up pattern. The VCCOSCP follows the VCCP power-up pattern. The value for TPOWER_UP must be at least 1 μs. The TPOWER_UP timing parameter is measured from VCCP at 3.3 V and VCC at 1.3 V.



T_release_pwron_rst_n could be 0 if use external OSCillator.
T_release_rst_n Min is 10ns

3.14 GPIO Definitions

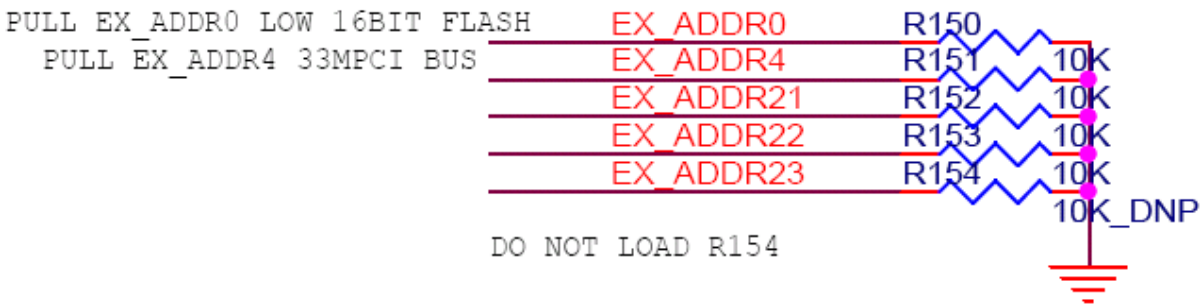
GPIO 0 pin y22 used as RXER0
GPIO 1 pin w21 used as power_dn_eth_phy
GPIO 2 use 0ohm resister connected to TXER0. We should not populate this resiester.
GPIO 2,3,4,5,12 connect to mini pci redundant signal.
GPIO 6 used as USB scl.
GPIO 7 used as USB sda.
GPIO 8,9,10,11 used as PCI intD,C,B,A.
GPIO 13 used as pci resetn.
GPIO 14 used as pci clk.
GPIO 15 used as expbus_clk.

3.15 Configuration Straps

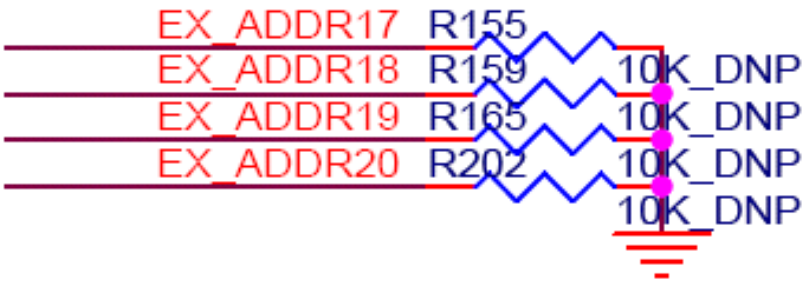
3.15.1. CPU speed

Factory Part Speed	*EX_ADDR 23 22 21*	*Actual Speed*
533 MHz	1 0 0	533 MHz
533 MHz	0 0 1	400 MHz
533 MHz	0 1 1	266 MHz
400 MHz	1 0 0	400 MHz
400 MHz	0 1 1	266 MHz
266 MHz	1 0 0	266 MHz

3.15.2. PCI bus clock and Flash bus width



3.15.3. User-Configurable Field



we load R155 on MSR2000, so when we read `Configuration Register 0, bit 20:17 = 0xE, software use this number identify different board. Lanready is 0xF`

4. Software considerations

Memory Map (Sheet 1 of 2)

Start Address	End Address	Size	Use
0000_0000	0FFF_FFFF	256 MB	Expansion Bus Data†
0000_0000	2FFF_FFFF	756 MB	SDRAM Data†
3000_0000	3FFF_FFFF		(Reserved)
4000_0000	47FF_FFFF		(Reserved)
4800_0000	4FFF_FFFF	128 MB	PCI Data
5000_0000	5FFF_FFFF	256 MB	Expansion Bus Data
6000_0000	63FF_FFFF	64 MB	Queue manager
6400_0000	BFFF_FFFF		(Reserved)
C000_0000	C3FF_FFFF	64 MB	PCI Controller Configuration and Status Registers
C400_0000	C7FF_FFFF	64 MB	Expansion Bus Configuration Registers
C800_0000	C800_0FFF	1 KB	High-Speed UART
C800_1000	C800_1FFF	1 KB	Console UART
C800_2000	C800_2FFF	1 KB	Internal Bus Performance Monitoring Unit
C800_3000	C800_3FFF	1 KB	Interrupt Controller
C800_4000	C800_4FFF	1 KB	GPIO Controller
C800_5000	C800_5FFF	1 KB	Timers
C800_6000	C800_6FFF	1 KB	WAN/HSS NPE = NPE A (IXP400 software definition) – Not User Programmable
C800_7000	C800_7FFF	1 KB	Ethernet NPE A = NPE B (IXP400 software definition) – Not User Programmable
C800_8000	C800_8FFF	1 KB	Ethernet NPE B = NPE C (IXP400 software definition) – Not User Programmable
C800_9000	C800_9FFF	1 KB	Ethernet MAC A
C800_A000	C800_AFFF	1 KB	Ethernet MAC B
C800_B000	C800_BFFF	1 KB	USB Controller
C800_C000	C800_FFFF		(Reserved)

Start Address	End Address	Size	Use
C801_0000	CBFF_FFFF		(Reserved)
CC00_0000	CC00_00FF	256 Byte	SDRAM Configuration Registers
CC00_0100	FFFF_FFFF		(Reserved)