Change from Rev1.0 to Rev 1.1

A. PCI BUS CHANGE IN PAGE 5 AND 6

1. in page 5 change wire connected to r218 from PCI_AD30 to PCI_AD29, to keep same config as MSR50

2. in page 6 change wire connected to r220 from PCI_AD29 to PCI_AD30, to keep same config as MSR50

3. Move r210 and r156 from bottom to top, in case we don't use pci on bottom.

4. Connect to foot to ground

B. CONSOLE (UART) AND HEAT CONTROL CHANGE IN PAGE 8

5. pin defined as 9pin DTE, need cross over cabel to connect to a PC, swaped pin2 and pin3

6. use fast uart (uart0) as console, also connect uart1 to the same port with a 0 ohm dnp resistor.

7. U27 TC620_8soic, swap pin 6 and 7, also change si9433 to FDN342P

C. POWER REGULATORS CHANGE IN PAGE 4

9 add 3V3 SUPERVISOR U57, IT DELAY 3V3 FAILURE BY 140 MS, KEEP RST OUT LOW WHICH DISABLE 1V3 OUTPUT.

10. change c261 from 0.1u(0603) to 4.7u(0805), change c248 from 8200p to 1000p, same footprint, change c259 from 33u to 150u, same footprint.

11. added a 4.7u c309 between pin 1 and 2 of U39.

12. fix poe footprint error.

D. IN PAGE 3

13. change R154, R202, R165, R159, R155 from 10k to 10k_DNP

14. make many change around U35

15. change symble U1B in page 3, Sort EX_DATA0 to 15 from top to bottom, to make same as EX_DATA bus order

16. change at uart interface, connect uart0 (fast uart) to 232 transceiver(rxdata and txdata). use 0ohm res DNP connect uart1 to another pair of transceiver(cts, rts).

E. IN PAGE9

11 pull addr[1:0] high, keep same as msr50 old config. phy1 are eth0, phy1 is eth1

Add D22 in page 8

add 1.6p cap in page5 and 6,

add 1.6p and 10pcap in page8

swap r133 and r218 on schematic only, reason is silkscreen and location is not match

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Size: A	Document Number: <Doc>	Rev: <RevCode>
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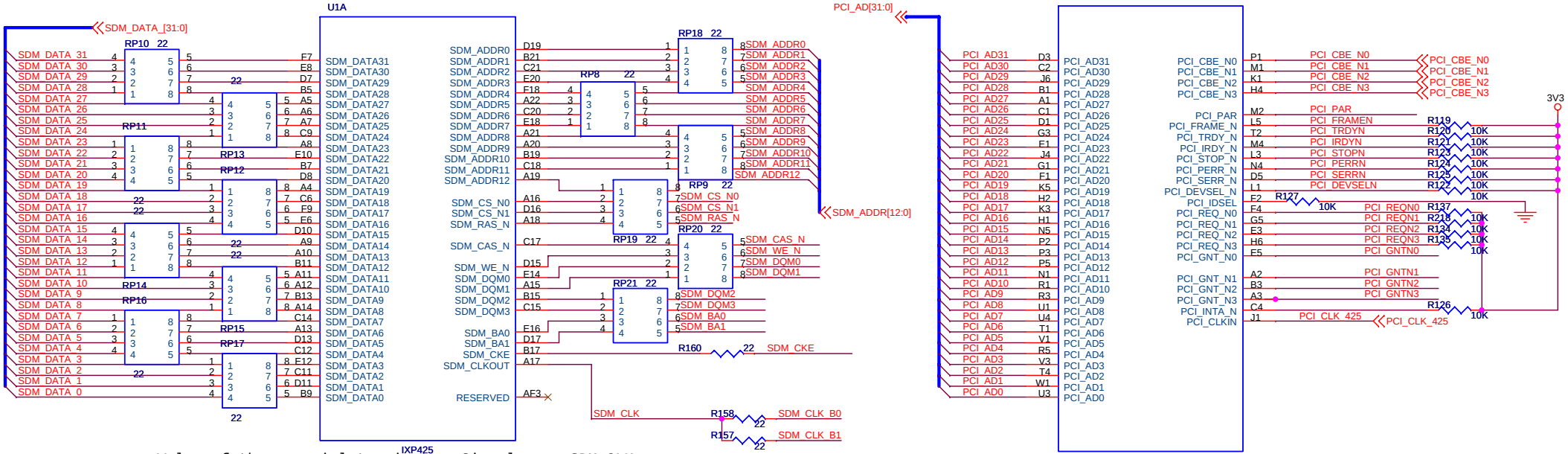

Value of these serial terminators need to be verified by simulation

Signal name SDM_CLK
Width 5 Spacing 15
Length Min 0.2 Max 0.5
Clocks must be routed with as much of the trace on inner signal layer as possible.
Clocks on the inner layer have a 5-mil ground trace surrounding them with vias stitched to ground at 0.5?intervals.

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Factory Part Speed	EX_ADDR 23 22 21	Actual Speed
533 MHz	1 0 0	533 MHz
533 MHz	0 0 1	400 MHz
533 MHz	0 1 1	266 MHz
400 MHz	1 0 0	400 MHz
400 MHz	0 1 1	266 MHz
266 MHz	1 0 0	266 MHz

PULL EX_ADDR0 LOW 16BIT FLASH
PULL EX_ADDR4 33MPCI BUS

change R154, R202, R165, R159, R155 from 10k to 10k_DNP

EX_ADDR0 R150 10K
EX_ADDR4 R151 10K
EX_ADDR21 R152 10K
EX_ADDR22 R153 10K
EX_ADDR23 R154 10K
10K_DNP
DO NOT LOAD R154

EX_ADDR17 R155 10K
EX_ADDR18 R159 10K
EX_ADDR19 R165 10K_DNP
EX_ADDR20 R202 10K_DNP
10K_DNP

change symble U1B, Sort EX_DATA0 to 15 from top to bottom, to make same as EX_DATA bus order

U1B
FLASH INTERFACE
EX_DATA [15:0]
EX_DATA 0 L25
EX_DATA 1 L26
EX_DATA 2 M24
EX_DATA 3 M26
EX_DATA 4 N25
EX_DATA 5 N26
EX_DATA 6 P22
EX_DATA 7 P23
EX_DATA 8 P24
EX_DATA 9 P26
EX_DATA 10 R26
EX_DATA 11 R25
EX_DATA 12 R24
EX_DATA 13 T26
EX_DATA 14 T24
EX_DATA 15 U26
EXPBUS_CLK M23
TP2
EX_RD_N A23
EX_WR_N F22
EX_CS_N0 K23
EX_CS_N1 H26
TP4 J25
TP5 K24
J26
M22
L24
K26
B23
EX_DATA0 C23
EX_DATA1 A24
EX_DATA2 G21
EX_DATA3 A25
EX_DATA4 C24
EX_DATA5 A26
EX_DATA6 D24
EX_DATA7 C25
EX_DATA8 J21
EX_DATA9 B26
EX_DATA10 E24
EX_DATA11 H22
EX_DATA12 G23
EX_DATA13 C26
EX_DATA14 F24
EX_DATA15 E25
EX_CLK J22
EX_RD_N D26
EX_WR_N H23
EX_CS_N0 E26
EX_CS_N1 G25
EX_CS_N2 F26
EX_CS_N3 G26
EX_CS_N4 J24
EX_CS_N5 T22
EX_CS_N6 U23
EX_CS_N7 U24
EX_IOWAITN V26
EX_ADDR0 D22
EX_ADDR1
EX_ADDR2
EX_ADDR3
EX_ADDR4
EX_ADDR5
EX_ADDR6
EX_ADDR7
EX_ADDR8
EX_ADDR9
EX_ADDR10
EX_ADDR11
EX_ADDR12
EX_ADDR13
EX_ADDR14
EX_ADDR15
EX_ADDR16
EX_ADDR17
EX_ADDR18
EX_ADDR19
EX_ADDR20
EX_ADDR21
EX_ADDR22
EX_ADDR23
EX_HRDY0
EX_HRDY1
EX_HRDY2
EX_HRDY3
EX_ALE
TP1
HSS0_TCLK Y1
HSS1_TCLK W5
HSS0_TDATA U5
HSS1_TDATA AB1
HSS0_TFRAME V5
HSS1_TFRAME Y3
HSS0_RCLK Y2
HSS1_RCLK AA4
HSS0_RDATA AA1
HSS1_RDATA AB2
HSS0_RFRAME W3
HSS1_RFRAME W6
USB_DENG E21
USB_DPOS F20
IXP425

3V3
R164 10K
R176 10K
R177 10K
R179 10K

U7
EX_DATA [15:0]
A0 32
A1 28
A2 27
A3 26
A4 25
A5 24
A6 23
A7 22
A8 20
A9 19
A10 18
A11 17
A12 13
A13 12
A14 11
A15 10
A16 8
A17 7
A18 6
A19 5
A20 4
A21 3
A22 1
A23 30
A24 56
GND 48
GND 42
GND 21
DQ0 33
DQ1 35
DQ2 38
DQ3 40
DQ4 44
DQ5 46
DQ6 49
DQ7 51
DQ8 34
DQ9 36
DQ10 39
DQ11 41
DQ12 45
DQ13 47
DQ14 50
DQ15 52
CE0 14
CE1 2
CE2 29
WE_N 55
OE_N 54
RP_N 16
BYTE_N 31
VPEN_N 15
sts 53
VCCQ 43
VCC 9
VCC 37
EX_DATA 0
EX_DATA 1
EX_DATA 2
EX_DATA 3
EX_DATA 4
EX_DATA 5
EX_DATA 6
EX_DATA 7
EX_DATA 8
EX_DATA 9
EX_DATA 10
EX_DATA 11
EX_DATA 12
EX_DATA 13
EX_DATA 14
EX_DATA 15
EX_CS_N0
EX_WR_N
EX_RD_N
RESET_IN_N
R130 10K
R141 10K_DNP
C187 10u
C48 0.1uF
C46 0.1uF
C47 0.1uF
E28F128J3C

U8
EX_DATA [15:0]
EX_CS_N1
EX_WR_N
EX_RD_N
RESET_IN_N
R142 10K
R143 10K_DNP
C217 10u
C51 0.1uF
C52 0.1uF
C49 0.1uF
E28F128J3C

a 0.1uf ceramic capacitor is required across each VCC/VSS and VCCQ signal. Capacitors should be palced as close as possible to device connections

PCI_INTD_N
PCI_INTC_N
PCI_INTB_N
PCI_INTA_N

RESET_IN_N
TX_ER R207 0_DNP GPIO2
RXER1 R227 0_DNP GPIO1

UART_TXDATA1
UART_RTS_N1
UART_RXDATA1
UART_CTS_N1

U1D
Fast UART Interface
UART_TXDATA0 AD25
UART_RTS_N0 AD26
UART_RXDATA0 AC24
UART_CTS_N0 AB23
UART_TXDATA1 AA22
UART_RTS_N1 AC25
UART_RXDATA1 Y21
UART_CTS_N1 AB24
R208 0_DNP
R209 0_DNP
R242 0_DNP 10K
R239 0_DNP
R241 10K
R240 0_DNP

MII Interface
ETH_RXD10 AF6
ETH_RXD11 AB9
ETH_RXD12 AC8
ETH_RXD13 AD7
ETH_TXD10 AD6
ETH_TXD11 AA9
ETH_TXD12 AB8
ETH_TXD13 AF4
ETH_TXCLK1 AF5
ETH_COL1 AF8
ETH_RXDV1 AE6
ETH_RXCLK1 AD8
ETH_CRS1 AF7
ETH_TXEN1 AE4
ETH_MDC AD5
ETH_RXD00 AC5
ETH_RXD01 AA7
ETH_RXD02 AF1
ETH_RXD03 AE1
ETH_TXD00 AC2
ETH_TXD01 AB4
ETH_TXD02 AA5
ETH_TXD03 AB3
ETH_TXCLK0 AD1
ETH_COL0 AE3
ETH_RXDV0 AD2
ETH_RXCLK0 AB6
ETH_CRS0 AD4
GPIO0 Y22
ETH_TXEN0 Y6
ETH_MDIO AF2
RXD00 RXD01 RXD02 RXD03 TXD00 TXD01 TXD02 TXD03 TXCLK0 COL0 RXDV RXCLK0 CRS0 RXER0 TXEN0 MDIO

GPIO0 USED BY ETH_RXER0
power_dn_eth_phy
GPIO1 W21
GPIO2 AC26
GPIO3 AA24
GPIO4 AB26
GPIO5 Y24
GPIO6
GPIO7
OSC_IN
SCL V21
SDA AA26
R139 30.0
GPIO8 W23
GPIO9 V22
GPIO10 Y26
GPIO11 W25
GPIO12 W26
GPIO13 V24
GPIO14 U22
GPIO15 U25
PCI_INTD_N R140 10K
PCI_INTC_N R138 10K
PCI_INTB_N R138 10K
PCI_INTA_N R139 10K
GPIO12
PCI_RSTN
PCI_CLK
EXPBUS_CLK

3V3
R131 10K
Y5
EN VCC GND OUT
33.33MHz
C92 0.1uF
sys_osc

U_IP_AD0 AA19
U_IP_AD1 AB20
U_IP_AD2 AF24
U_IP_AD3 AF23
U_IP_AD4 AD21
U_IP_D0 AF22
U_IP_D1 AD20
U_IP_D2 AC19
U_IP_D3 AF21
U_IP_D4 AE20
U_IP_D5 AF20
U_IP_D6 AB17
U_IP_D7 AD18
UTP_I_CLK AB19
UTP_I_FCI AA18
UTP_I_FCO AE22
UTP_I_SCO AC20
U_OP_AD0 AF19
U_OP_AD1 AC17
U_OP_AD2 AE18
U_OP_AD3 AD17
U_OP_AD4 AE18
U_OP_D0 AF16
U_OP_D1 AC15
U_OP_D2 AD15
U_OP_D3 AF15
U_OP_D4 AD14
U_OP_D5 AE14
U_OP_D6 AF14
U_OP_D7 AB13
UTP_O_CLK AF17
UTP_O_FCI AC16
UTP_O_FCO AE16
UTP_O_SCO AB15
R210 10K
PCI_RSTN
RESET_IN_N COMES 10 NS LATER THAN POWER_RSTN
10K_PDN_UTP
R192 10K
R213 10K
R195 10K
R201 10K
R200 10K
TP3

TCK AF26
TDI AE24
TDO AD23
TMS AE25
TRST_N AC22
AF11
BYPASS_CLK AF13
PLL_LOCK AD12
RESET_IN_N AC13
SCN_TST_M_N AB21
HIGH_Z AE26
POWER_RST_N AD13
IXP425
Add 10K pull up R232 here

R197 10K
R198 10K
R224 10K
R232 10K
PGOOD1V3
SW PUSHBUTTON
SW1
C41 270p
C33 51p
C40 270p 5%
100V

U35
1A VCC33
1Y 6A
2A 6Y
2Y 5A
3A 5Y
3Y 4A
GND 4Y
74LVC07A
R214 10K
POWER_RST_N
RESET_IN_N
SRST_N
RESET_IN_N = SRST_N && RST_BTN && PGOOG1V3

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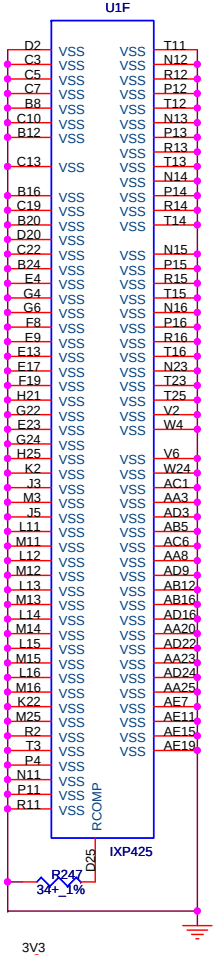
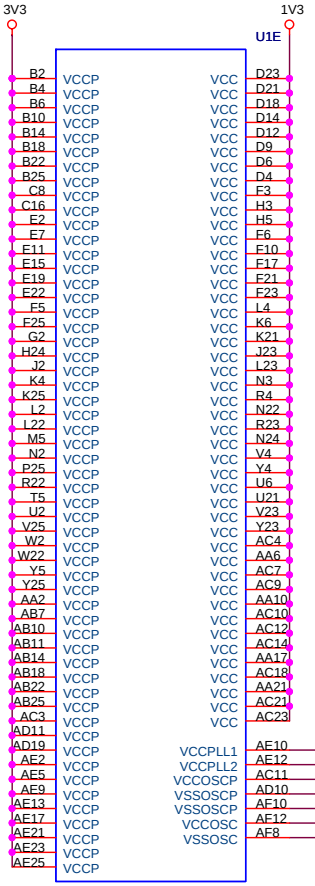
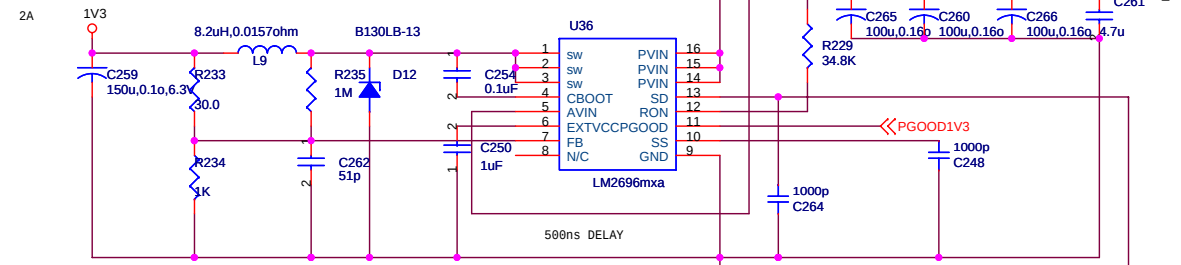
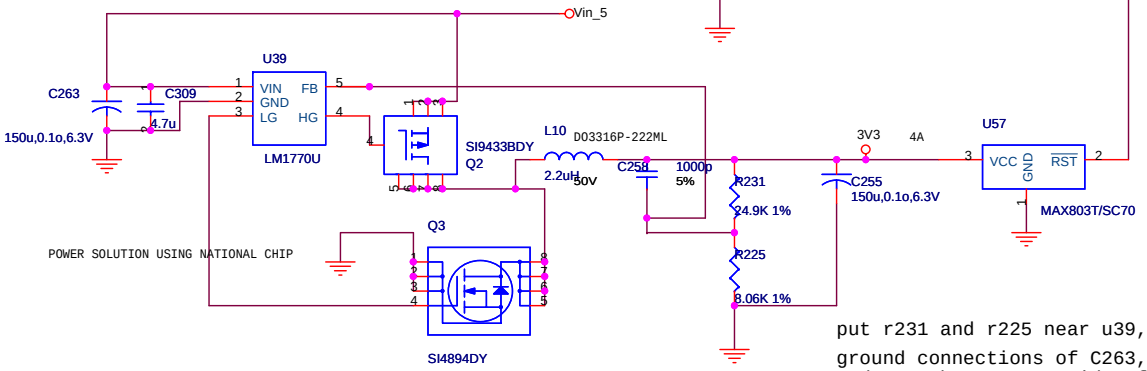
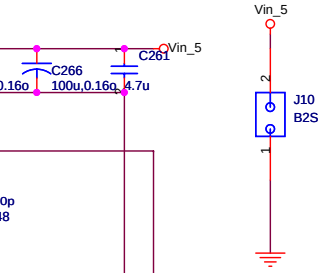
place D12 acap to U36,
place C261 acap to U36,
trace connected to U36 pin7 need to away from D12 and L9



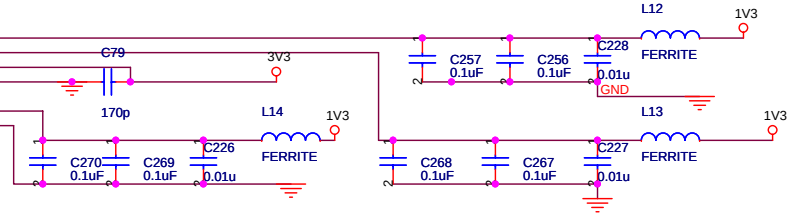




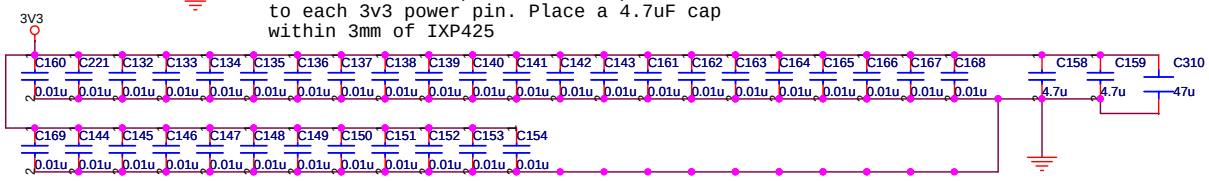


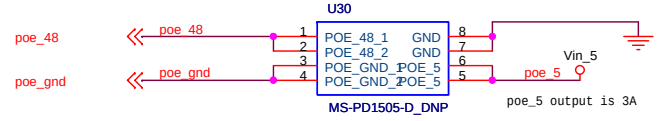


put r231 and r225 near u39,
ground connections of C263, C255, Q3 acap,
and put them on top side of the board
keep the connection node of Q2,Q3and L10 small.

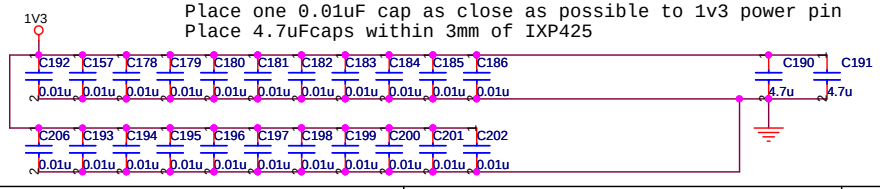


Place a 0.01uF cap as close as possible
to each 3v3 power pin. Place a 4.7uF cap
within 3mm of IXP425





CORE DECOUPLING
Place one 0.01uF cap as close as possible to 1v3 power pin
Place 4.7uFcaps within 3mm of IXP425



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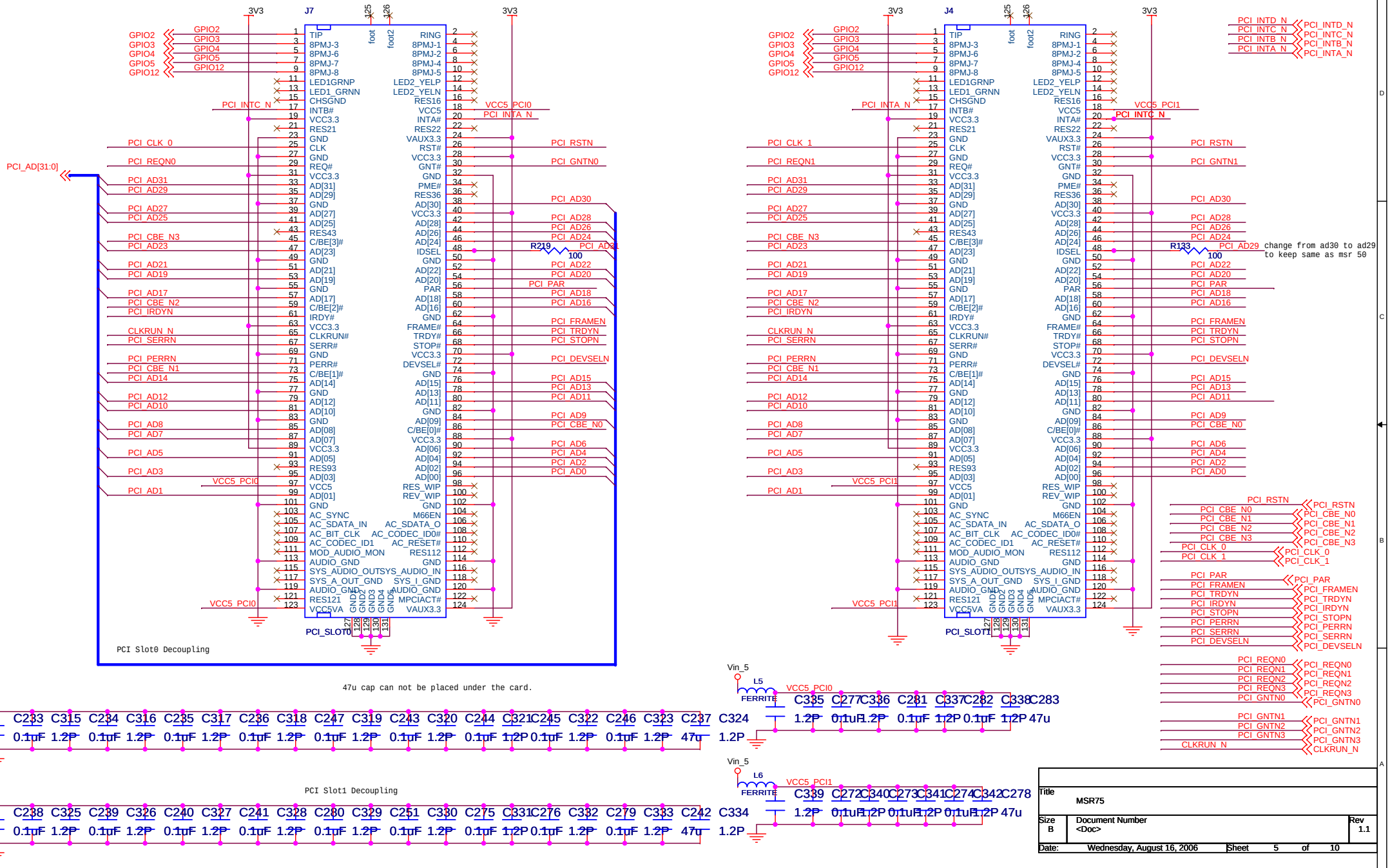
J7
J4
PCI_SLOT
3V3
GPIO2
GPIO3
GPIO4
GPIO5
GPIO12
PCI_INTC_N
PCI_INTA_N
PCI_CLK_0
PCI_CLK_1
PCI_REQN0
PCI_REQN1
PCI_AD[31:0]
PCI_RSTN
PCI_GNTN0
PCI_GNTN1
VCC5_PCI0
VCC5_PCI1
R219
R133
100
PCI_AD29 change from ad30 to ad29 to keep same as msr 50
PCI_INTD_N
PCI_INTB_N
PCI Slot0 Decoupling
47u cap can not be placed under the card.
PCI Slot1 Decoupling
Vin_5
L5
L6
FERRITE
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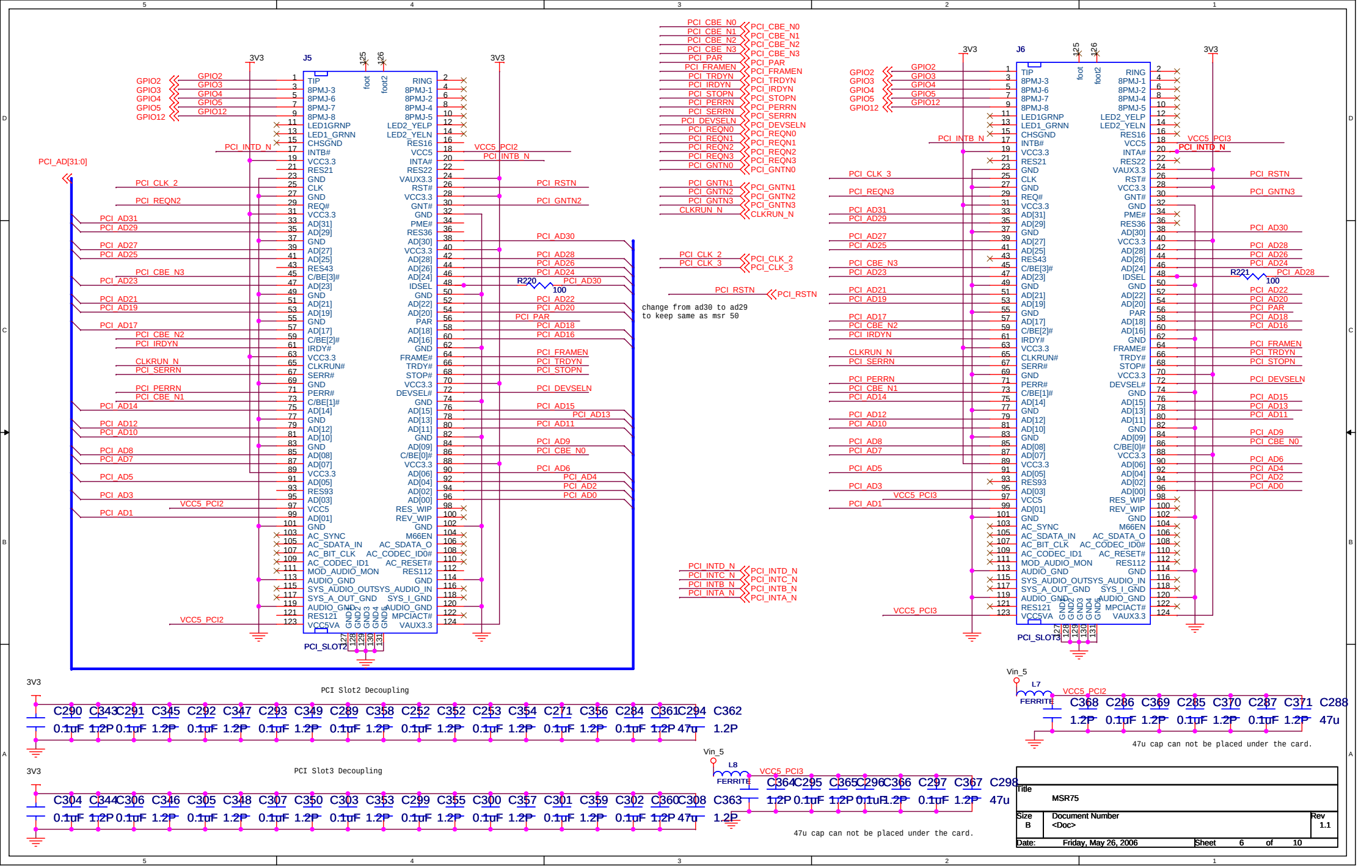
J5
PCI_SLOT2
J6
PCI_SLOT3
3V3
VCC5_PCI2
VCC5_PCI3
PCI_AD[31:0]
PCI_INTD_N
PCI_INTB_N
PCI_CLK_2
PCI_REQN2
PCI_RSTN
PCI_GNTN2
PCI_GNTN3
PCI_REQN3
PCI_CLK_3
CLKRUN_N
PCI_SERRN
PCI_PERRN
PCI_CBE_N0
PCI_CBE_N1
PCI_CBE_N2
PCI_CBE_N3
PCI_PAR
PCI_FRAMEN
PCI_TRDYN
PCI_IRDYN
PCI_STOPN
PCI_DEVSELN
R220
R221
100
change from ad30 to ad29
to keep same as msr 50
PCI Slot2 Decoupling
PCI Slot3 Decoupling
47u cap can not be placed under the card.
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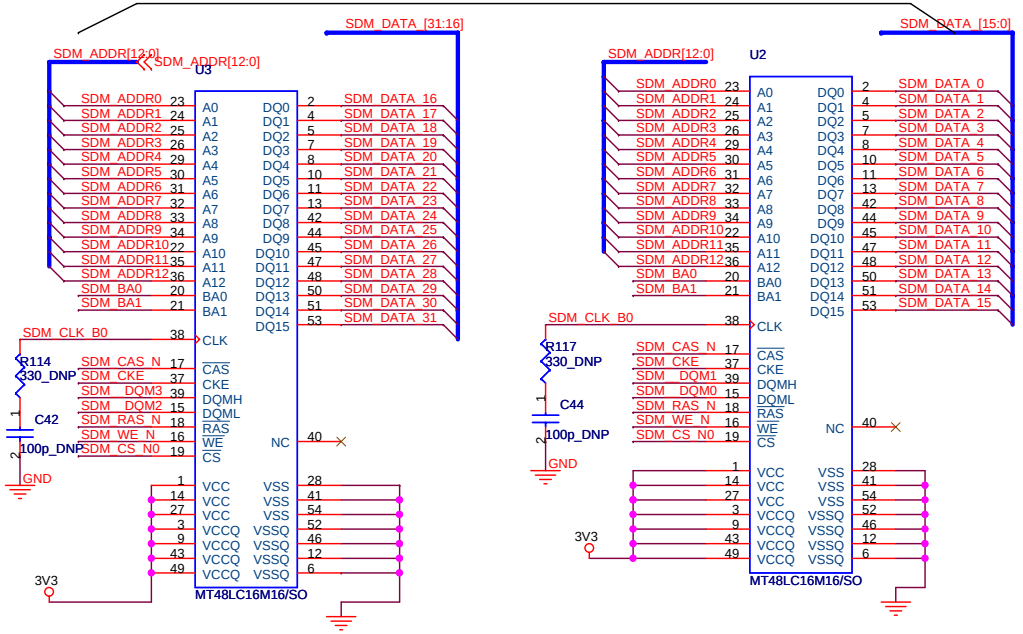
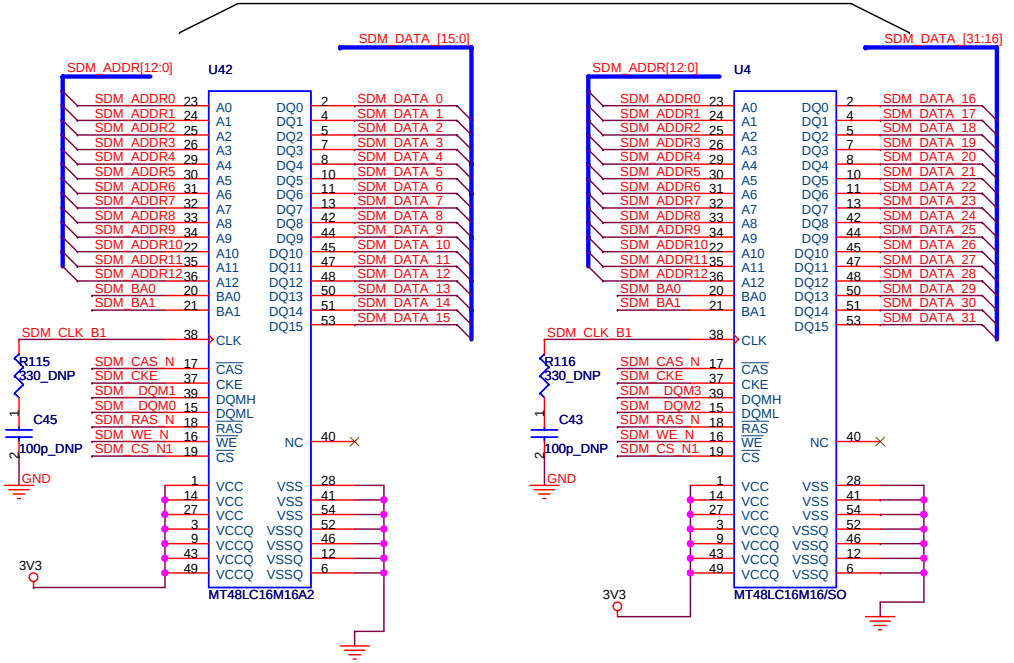
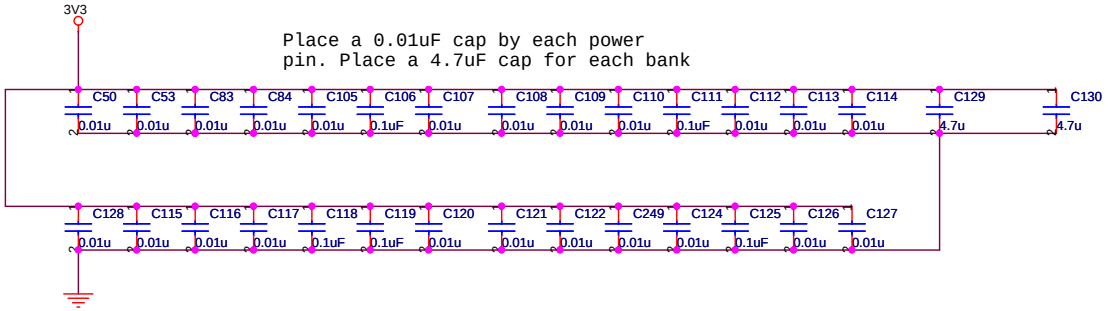
Bank0

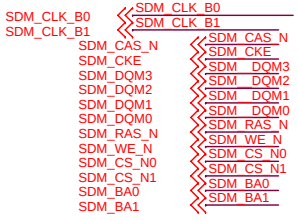


Bank1



SDM_CLK1-4
Width 5 Spacing 15 Min 0.1 Max 4





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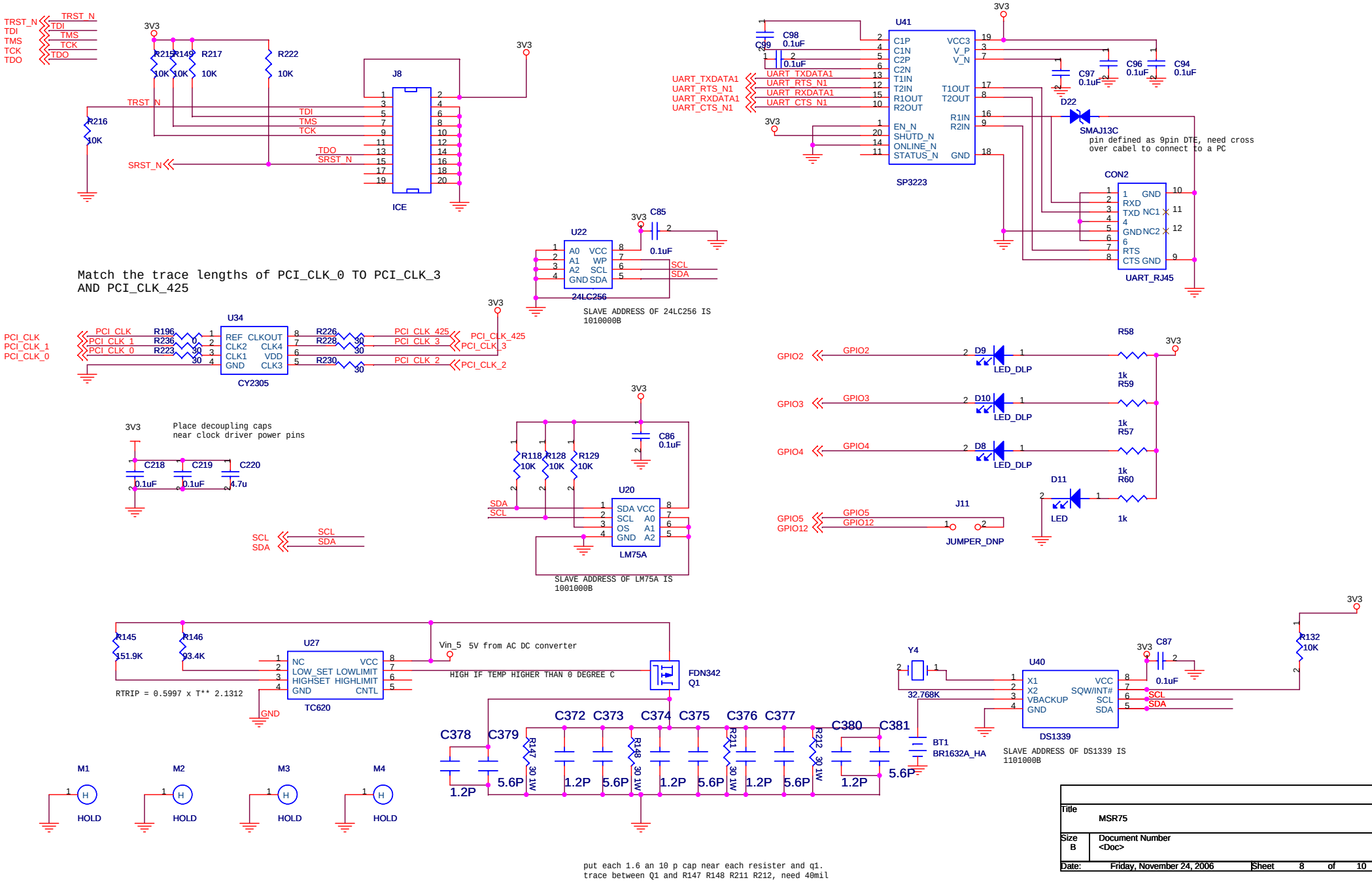
TRST_N
TDI
TMS
TCK
TDO
3V3
R215 10K
R149 10K
R217 10K
R222 10K
R216 10K
J8
ICE
SRST_N
U41
SP3223
C98 0.1uF
C99 0.1uF
C97 0.1uF
C96 0.1uF
C94 0.1uF
UART_TXDATA1
UART_RTS_N1
UART_RXDATA1
UART_CTS_N1
D22
SMAJ13C
pin defined as 9pin DTE, need cross over cabel to connect to a PC
CON2
UART_RJ45
Match the trace lengths of PCI_CLK_0 TO PCI_CLK_3
AND PCI_CLK_425
U22
24LC256
C85 0.1uF
SLAVE ADDRESS OF 24LC256 IS 1010000B
U34
CY2305
PCI_CLK
PCI_CLK_1
PCI_CLK_0
PCI_CLK_425
PCI_CLK_3
PCI_CLK_2
R196 0
R236 0
R223 30
R226 30
R228 30
R230 30
Place decoupling caps near clock driver power pins
C218 0.1uF
C219 0.1uF
C220 4.7u
C86 0.1uF
R118 10K
R128 10K
R129 10K
U20
LM75A
SLAVE ADDRESS OF LM75A IS 1001000B
SDA
SCL
R58
R59 1k
R57 1k
R60 1k
D9
D10
D8
D11
LED_DLP
LED
GPIO2
GPIO3
GPIO4
GPIO5
GPIO12
J11
JUMPER_DNP
R145 151.9K
R146 93.4K
U27
TC620
RTRIP = 0.5997 x T** 2.1312
Vin_5 5V from AC DC converter
HIGH IF TEMP HIGHER THAN 0 DEGREE C
FDN342
Q1
GND
C372 C373 C374 C375 C376 C377 C378 C379 C380 C381
R147 30 1W
R148 30 1W
R211 30 1W
R212 30 1W
1.2P
5.6P
Y4
32.768K
BT1
BR1632A_HA
U40
DS1339
SLAVE ADDRESS OF DS1339 IS 1101000B
C87 0.1uF
R132 10K
M1
M2
M3
M4
HOLD
put each 1.6 an 10 p cap near each resister and q1.
trace between Q1 and R147 R148 R211 R212, need 40mil
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Keep transmit and receive pairs (RX+- & TX+-) away from each other. or On difference side of the board

put r13 , r8, r6 near to u5

c10 c25 close to u5

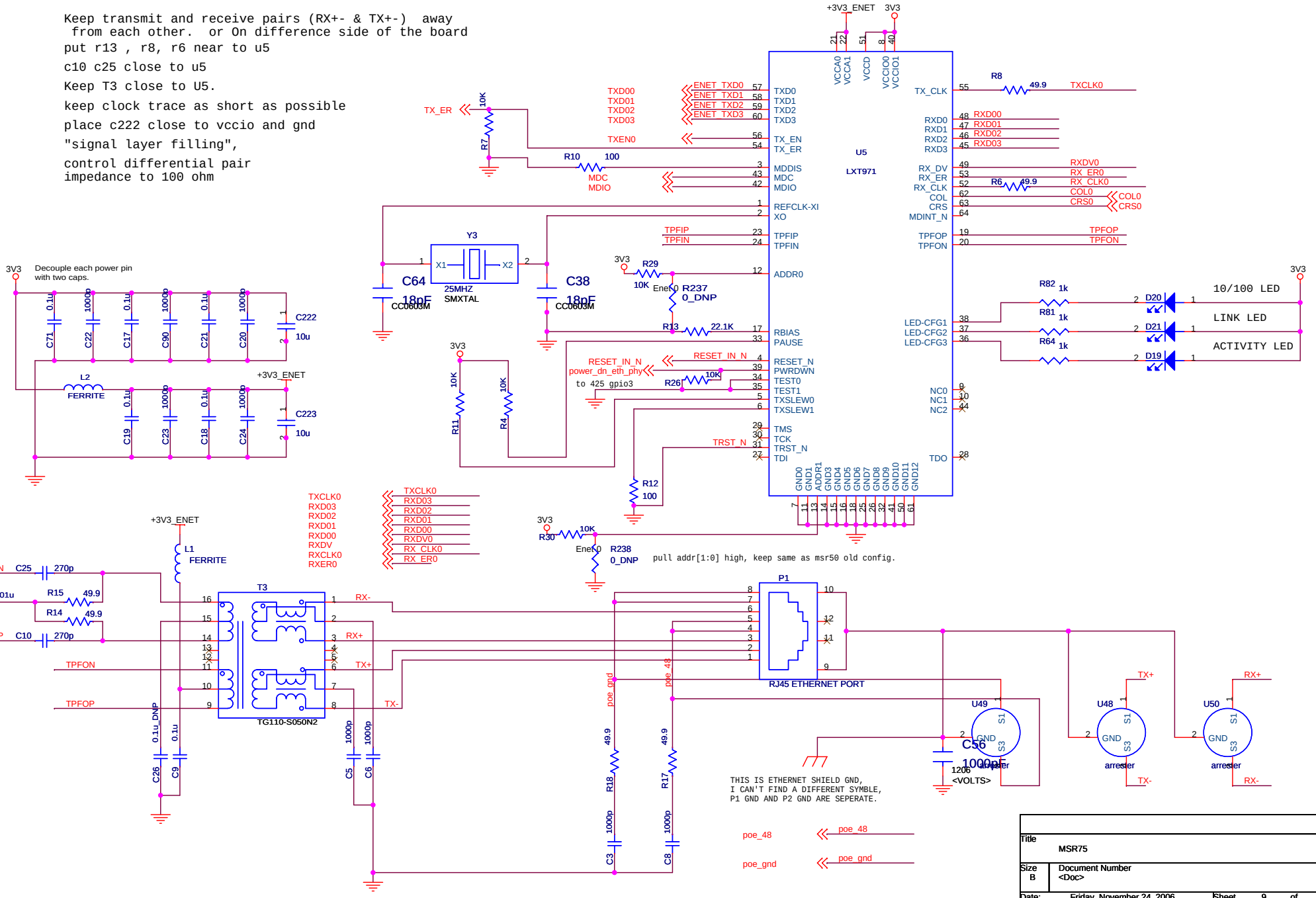
Keep T3 close to U5.

keep clock trace as short as possible

place c222 close to vccio and gnd

"signal layer filling",

control differential pair impedance to 100 ohm



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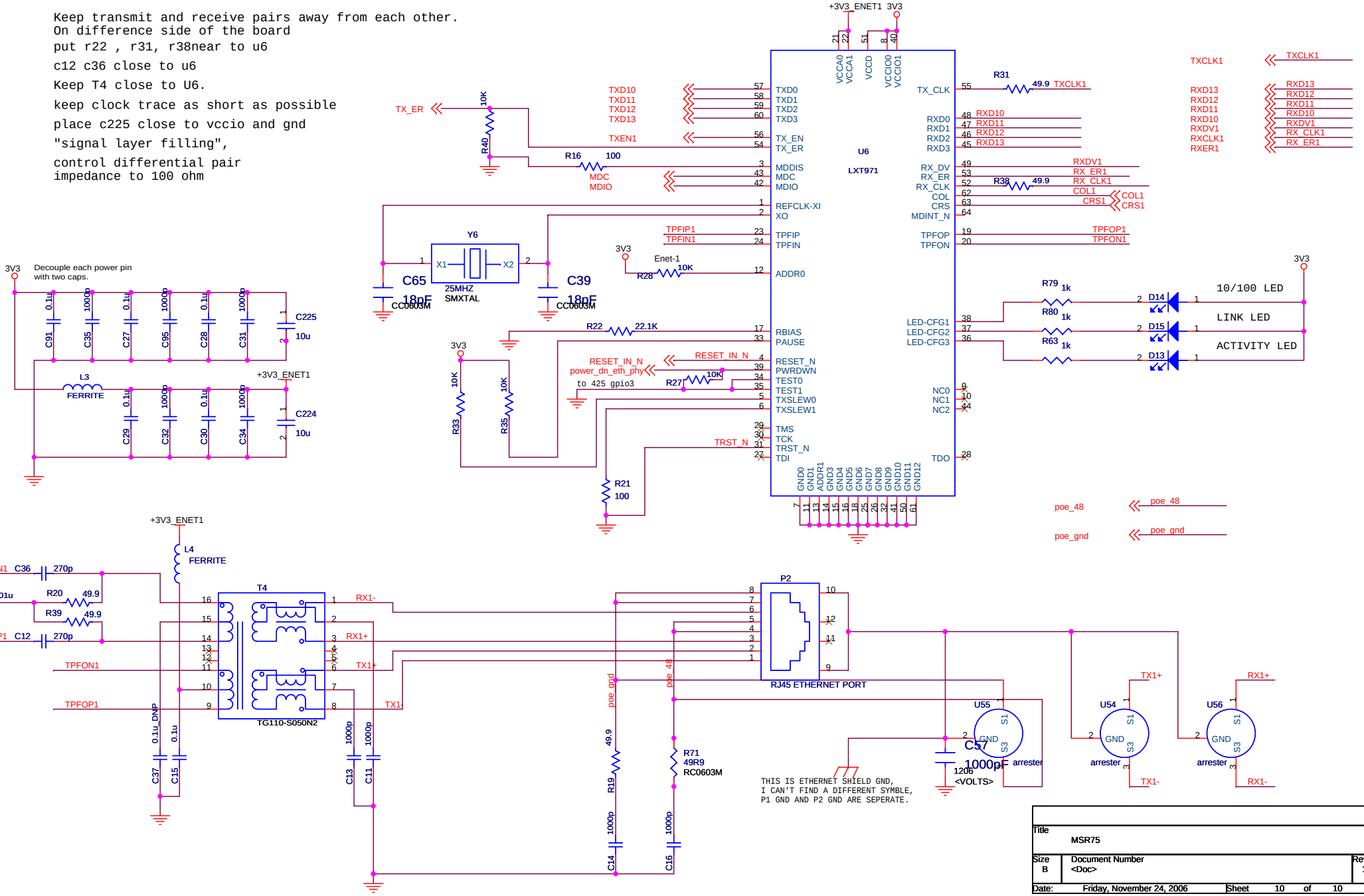
Keep transmit and receive pairs away from each other.
On difference side of the board
put r22 , r31, r38near to u6
c12 c36 close to u6
Keep T4 close to U6.
keep clock trace as short as possible
place c225 close to vccio and gnd
"signal layer filling",
control differential pair
impedance to 100 ohm



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