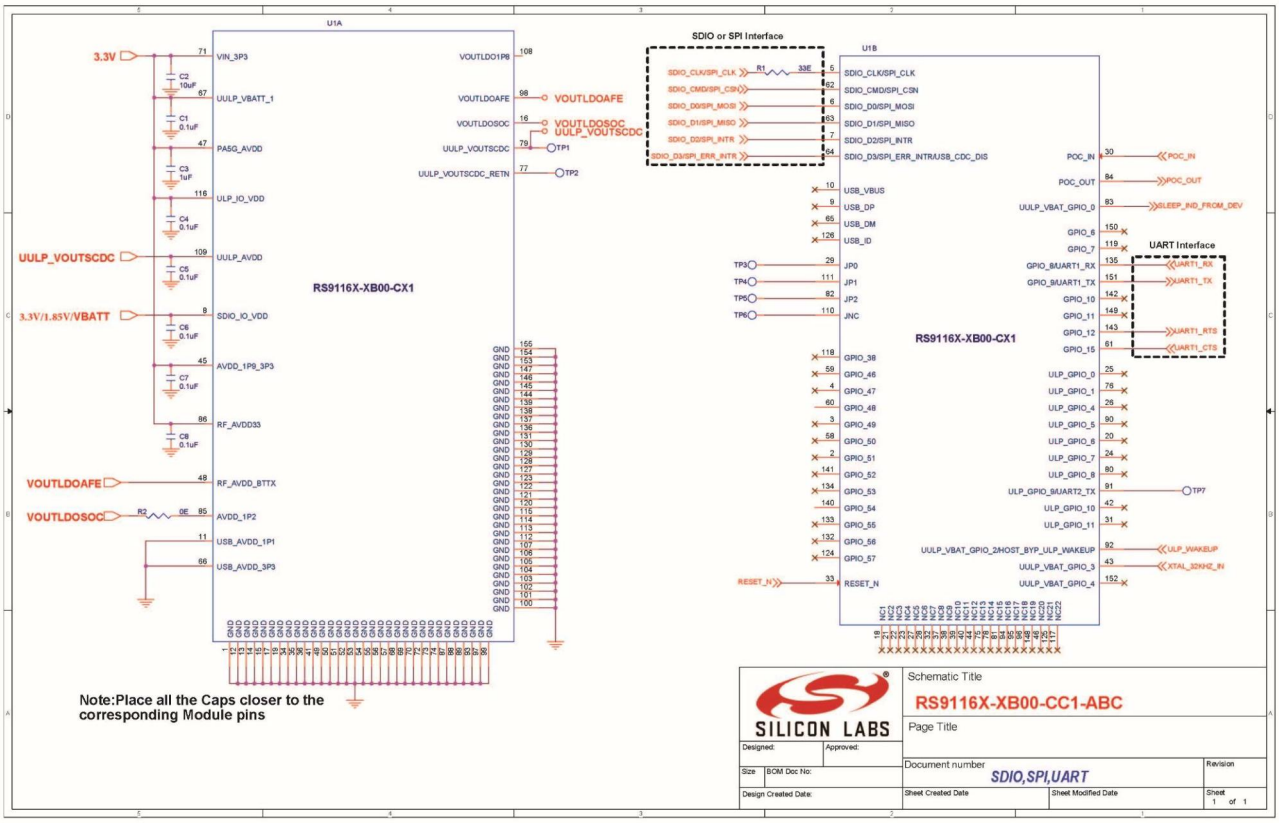

Figure 16. Schematics with SDIO/SPI/UART Host Interface