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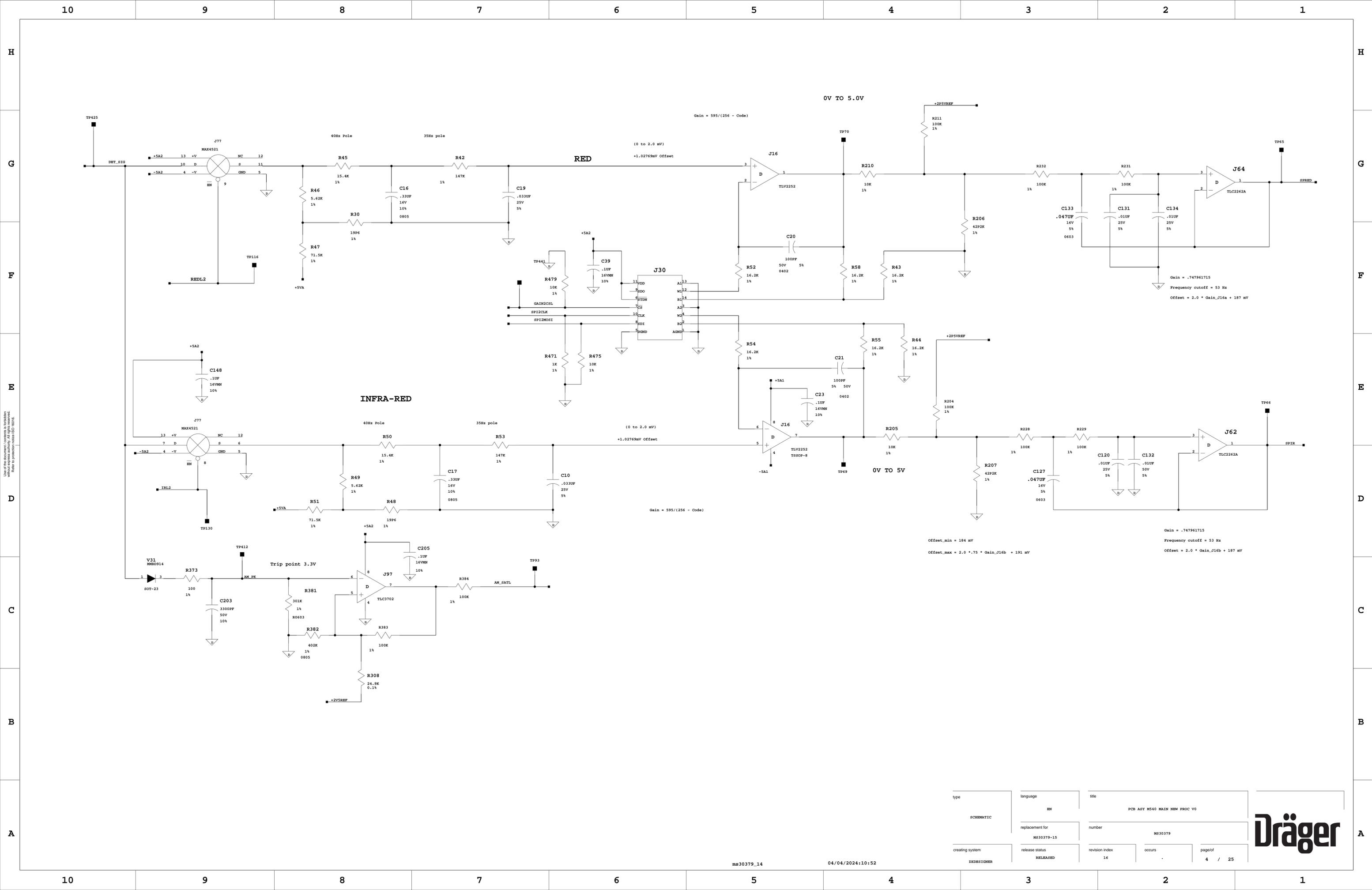
A

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REVISION HISTORY	
REV 00	REPLACE THE FXA255 WITH THE FXA166 AND OTHER OBSOLETE PARTS
REV 01	UPDATED PCB FOR DFM FROM JABIL - PROTOTYPE 1 DOCUMENTATION
REV 02	UPDATED SCHEMATIC WITH FIXES FROM PROTOTYPE 1 - SEE M540 CHANGES DOC FOR ALL CHANGES
REV 03	UPDATED SCHEMATIC WITH FIXES FROM PROTOTYPE 2 - SEE M540 CHANGES DOC FOR ALL CHANGES
REV 04	UPDATED SCHEMATIC WITH FIXES FROM PROTOTYPE 3 - SEE M540 CHANGES DOC FOR ALL CHANGES
REV 05	UPDATED SCHEMATIC WITH FIXES FROM PROTOTYPE 4 - SEE M540 CHANGES DOC FOR ALL CHANGES
REV 06	UPDATED SCHEMATIC WITH FIXES FROM PROTOTYPE 5 - SEE M540 CHANGES DOC FOR ALL CHANGES
REV 07	UPDATED J43 AND J44 FOOTPRINTS, ADDED CUSTOM STANDOFFS
REV 08	UPDATED ASSEMBLY DWG AND FAB DWG - NO SCHEMATIC OR BOM CHANGES
REV 09	UPDATED PRE-PROGRAMMED FLASH FILE ONLY
REV 10	UP-REV FOR TRACEABILITY ONLY Change to Diagnostic Application for Type 1 Display Field Issue
REV 11	UP-REV FOR OPTICAL LENS PART NUMBER CHANGES
REV 12	TRACK NEW V6 FIRMWARE FOR SUB FLASH / REVERT TO REV 10 OPT. LENSES
REV 13	REMOVE CONNECTION AT Y4 ENABLE PIN TO "MRL" NET. Y4.1 IS N/C
REV 14	UP-REV FOR OPTICAL LENS PART NUMBER CHANGES
REV 15	Changed J14 from 7490324 to 1801275
REV 16	Changed J14 from 1801275 back to 7490324

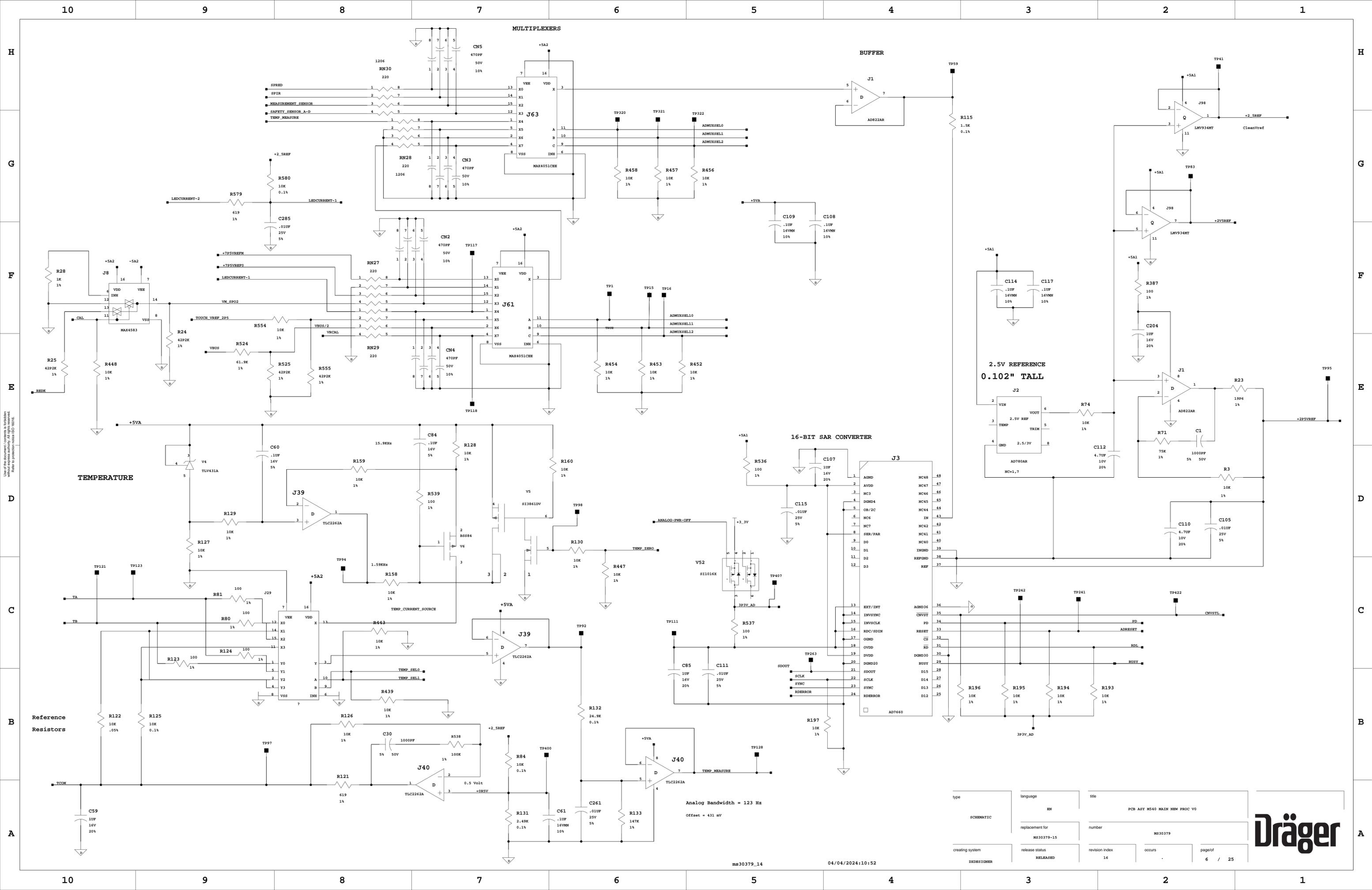
scale	general tolerances	material	safety class
field reserved	revision text	Changed J14 from 1801275 back to 7490324	
revision text	(.)		
author	approved	contract	
date	See Aras	See Aras	
name	PCB ASY M540 MAIN NEW PROC V0		
language	EN	number	M530379
replacement for	M530379-15	revision index	16
creating system	DXDESIGNER	release status	RELEASED
revision index	16	occurs	page / of
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TEMPERATURE

Reference Resistors

MULTIPLEXERS

BUFFER

16-BIT SAR CONVERTER

2.5V REFERENCE

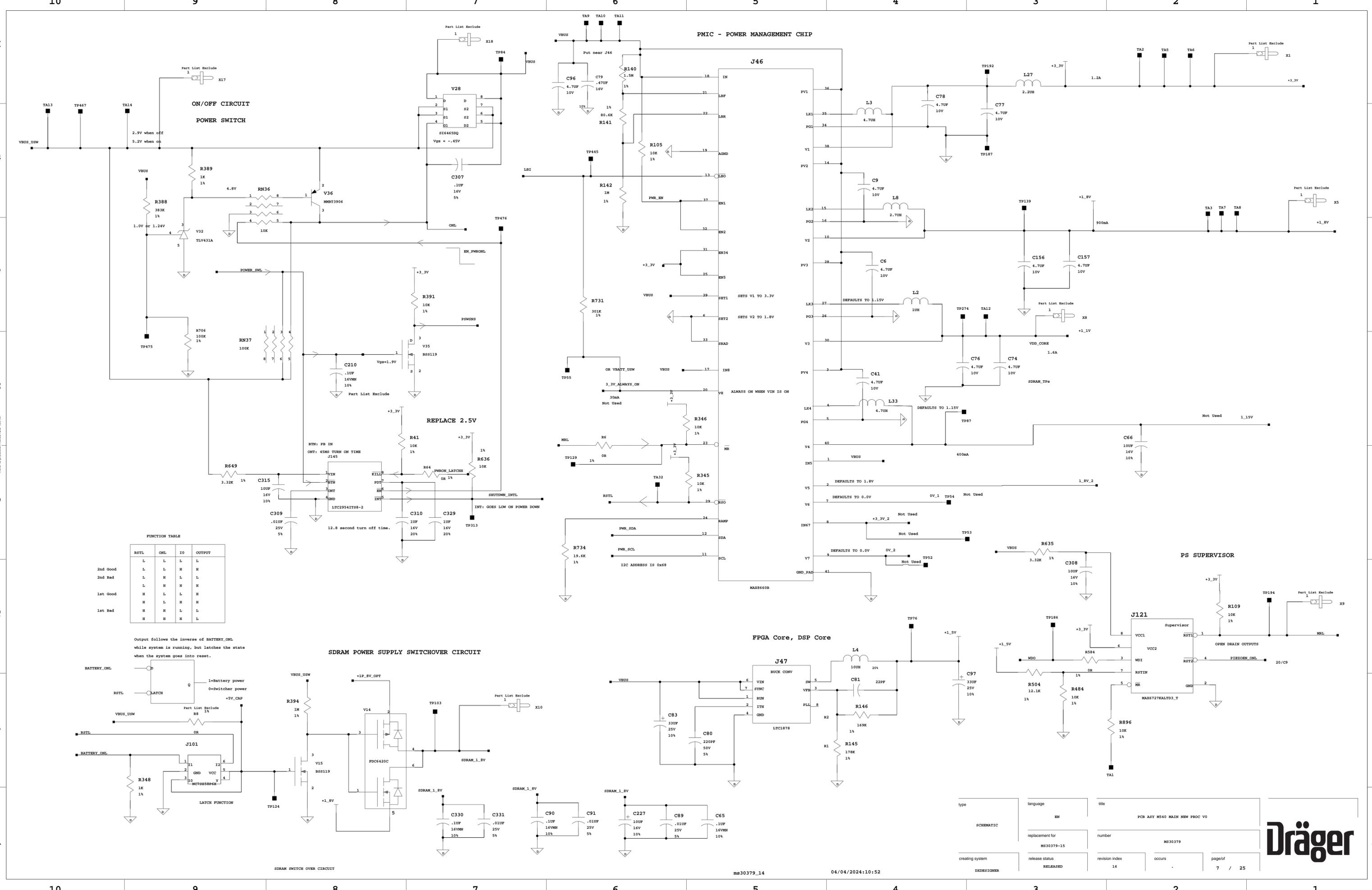
0.102" TALL

Analog Bandwidth = 123 Hz

Offset = 431 mV

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SCHMATIC	EN	PCB ASY MS40 MAIN NEW PROC V0
creating system	release status	number
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FUNCTION TABLE

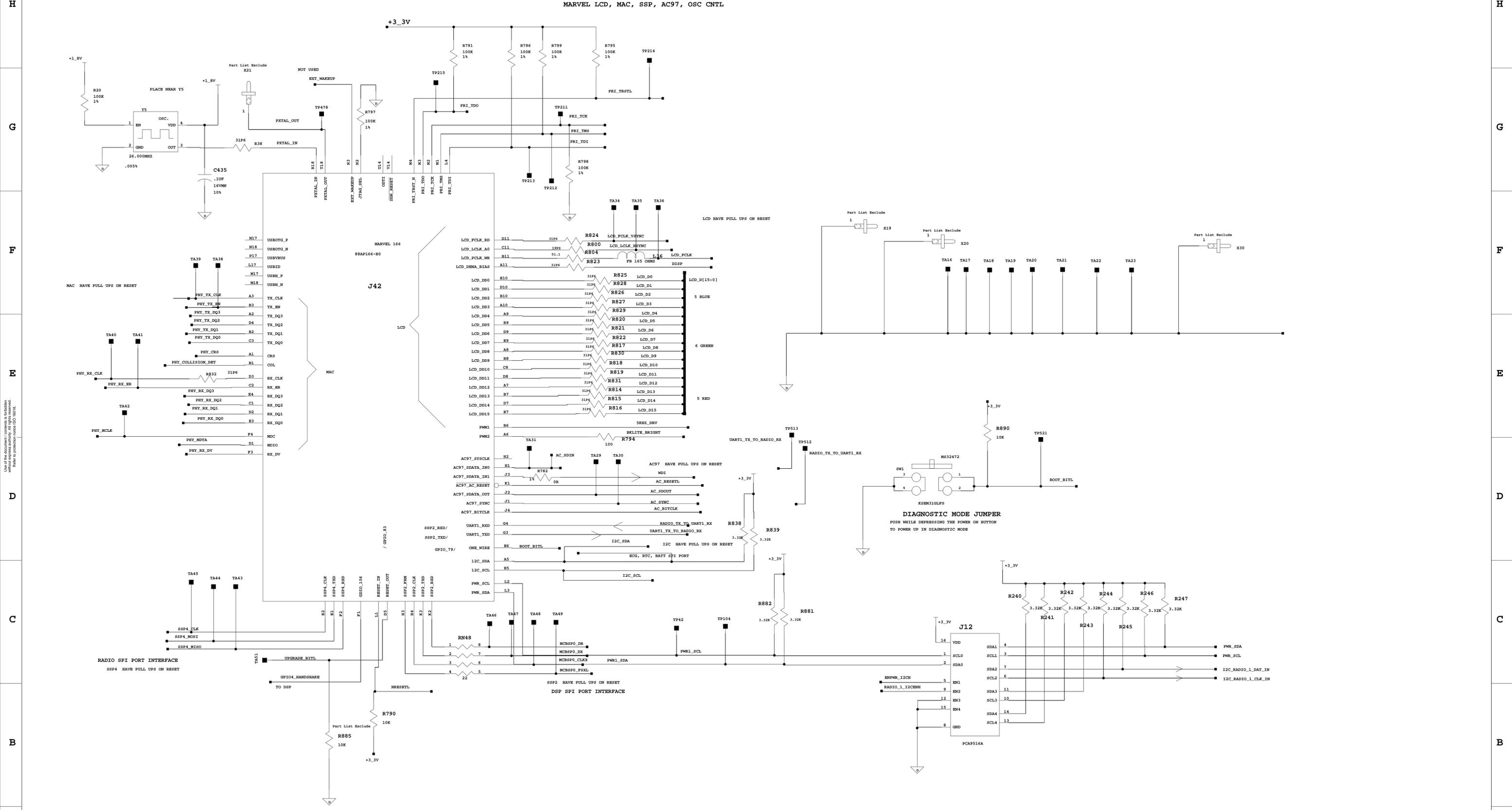
	RSTL	ONL	IO	OUTPUT
2nd Good	L	L	L	L
2nd Bad	L	L	H	H
1st Good	L	H	L	L
1st Bad	L	H	H	H
	H	L	L	H
	H	L	H	H
	H	H	L	L
	H	H	H	L

Output follows the inverse of BATTERY_ONL while system is running, but latches the state when the system goes into reset.

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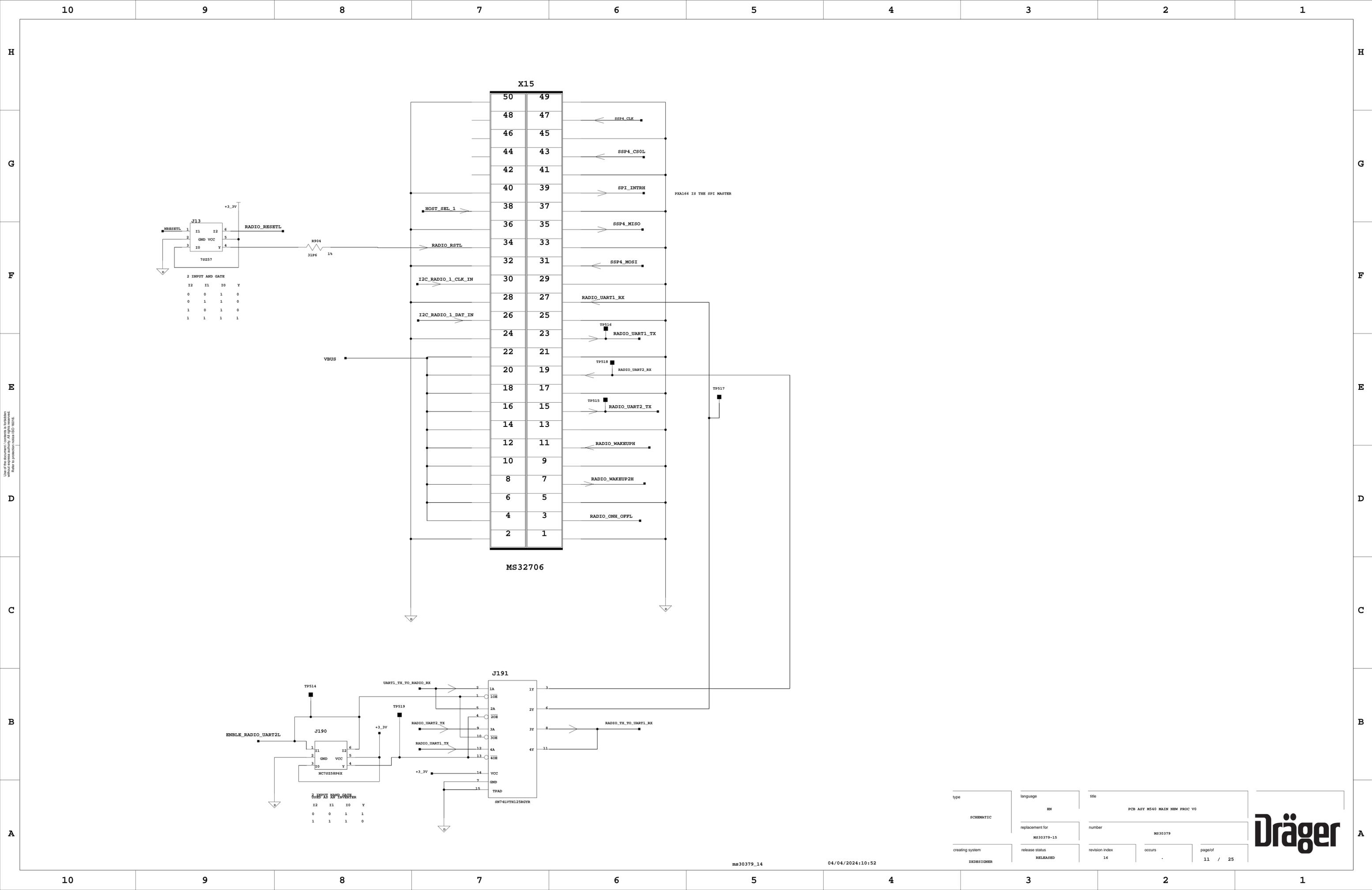


MARVEL LCD, MAC, SSP, AC97, OSC CNTL



type	language	title	
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creating system	release status	number	revision index
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75257

2 INPUT AND GATE

I2	I1	I0	Y
0	0	1	0
0	1	1	0
1	0	1	0
1	1	1	1

NCT75258PEX

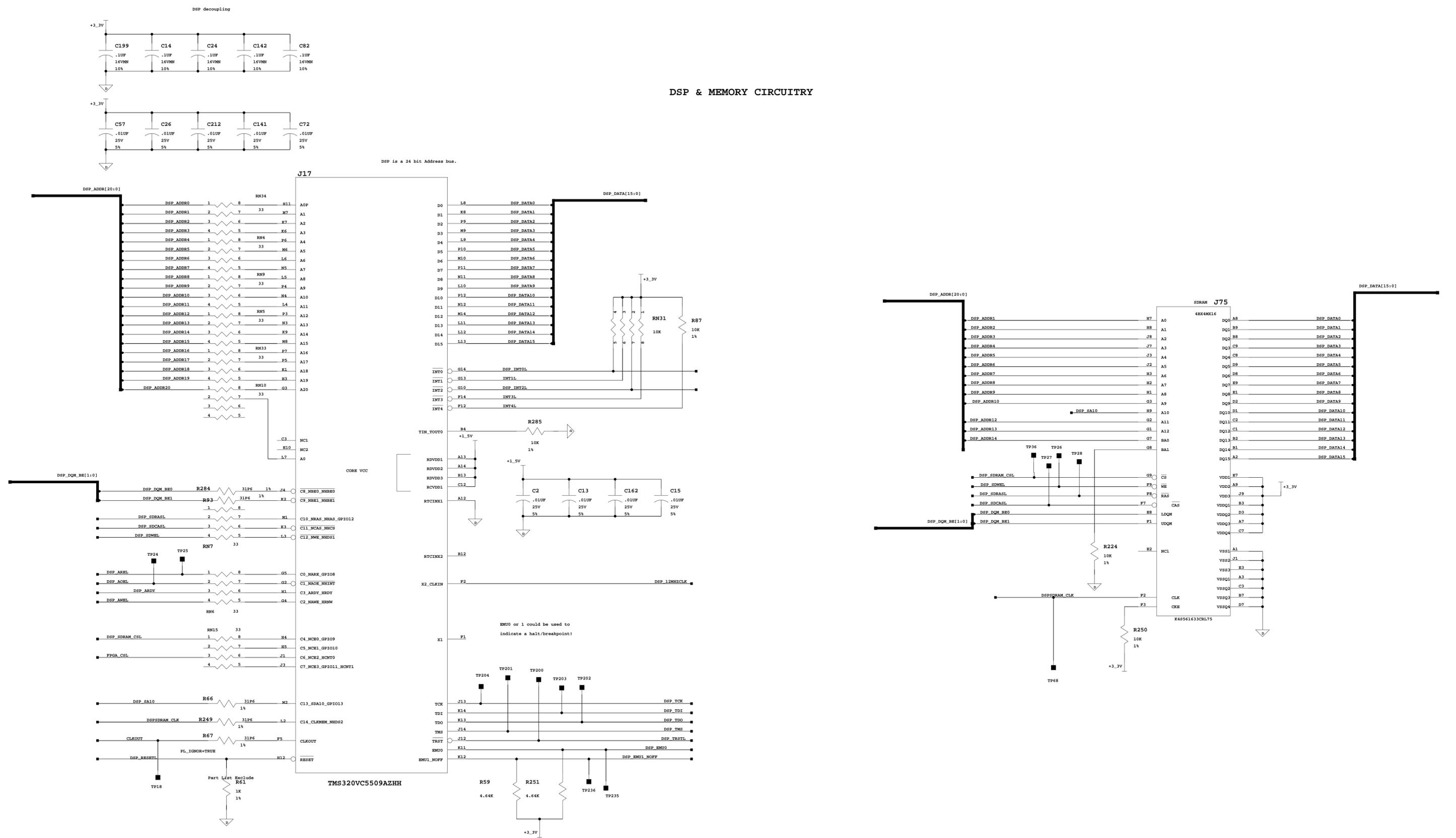
2 INPUT AND GATE

I2	I1	I0	Y
0	0	1	1
1	1	1	0

type	language	title	
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DSP & MEMORY CIRCUITRY



type	language	title	
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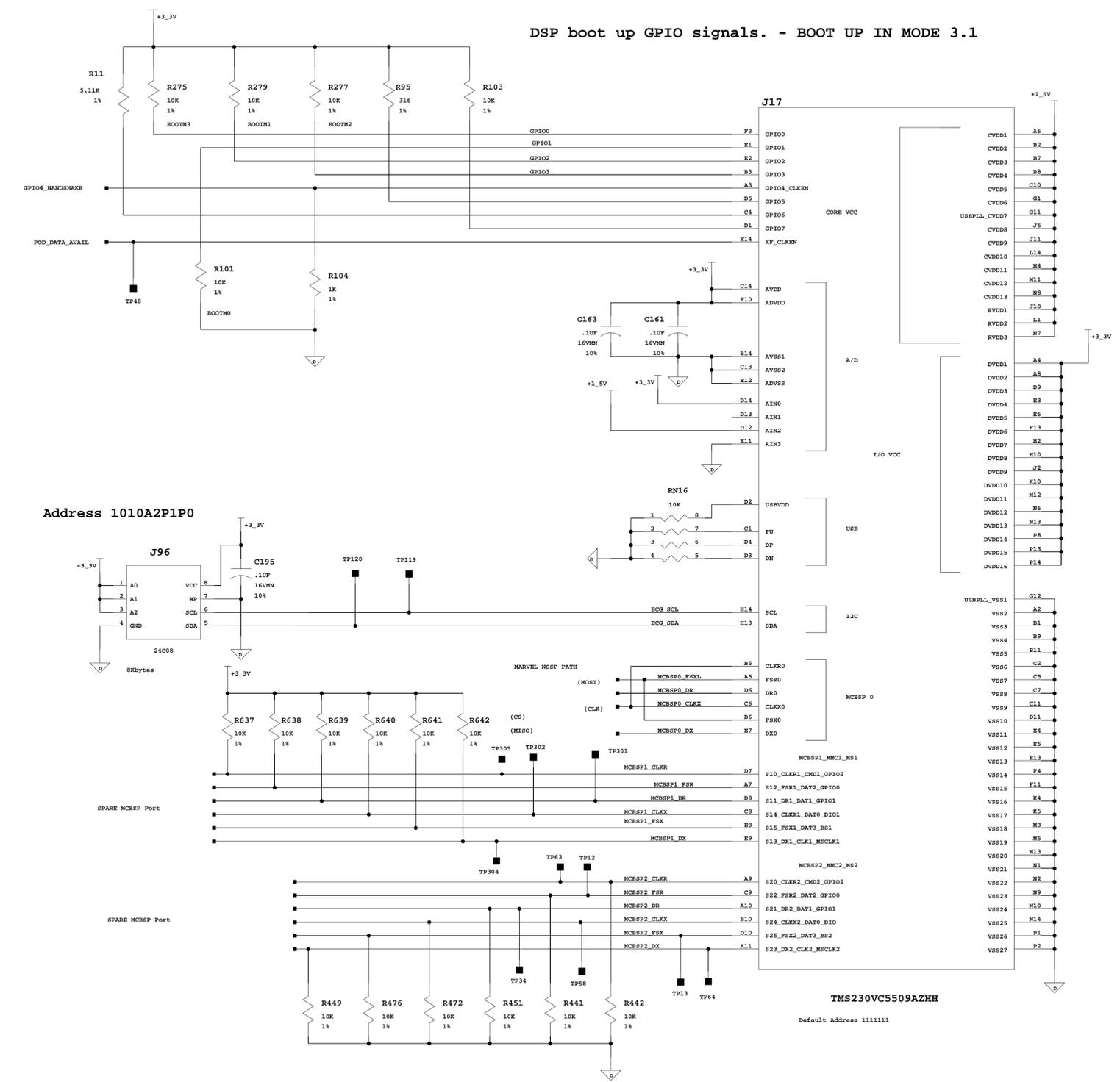


Refer to Table 3-3 for boot configurations page 27 of the Hardware Manual.

BOOTM3	BOOTM0
0000	SPI Boot 24 bit Address, MCRSP0
0010	USB Boot
0101	EMPI Boot Multiplexed mode
0110	EMPI Boot non-multiplexed mode
1000	Boot from 16 bit Ext. Async Memory
1001	SPI Boot 16 bit Address, MCRSP0
1010	Parallel EMIF Boot, 8 bit Memory
1011	Parallel EMIF Boot, 16 bit Memory
1100	Boot from 8 bit Ext. Async Memory
1110	Serial Boot 16 bit data, MCRSP0
1111	Serial Boot 8 bit data, MCRSP0

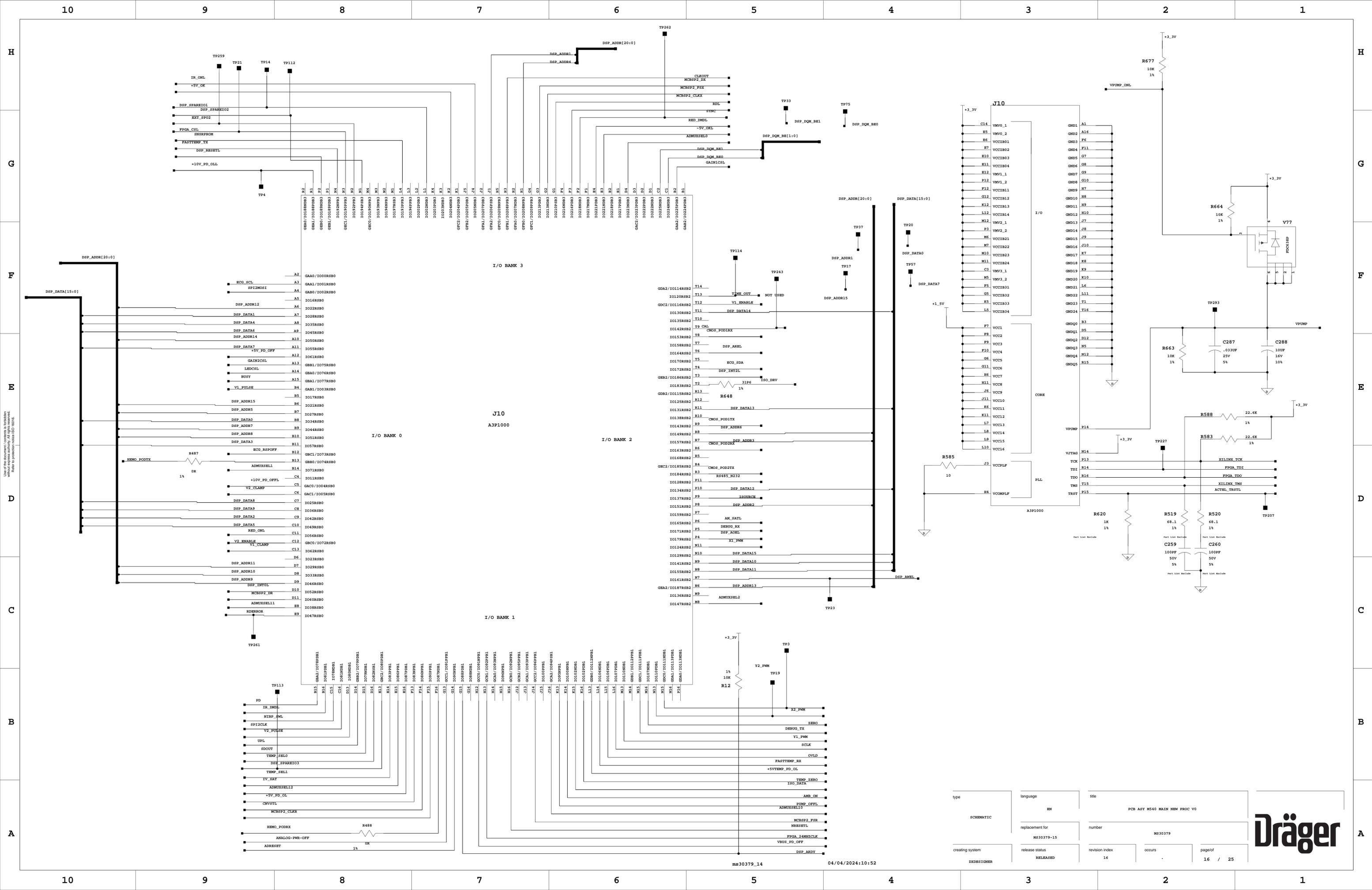
All other combinations are RESERVED.

DSP boot up GPIO signals. - BOOT UP IN MODE 3.1



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creating system	release status	number
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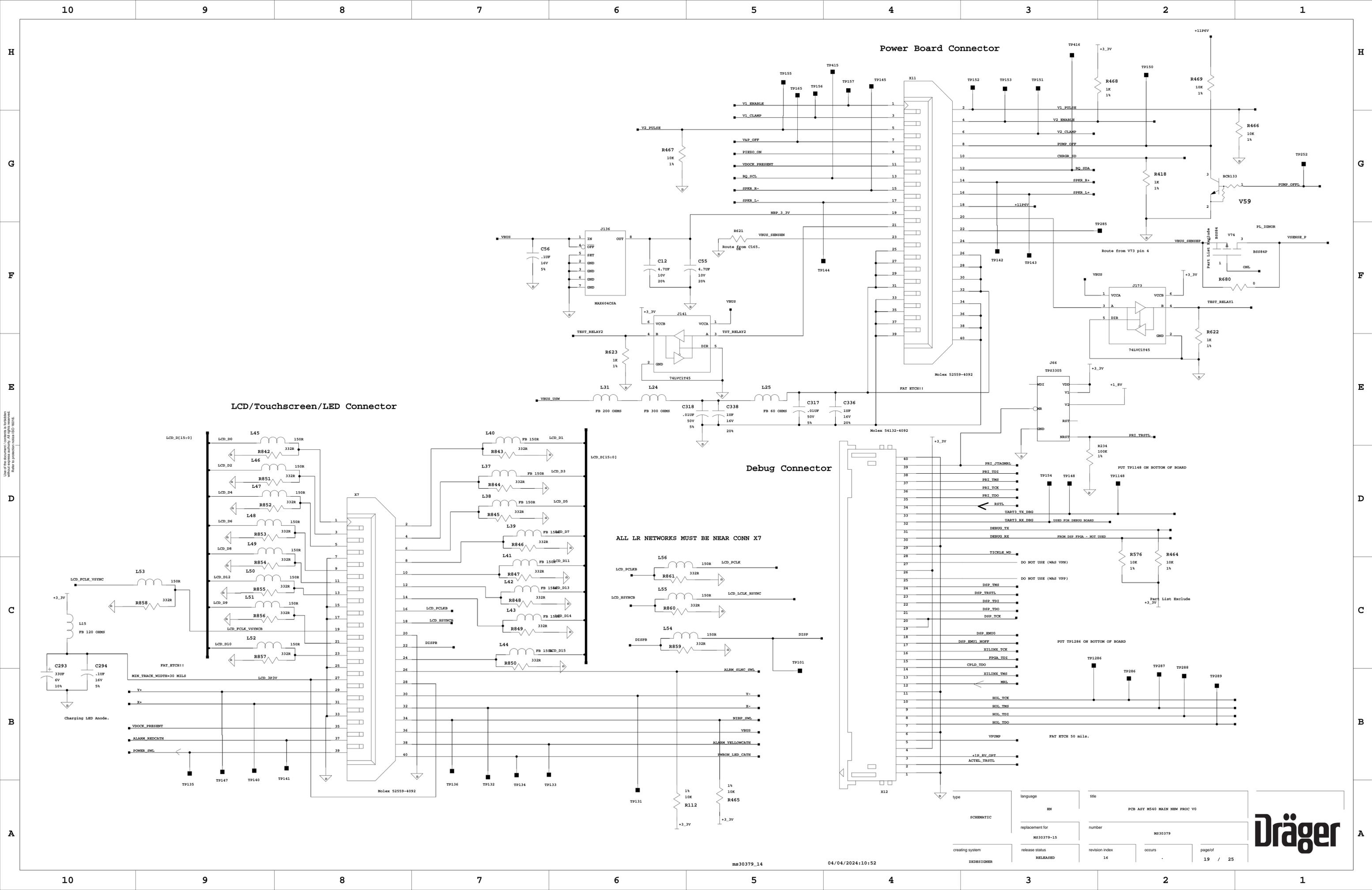




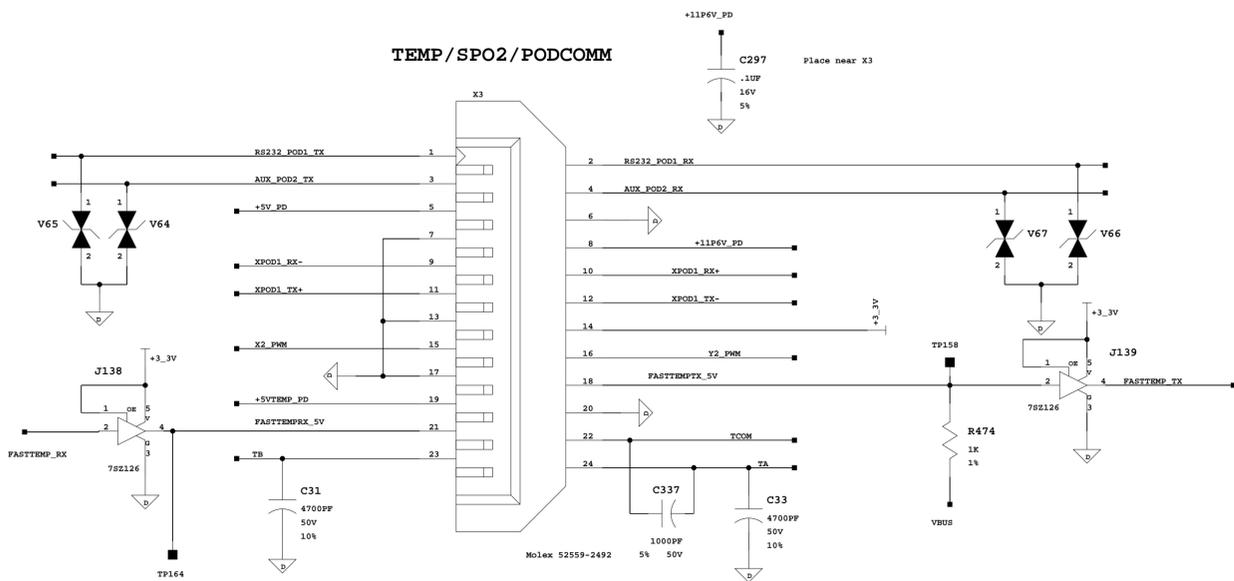
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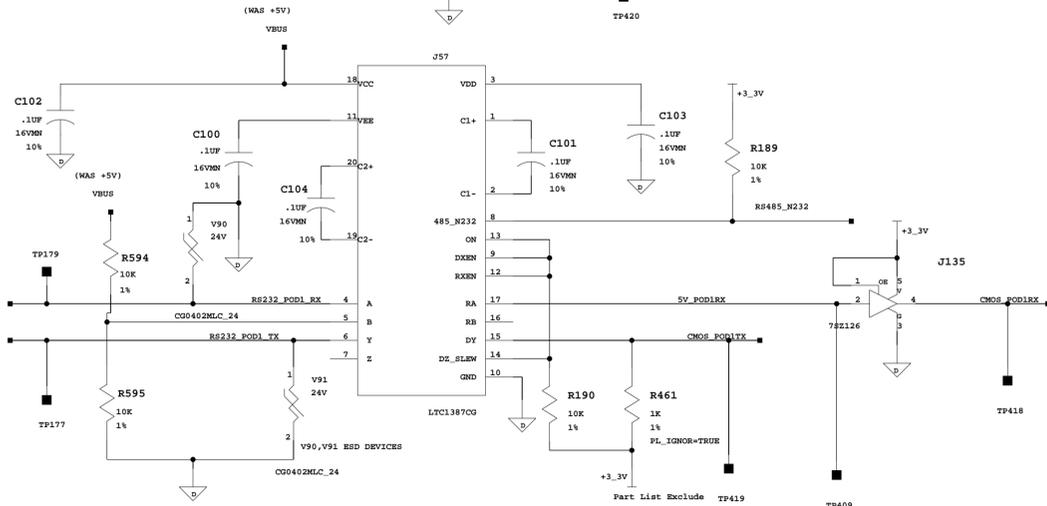
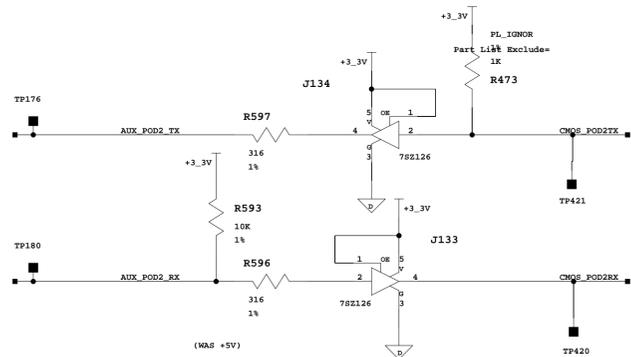




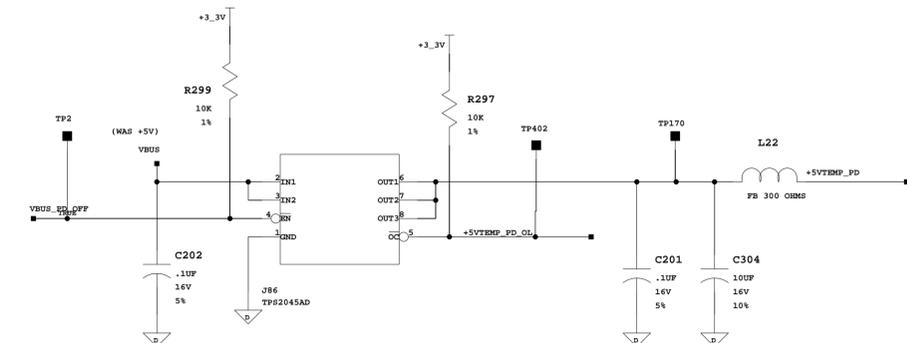
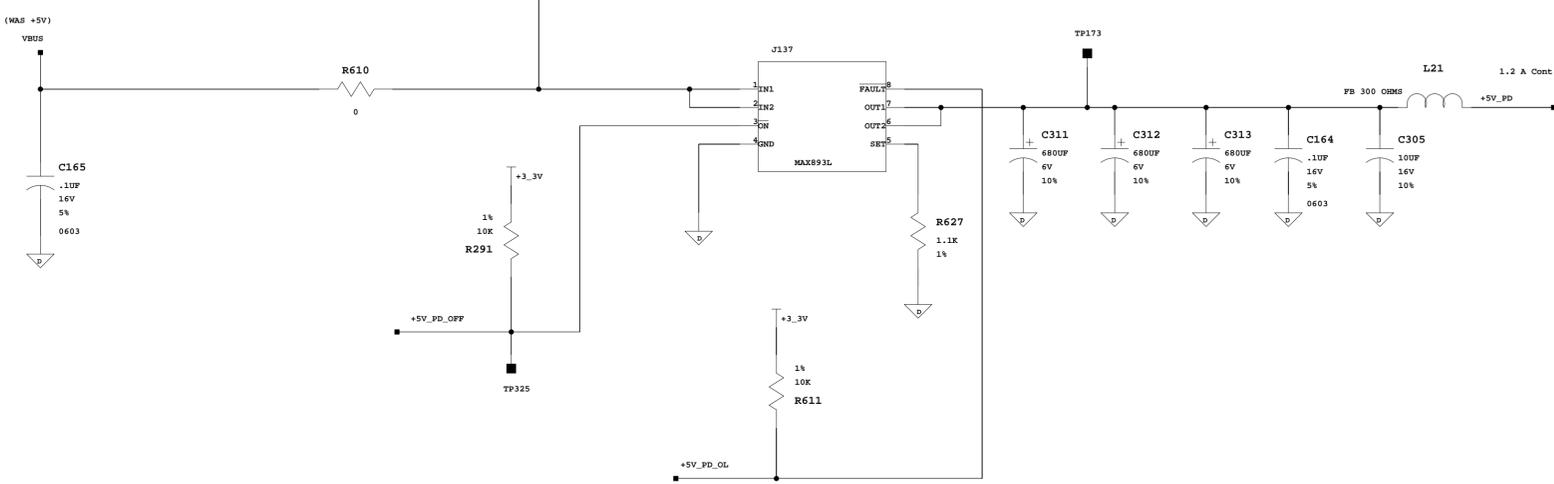
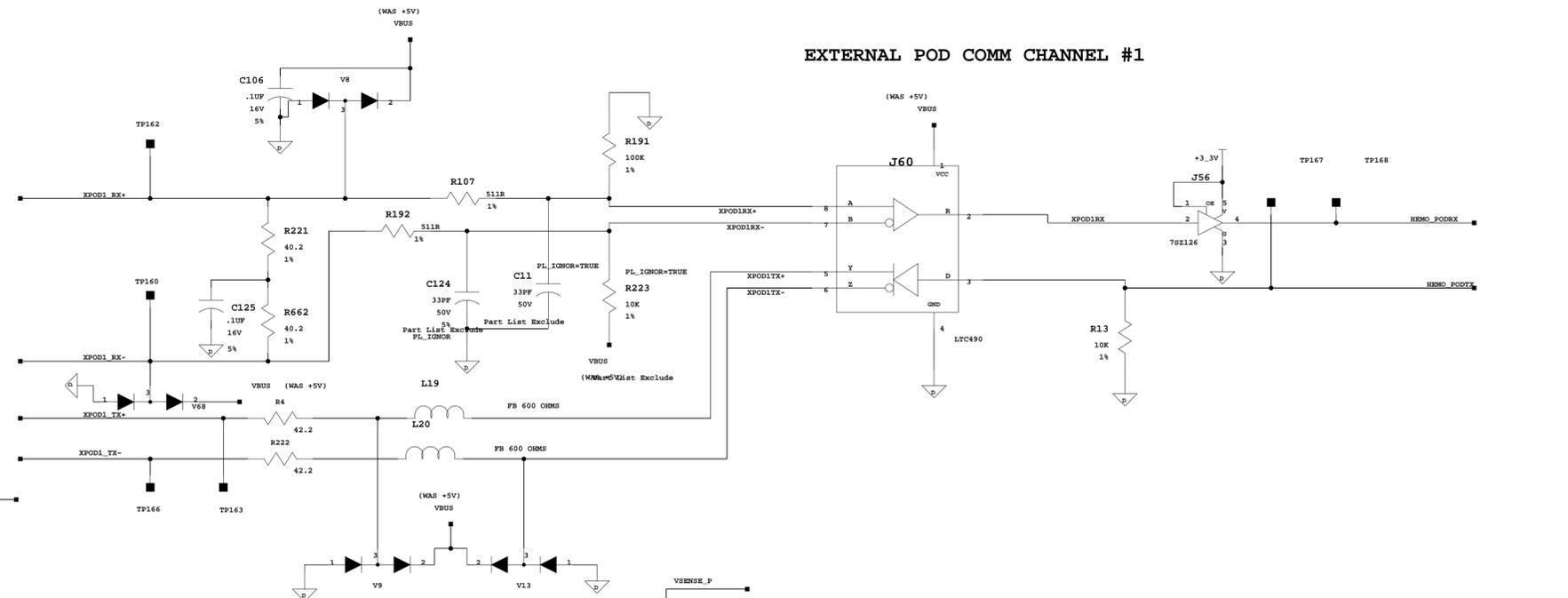
TEMP/SPO2/PODCOMM



AUX POD COMM



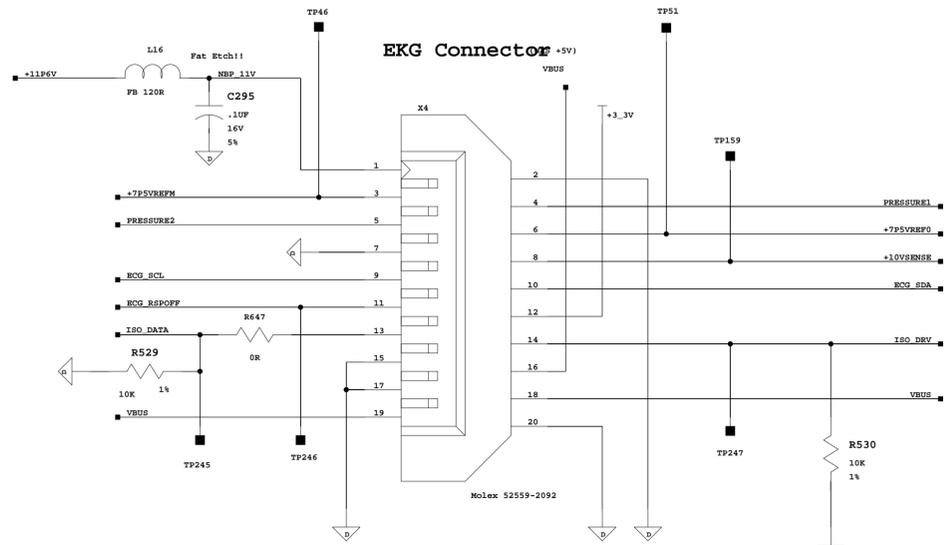
EXTERNAL POD COMM CHANNEL #1



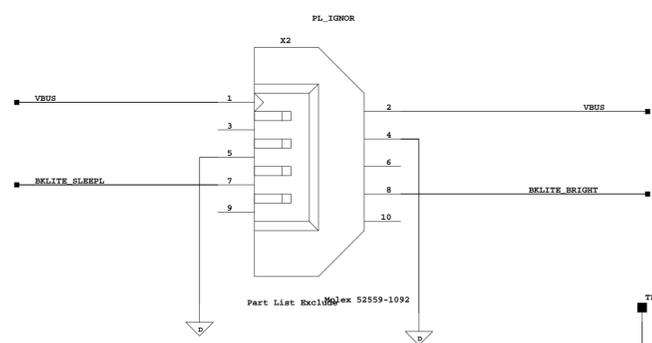
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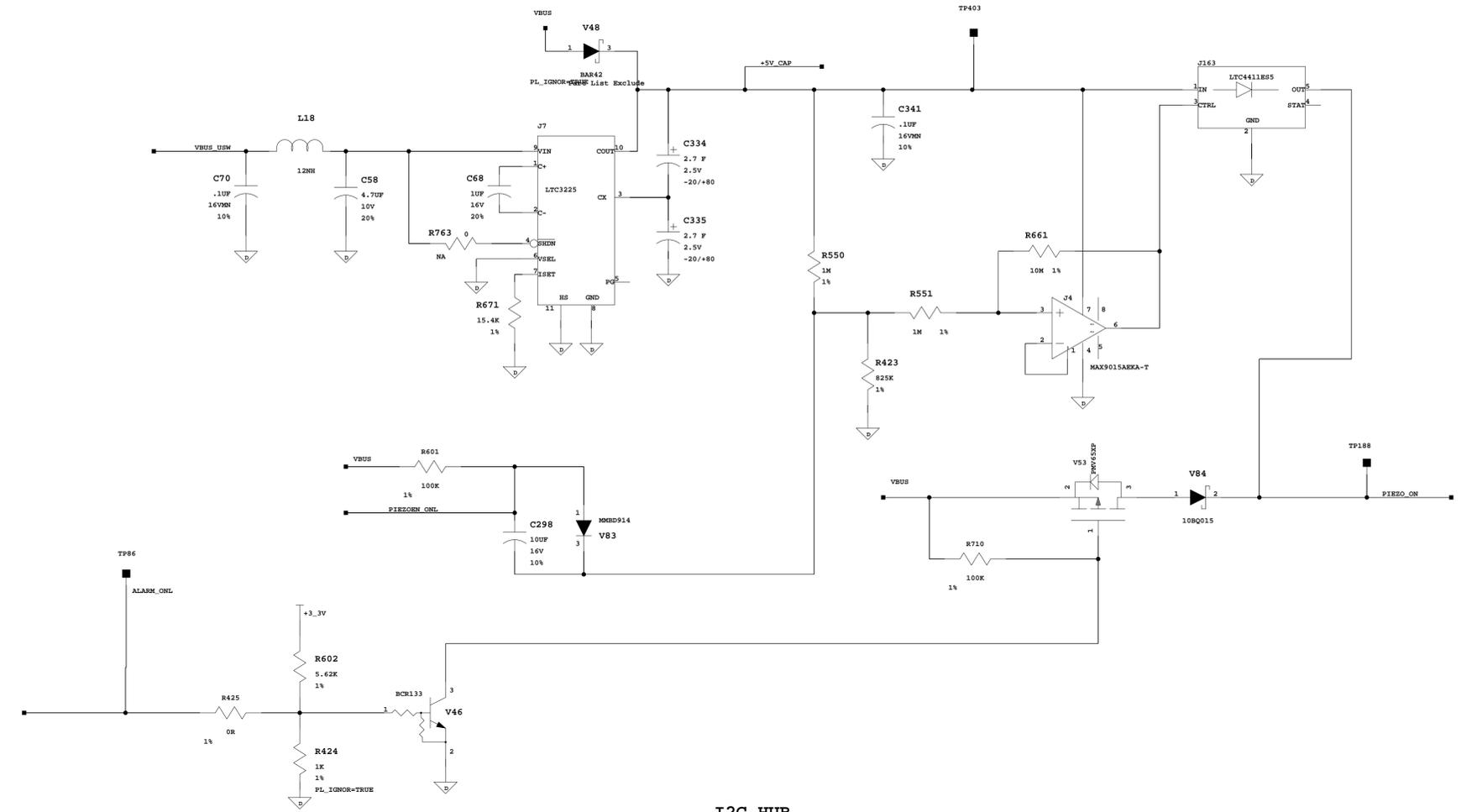
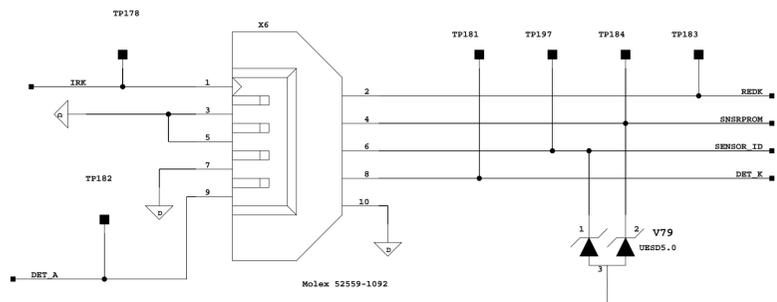
POWER FAIL ALARM



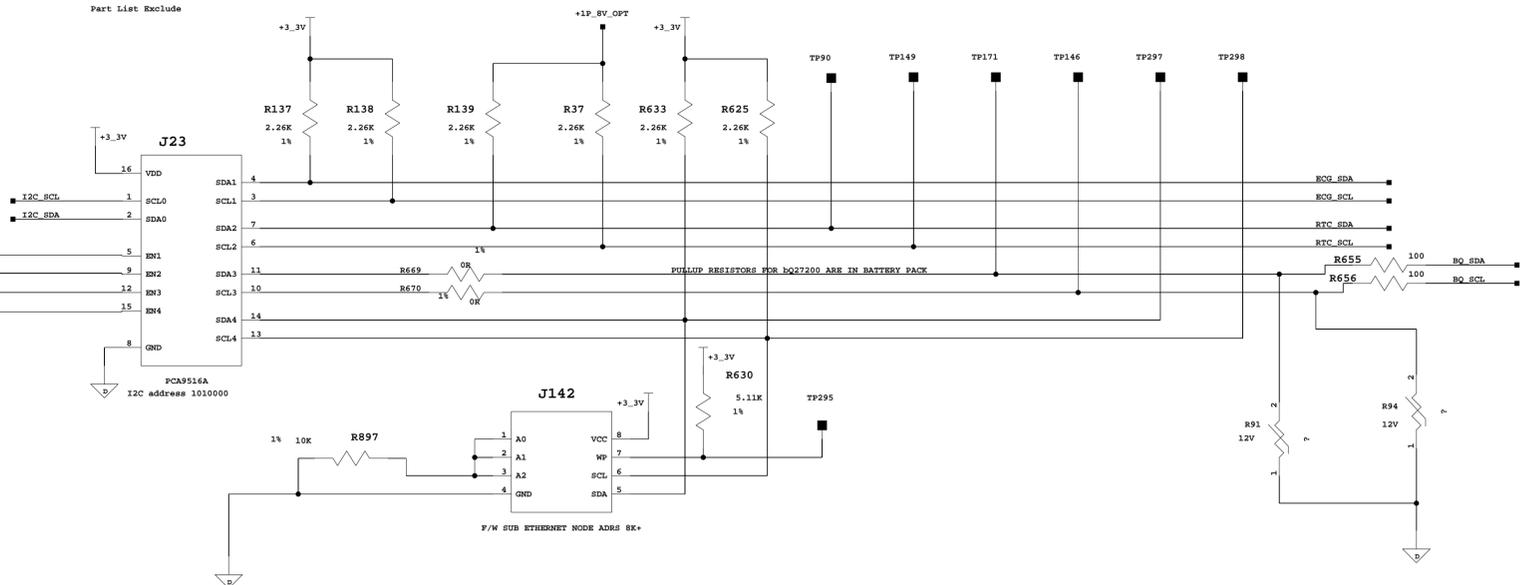
Backlight Inverter Connector



SPO2 Connector

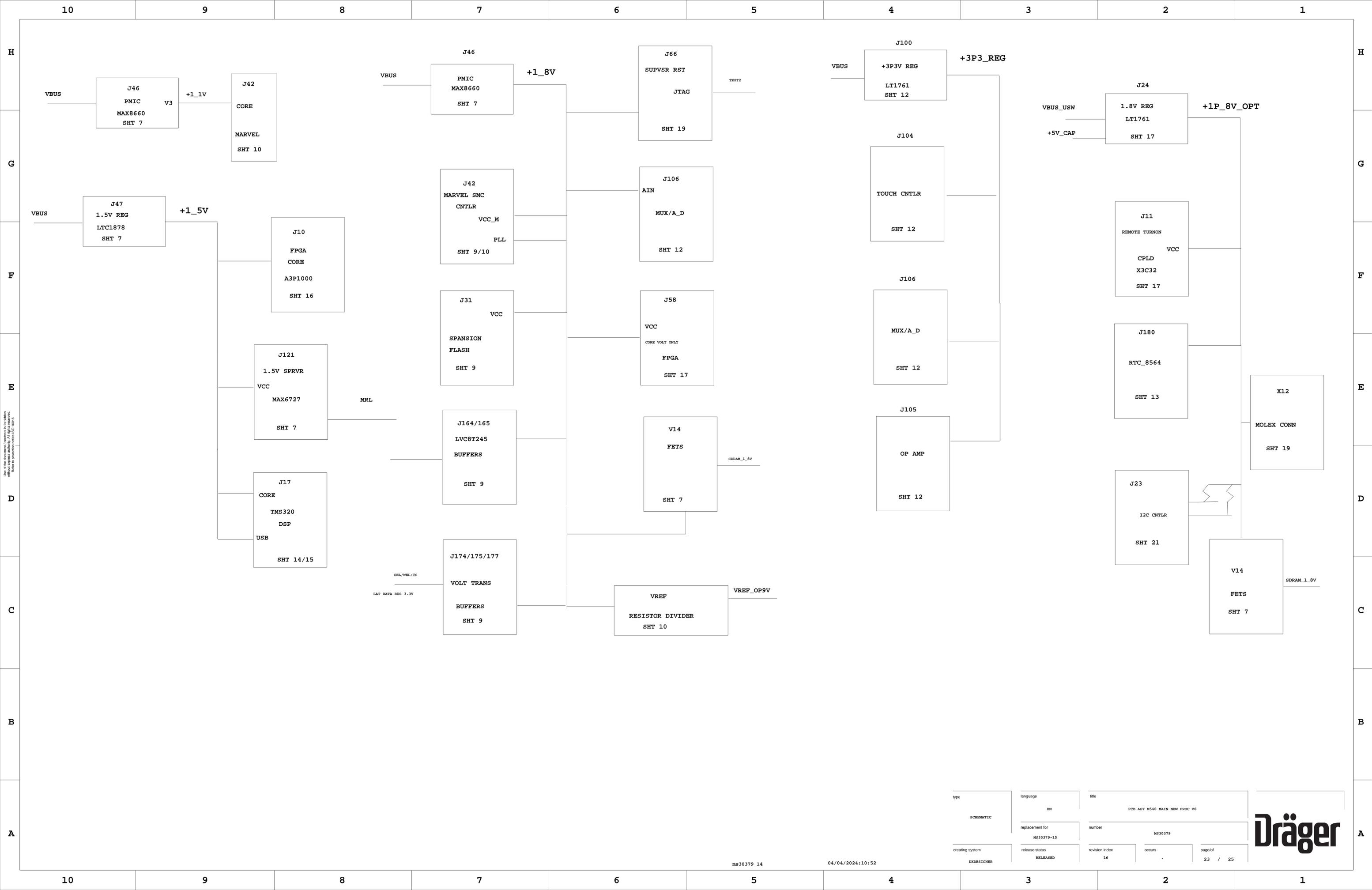


I2C HUB



type	language	title
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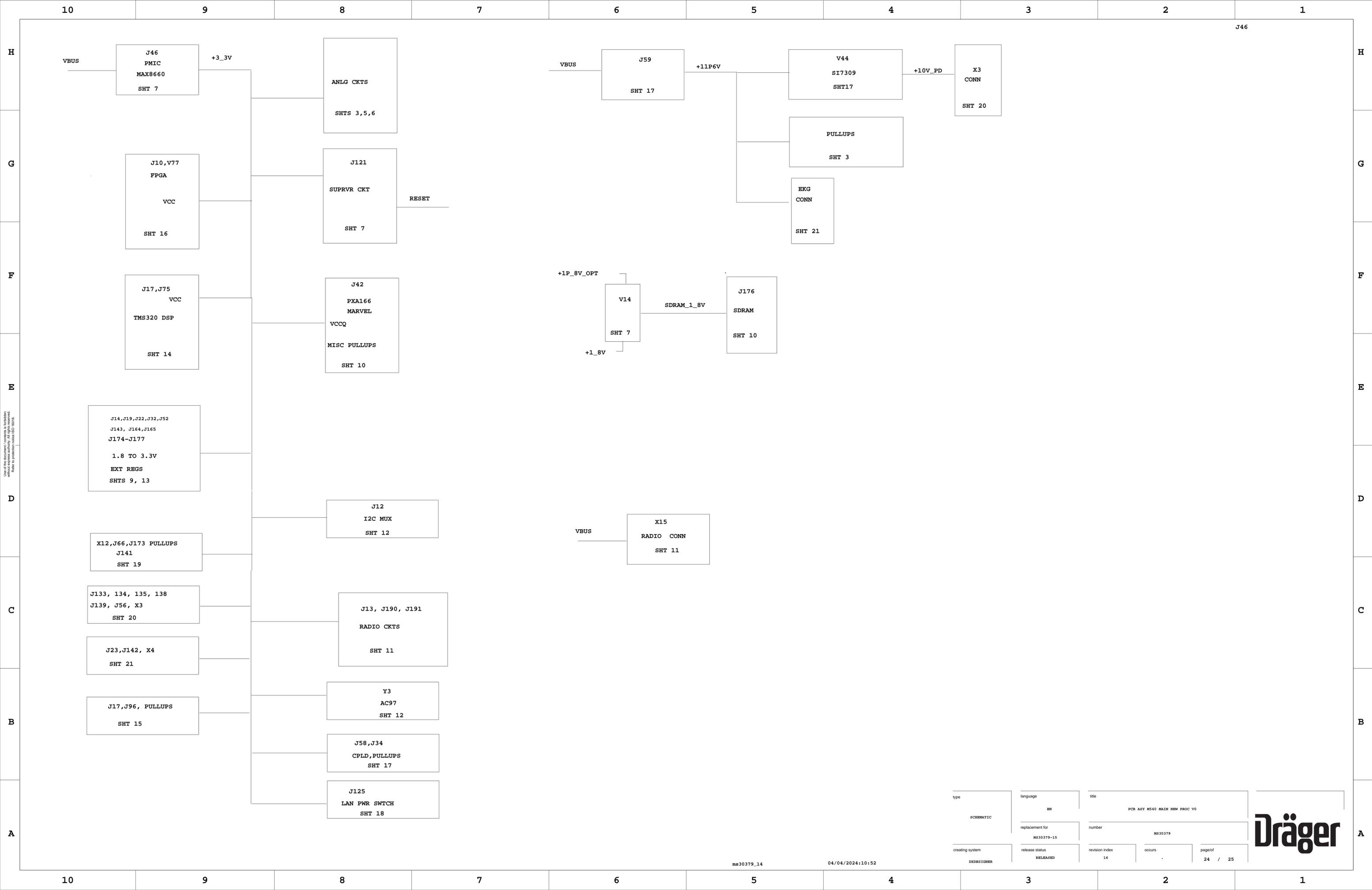




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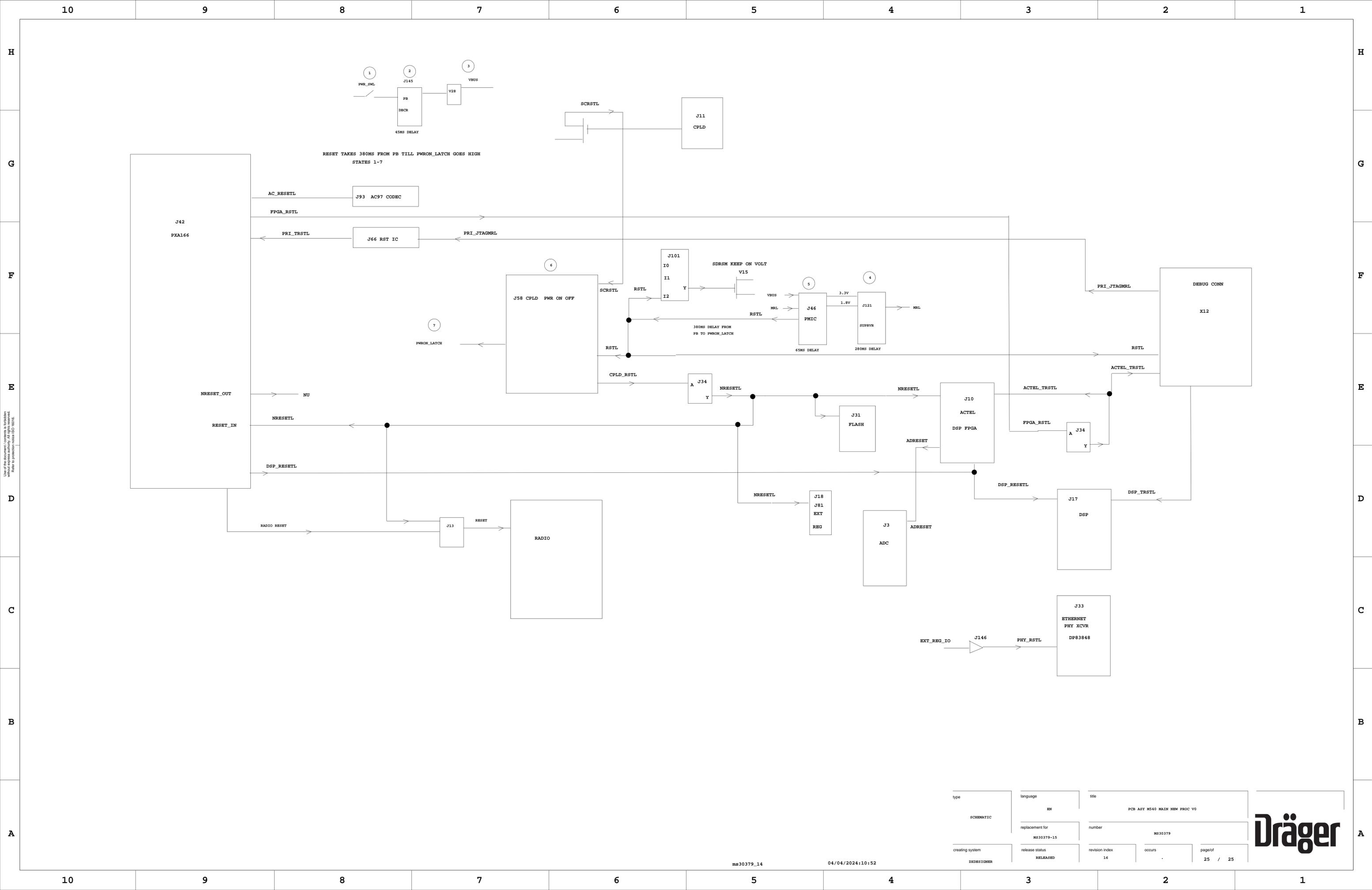




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release status	revision index	page/of	
RELEASED	16	24 / 25	





RESET TAKES 380MS FROM PB TILL PWRON_LATCH GOES HIGH STATES 1-7

J93 AC97 CODEC

J66 RST IC

J58 CPLD PWR ON OFF

J101 I0 I1 I2

SDRSM KEEP ON VOLT V15

J46 PMIC

J121 SUPKVR

DEBUG CONN X12

J42 PXA166

J33 ETHERNET PHY XCVR DP83848

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