F1M26

Databook

Confidential / Preliminary Documentation

Revision v1.0

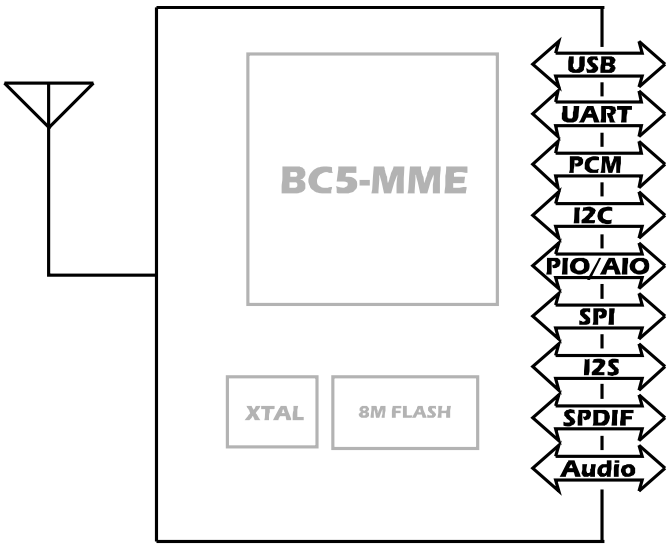
List of Contents

1. General

1.1 overview

This specification covers Bluetooth module (class-2) which complies with Bluetooth specification version 2.1+ EDR and integrates RF & Baseband controller in small package. This Module has deployed CSR's BC05-Multimedia External chipset.

All detailed specification including pinouts and electrical specification may be changed without notice.



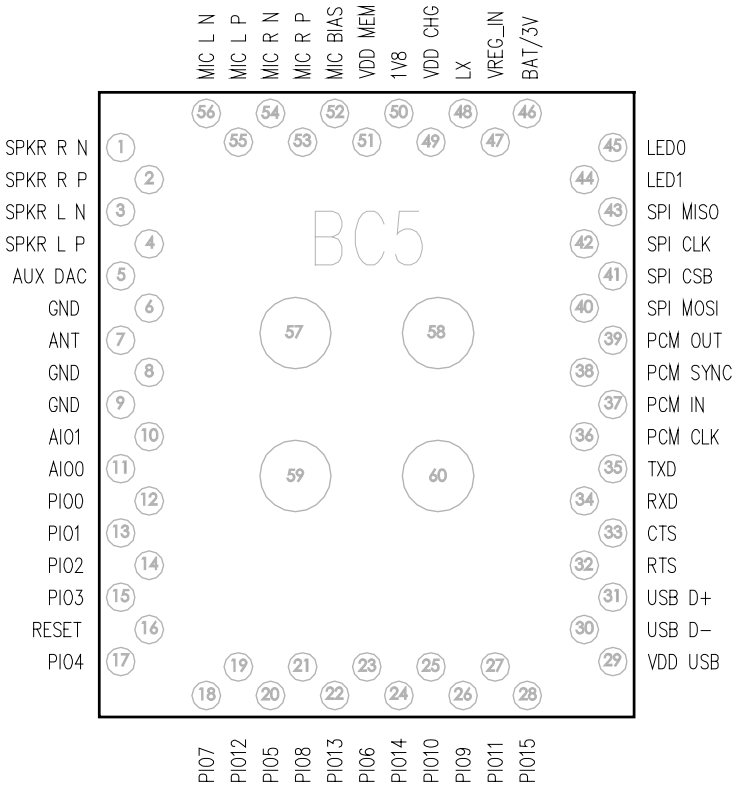
1.2 Features

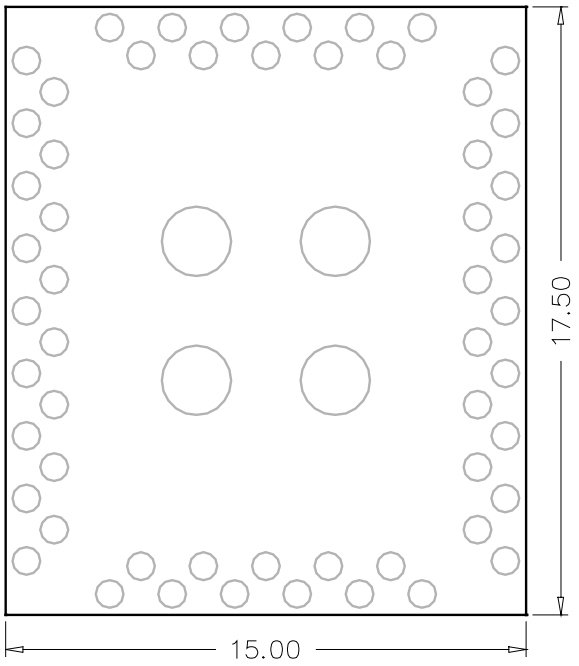
- Fully Qualified Bluetooth v2.1+EDR System
- Kalimba DSP Co-Processor
- 16-bit Internal Stereo Codec – 95dB SNR for DAC
- Integrated Switched-Mode Regulator
- Integrated Battery Charger
- USB and UART with Dual Port Bypass Mode to 4Mbits/s
- Supports up to 32Mbits of External Flash Memory (8Mbits Typical Requirement)
- Multi-Configurable I^2S, PCM or SPDIF Interface
- Enhanced Audibility and Noise Cancellation
- Support for 802.11 Co-existence
- RoHS Compliant
- Competitive Size (15mm x 17.5mm x 2mm : QFN 60Pin)

1.3 Application

- Bluetooth-Enabled Automotive Wireless Gateways
- High Quality Stereo Wireless Headsets
- High Quality Mono Headsets
- Hands-Free Car Kits
- Wireless Speakers
- VOIP Handsets
- Analogue and USB Multimedia Dongles

1.4 Pinout Diagram & Outline Size

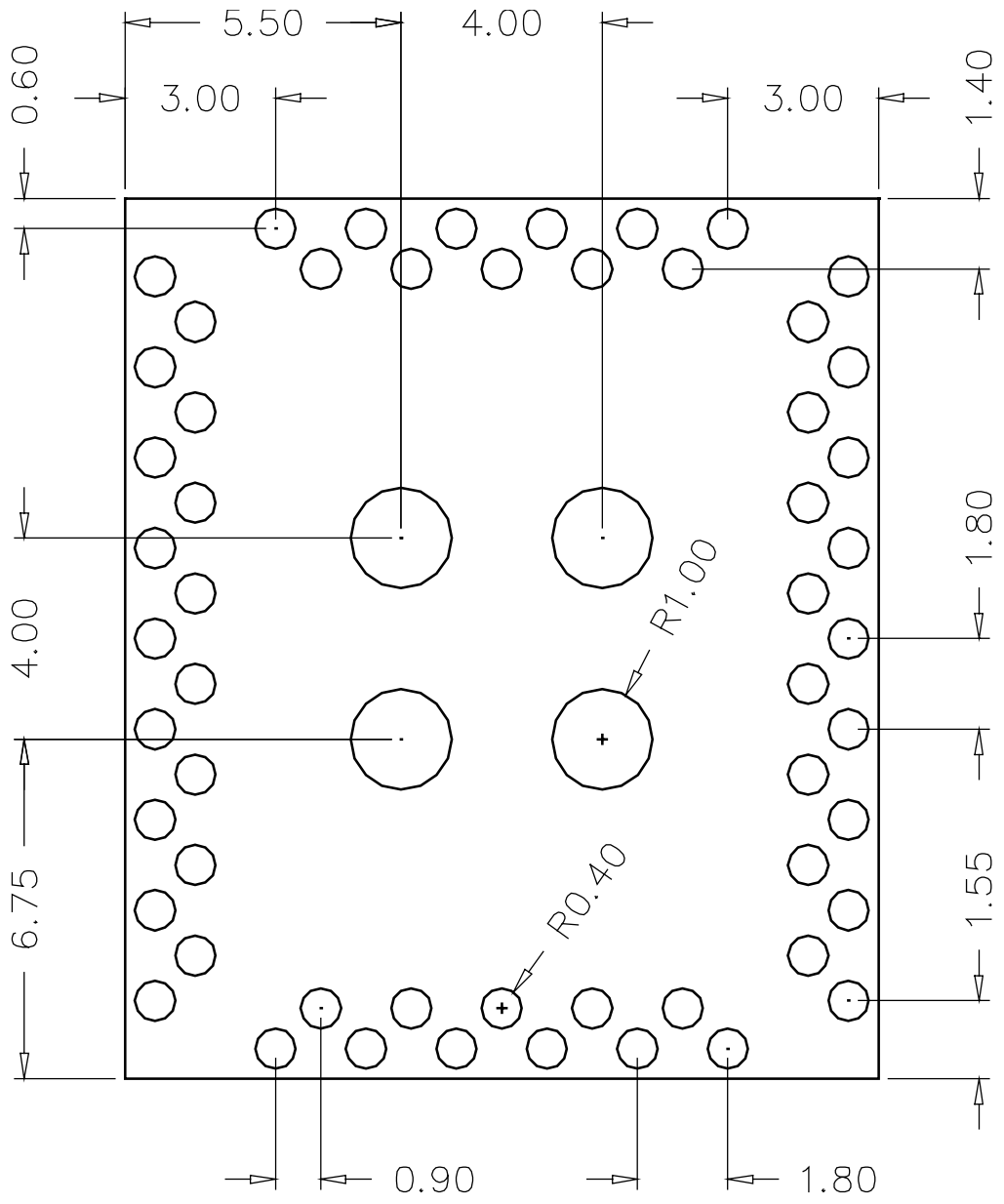




1.5 Device Terminal Functions

	Name	PIN	Description
PCM	PCM OUT	39	Synchronous data output
	PCM IN	37	Synchronous data input
	PCM CLK	36	Synchronous data clock
	PCM SYNC	38	Synchronous data sync
UART	TXD	35	UART data output, active low
	RXD	34	UART data input, active low (idle status high)
	CTS	33	UART clear to send active low
	RTS	32	UART request to send active low
USB	USB -	30	USB -
	USB +	31	USB + with selectable internal 1.5k pull-up resistor
PIO & AIO	PIO0	12	Programmable input/output line PIO 4,5,6,7 Can be used UART bypass mode PIO 6,7,8 Can be used to form I2C interface
	PIO1	13	
	PIO2	14	
	PIO3	15	
	PIO4	17	
	PIO5	20	
	PIO6	23	
	PIO7	18	
	PIO8	21	
	PIO9	26	
	PIO10	25	
	PIO11	27	
	PIO12	17	
	PIO13	22	
	PIO14	24	
	PIO15	28	
	AIO0	11	
	AIO1	10	
SPI	SPI MOSI	40	Serial Peripheral Interface data input
	SPI CLK	42	Serial Peripheral Interface clock
	SPI MISO	43	Serial Peripheral Interface data output
	SPI CSB	41	Chip Select for Synchronous SPI active low
Audio	AIN R-	54	Microphone input negative (Right side)
	AIN R+	53	Microphone input positive (Right side)
	AIN L-	56	Microphone input negative (Left side)
	AIN L+	55	Microphone input positive (Left side)
	MIC BAIS	52	Microphone bias
	AOUT R-	1	Speaker output negative (Right side)
	AOUT R+	2	Speaker output positive (Right side)
	AOUT L-	3	Speaker output negative (Left side)
	AOUT L+	4	Speaker output positive (Left side)
Other Pins	ANT	7	RF Connection to Antenna
	GND	6,8,9,57,58,59,60	Ground
	AUX DAC	5	8-bit voltage-output DAC
	1V8	50	1.8V
	BAT/3V	46	Main supply input voltage.
	RESETB	16	Reset if low. Input debounced so must be low for >5ms to cause a reset
	VREG IN	47	Take high to enable high-voltage linear regulator and switch-mode regulator
	VDD CHG	49	Lithium ion/polymer battery charger input
	VDD MEM	51	Positive supply for Flash pads
	VDD USB	29	Positive supply for UART/USB ports
	LX	48	Switch-mode power regulator output
	LED0	45	LED driver
	LED1	44	LED driver

1.6 Module Dimension



2. Characteristics

2.1 Electrical Characteristics

Absolute Maximum Ratings		
Rating	Minimum	Maximun
Storage temperature	-40°C	85°C
Supply voltage : VCC	-0.4V	3.7V
Supply voltage : VDD_CORE	-0.4V	2.2V
Other terminal voltages	VSS-0.4V	VCC+0.4V

Recommended Operating Conditions		
Operating Condition	Minimum	Maximun
Operating temperature range	-30°C	70°C
Supply voltage : VCC	1.7V	3.6V
Supply voltage : VDD_CORE	1.7V	1.9V

2.2 RF Characteristics

Transmitter (Measured at 2441MHz)

Specification	Condition	Min	Typ	Max	Unit
Output transmit power	Normal	-6	1	4	dBm
Transmit power density	Normal			4	dBm
Transmit power control	Normal	2		8	dBm
Frequency Range	Normal	2400		2483.5	MHz
20dB bandwidth for modulated carrier	Normal		850	1000	KHz
Adjacent channel transmit power	±2MHz ±3MHz ±4MHz			-20 -40 -40	dBm
Modulation Characteristics	f1avg f2max f2avg / f1avg	140 115		175 80	KHz KHz %
Initial carrier frequency tolerance	Normal	-20		20	KHz
Carrier frequency Drift	One slot packet(DH1) Three slot packet(DH3) Five slot packet(DH5)	-25 -40 -40		25 40 40	KHz

Transceiver

Specification	Condition	Min	Typ	Max	Unit
Adjacent channel transmit power	30MHz ~ 1GHz 1GHz ~12.75GHz 1.8GHz ~5.1GHz 5.1GHz ~5.3GHz			-36 -30 -47 -47	dBm

Receiver (Measured at 2441MHz)

Specification	Condition	Min	Typ	Max	Unit
Sensitivity level (0.1% BER)	Single slot packets	-70	-78		dBm
Transmit power density	Multi slot packet	-70	-78		dBm
C/I performance	co-channel 1MHz (Adjacent channel) 2MHz (2nd Adjacent channel) 3MHz (3rd Adjacent channel)			11 0 -30 -40	dB
Blocking performance	30MHz ~ 2000MHz 2000MHz ~ 2400MHz 2500MHz ~ 3000MHz 3000MHz ~ 12.75GHz	-10 -27 -27 -10			dBm
Intermodulation performance	n=5	-39			dBm
Maximum input level		-20	-10		dBm

3. Terminal Description

3.1 UART

Four signals are used to implement the UART function.

UART_TXD and UART_RXD transfer data between the two devices.

3.1.1 UART Setting

User can change data format the following selection using PSKEY.

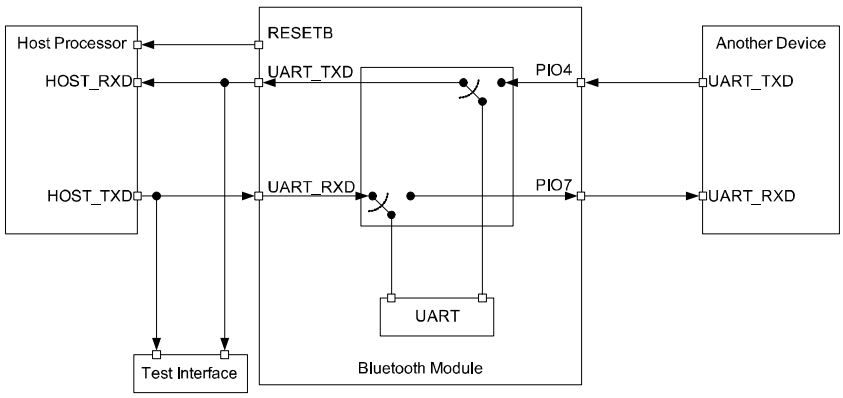
However, host shall communicate with default setting UART connection initiated at first time.

Baud Rate = (PSKEY_UART_BAUD_RATE) / 0.004096

Parameter	Possible value
Baud Rate	9600 ~ 3M Baud
Flow Control	None
Parity	None, Odd or Even
Number of Stop Bits	1 or 2
Bits per channel	8

3.1.2 UART Bypass Mode

switch the bypass to PIO4, 7 as shown in figure. When the bypass mode has been invoked, module enters the deep sleep state indefinitely



3.2 USB

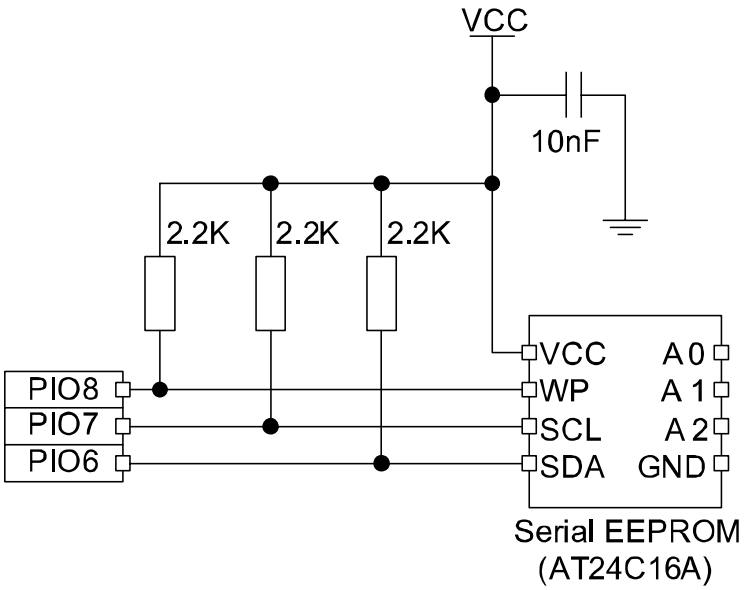
BlueCore5-Multimedia External devices contain a full speed (12Mbits/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.1 or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

As USB is a Master/slave oriented system (in common with other USB peripherals), BlueCore3-Multimedia External only supports USB slave operation.

3.3 I²C

PIO[8:6] can be used to form an interface. The interface is driven by “bit banging” these PIO pins using software. Therefore it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD).

Note. PIO[7:6] dual functions, UART bypass and EEPROM support, therefore devices using an EEPROM connect support UART bypass mode. PIO Lines need to be pulled-up through 2.2K



3.4 PCM

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, this module has hardware support for continual transmission and reception of PCM data, so reducing processor overhead for wireless headset applications. This module offers a bi-directional digital audio interface that route directly into the baseband layer of the on-chip firmware. It dose not pass through the HCI protocol layer.
Hardware allows the data to be sent to and received from a SCO connection. This module interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 for channel A-law and u-law CODEC
- Motorola MC145481 8-bit A-law and u-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs

3.4.1 PCM Configuration

The PCM configuration is set using two PS keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The default for long frame sync and interface master generating 256KHz PCM_CLK with no tristating of PCM_OUT.

Parameter	Possible value
Mode	Slave, Master
Clock rate	Master Mode : 128, 256, 512KHz Slave Mode : up to 2048KHz
Sync formats	Long frame sync, Short frame sync
Data formats	13 or 16bit linear, 8-bit A-law to u-law

3.5 Stereo Audio Interface

3.5.1 ADC

The ADC consists of two second order Sigma Delta converters allowing two separate channels that art identical in functionality. Each ADC Support 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz sample rates. The ADC contains two gain stages for each channel, an analogue and a digital gain stage. The digital gain stage has a value in the range of 0 to 15. In simple terms the first stage simplifier has a selectable 20dB gain stage for the microphone. The Second stage of the analogue amplifier has a gain with seven individual 3dB steps. The overall range of the analogue amplifier is approximately -4dB to 40dB. The full scale range of the input to the ADC is kept to approximately 400mV rms.

3.5.2 DAC

The DAC consists of two second order Sigma Delta converters allowing two separate channels that are identical in functionality. Each DAC supports 48kHz, 44.1kHz, 32kHz, 24kHz, 22.05kHz, 16kHz, 11.025kHz, 8kHz samples rates. The DAC contains two gain stages for each channel, a digital and an analogue gain stage. The digital gain stage has a value in the range of 0 to 15. The second stage of the DAC analogue amplifier has a gain with seven individual 3dB steps.

3.5.3 Digital Audio Interface

Digital audio bus shares the same pins as the PCM CODEC interface. Each of the audio busses are mutually exclusive in their usage.

PCM interface	SPDIF interface	I2S interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC		WS
PCM_CLK		SCK

3.5.3.1 I2S Interface

The digital audio interface supports the industry standard formats for I2S, left-justified (LJ) or right-justified (RJ). SD_OUT is limited to 16-bit per channel. SD_IN could have more then 16-bit per channel. SCK typically operates 64 x WS frequency and cannot be less then 36 x WS.

3.5.3.2 SPDIF Interface

The input and output stages of the SPDIF pins can interface either 75 connector ot there is an option to use an optical link that uses optical components.

4. Revision History

Revision	Date	Change Descriptions	Issued by
Rev 1.0	2008-02-26	Initial release	Narsen

5. Application Schematic