REVISION HISTORY

Version	Date	Description
VER.1.0	2014.10.10	▪ First version release.

1. INTRODUCTION

The LM2471-EM is a module applied by the MG2471-F48, System-on-Chip (SOC) of RadioPulse. It is designed for IEEE802.15.4 and RF4CE to realize low power and low cost application.
Basically it is used on ISM band of 2.405~2.48GHz, and it supports multiple data-rate modes(31.25Kbps ~ 1Mbps) applied with channel coding beside IEEE802.15.4 data-rate.

2. DEFINITIONS

MG2471-F48: 2.4GHz System-on-Chip developed by RadioPulse.

LM2471-EM: 2.4GHz Evaluation module(2-Layer) applied to ZigBee, IEEE802.15.4, and RF4CE.

3. APPLICATIONS

- 2.4 GHz IEEE 802.15.4 Applications
- RF4CE Remote Control Systems
- Lighting Systems
- Voice Applications
- Home/Building Automation
- Industrial Control and Monitoring
- Energy Management
- Low Power Wireless Sensor Networks
- Consumer Electronics
- Health-care equipments
- Toys

4. FEATURES

RF Transceiver

- Single-chip 2.4GHz RF Transceiver
- Low Power Consumption
- High Sensitivity of –98dBm at 250kbps
- No External T/R Switch or Filter needed
- On-chip VCO, LNA, and PA
- Programmable Output Power up to +9dBm
- Direct Sequence Spread Spectrum
- O-QPSK Modulation
- Scalable Data Rate including 250Kbps specified in IEEE802.15.4: 31.25Kbps ~ 1Mbps
- RSSI Measurement
- Compliant to IEEE802.15.4

Hardwired MAC

- Two 256-byte circular FIFOs
- FIFO management
- AES Encryption/Decryption Engine(128 bit)
- CRC-16 Computation and Check

8051-Compatible MCU

- 8051 Compatible (single cycle execution)
- 64KB Embedded Flash Memory
- 6KB Data Memory
- 128-byte CPU dedicated Memory
- 1KB Boot ROM
- Dual DPTR Support
- I2S/PCM Interface with two 256-byte FIFOs
- Two High-Speed UARTs with Two 16-byte FIFOs(up to 1Mbps)
- Four Timer/Counters
- 5 PWM channels
- Watchdog Timer
- Sleep Timer using the 32KHz RC-OSC clock
- Quadrature Signal Decoder
- 22 General Purpose I/Os for MG2471-F48B
- Internal 32KHz RC oscillator for Sleep Timer
- 16 MHz High Speed RC oscillator for the fast start-up from reset & power-down mode
- On-chip Power-on-Reset and Brown-out detector
- 4-channel 12-bit ADC(ENOB > 10-bit)
- SPI Master/Slave Interface with two 16-byte FIFOs
- Programmable IR(Infra-Red) Modulator
- ISP (In System Programming)
- External clock output function(500KHz, 1/2/4/8/16/32 MHz selectable)

Clock Inputs

- 32MHz Crystal for System Clock

Power

- 1.8V(Core)/2.0~3.6V(I/O) Operation
- Power Management Scheme with Deep Sleep Mode
- Separate On-chip Regulators for Analog and Digital Circuitry.
- Power Supply Range for Internal Regulator(2.0V(Min) ~ 3.6V(Max))

Package

- Lead-Free 48-pin QFN Package (7mm x 7mm)

5. HARDWARE DESCRIPTION

LM2471-EM is a ZigBee module using MG2471-F48. The components of LM2471-EM are as follows;

- MG2471-F48 : RadioPulse ZigBee System-on-Chip (SOC)
- Crystal : 32MHz Crystal (CL=9pF)
- RF Connector : SMA Type RF Connector
- CON(20PIN) : 20-Pin Connector*2 with 1.27mm pin pitch

In addition, this module needs only few components such as resistors and capacitors.

5.1. Block Diagram

As shown in [Figure 1], LM2471-EM includes the following features.

- MG2471: ZigBee Single chip embedded with 2.4GHz RF transceiver, base-band modem, a hardwired MAC, 64KB internal flash memory, 8051 microcontroller, 6KB data RAM, voice codec block, I2C, and 5-channel PWM.
- SMA type Antenna.
- 22 General Purpose I/Os, 4-channel 10-bit ADC, various peripherals such as Two High-Speed UARTs etc.
- Firmware downloading by UART1 in ISP mode (In-System-Programming) mode.

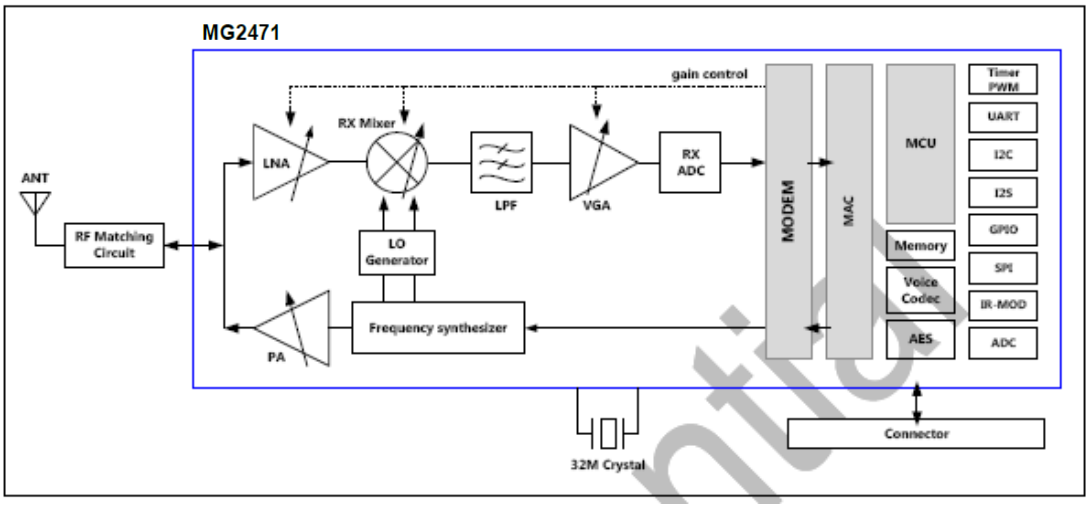


Figure 1. LM2471– EM Block Diagram

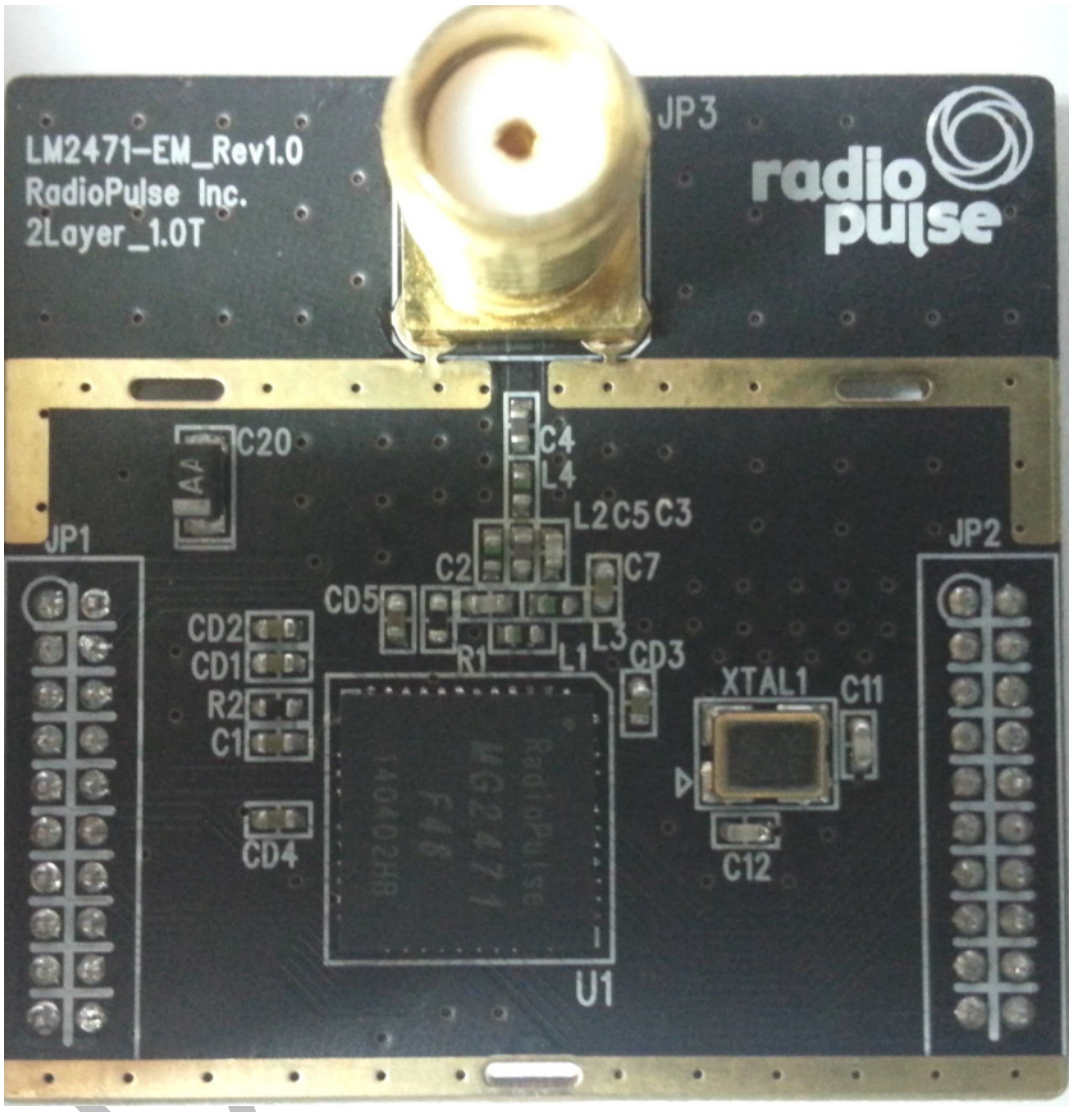
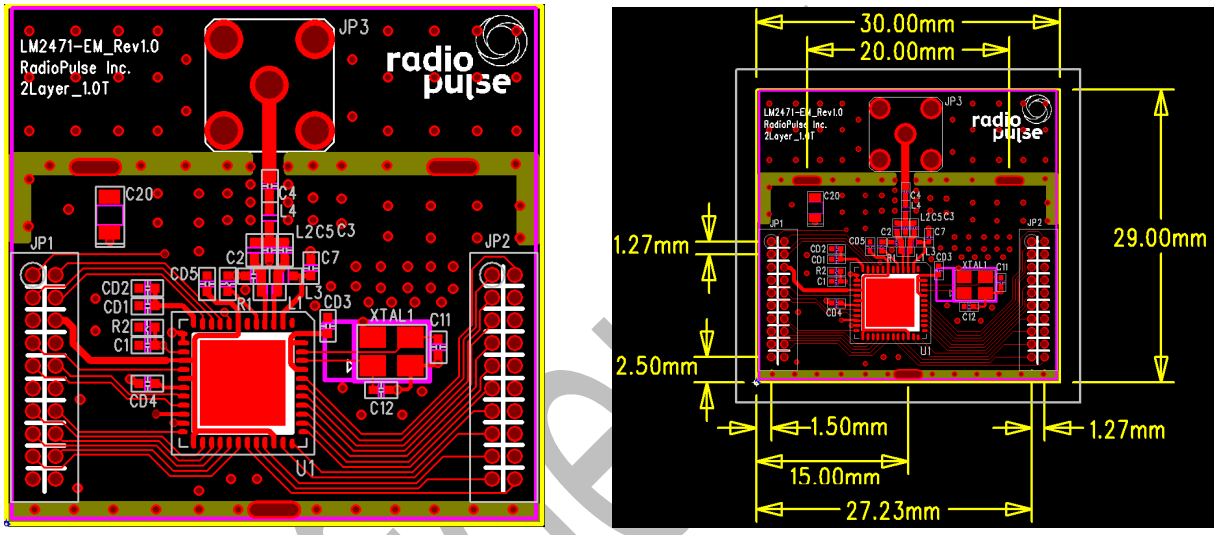


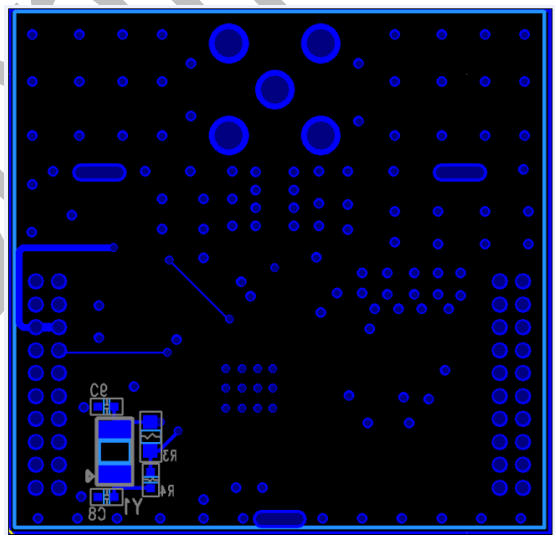
Figure 2. Appearance of LM2471-EM

5.2. Module Dimension

The following [Figure 3] shows the dimension of the LM2471-EM module. (a), (c) in [Figure 3] shows the component placement. (b) in [Figure 3] shows the dimension of LM2471-EM and placement for the connector pin. Two 20-pin connectors are located at the bottom.



(a) Top (b) Dimension



(C) Bottom

Figure 3. LM2471-EM

5.3. Antenna Matching Circuitry

[Figure 4] shows the recommended RF matching circuit. For PCB pattern, please refer to the [Figure 5].

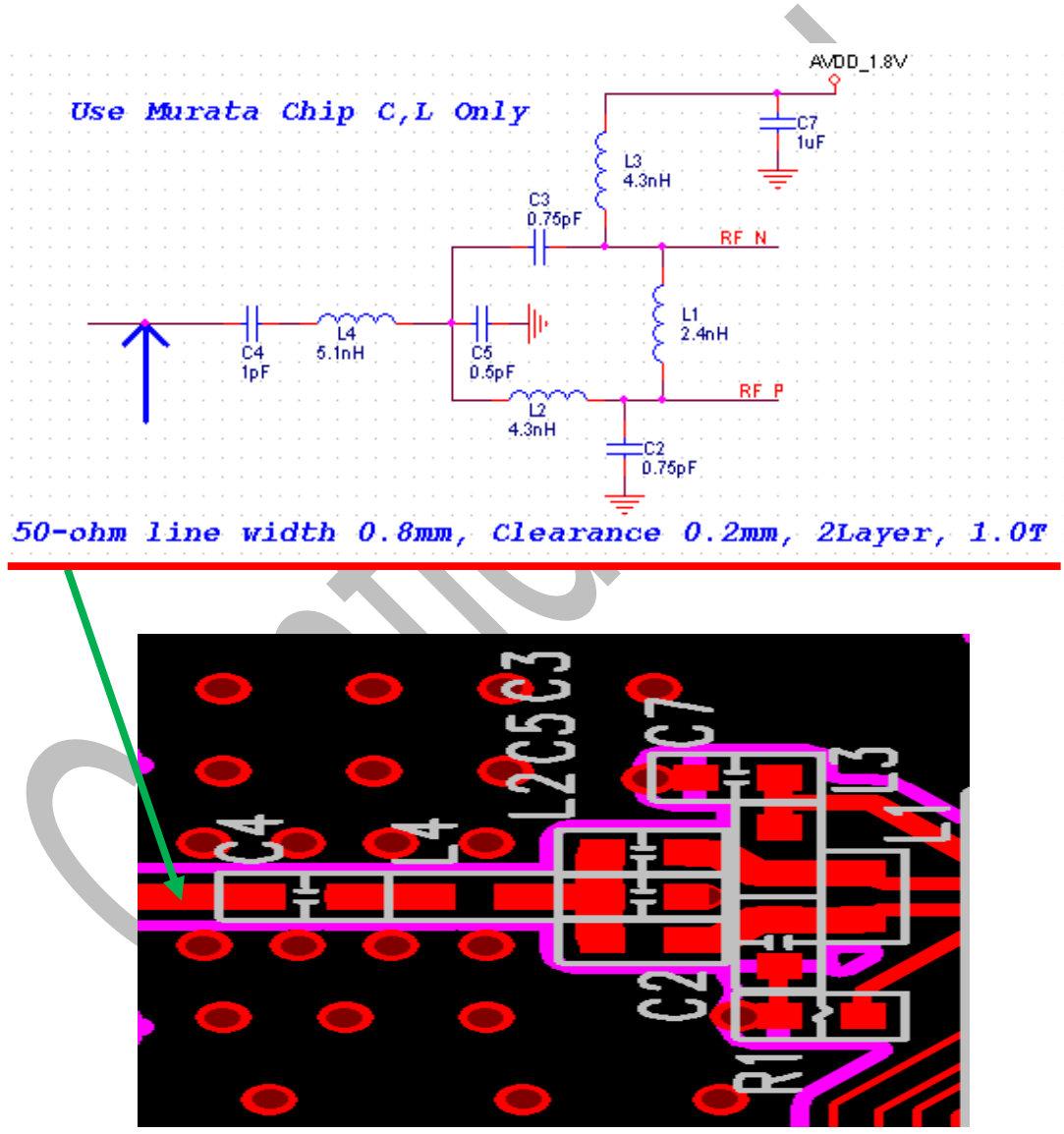


Figure 4. Antenna Matching Circuit

RF Matching Procedure

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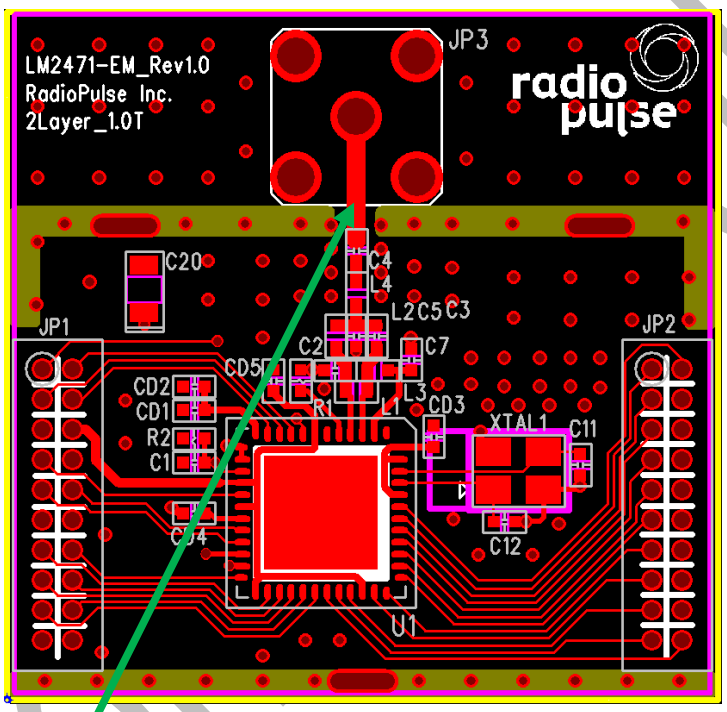
① The value of L2/C2/L4/C4 is adjusted to 2.4GHz.
② L4 and C4 are fixed value to organize Narrow Band-Filter.
③ Adjust L1 and C5 value to maximize output level.
④ Adjust L4 and C4 to minimize 2nd and 3rd harmonic.



***PCB Thickness: 1mm /0.5 OZ(2-Layer)**

Figure 5. Antenna PCB Pattern

Table 1. PCB Thickness 50ohm Line Width

H(mm)	W(mm)	Z0(Ohm)
0.4	0.5	49.487
0.8	0.7	50.514
1.0	0.8	49.798
1.2	0.8	50.821
1.6	0.9	50.192

6. SPECIFICATION

6.1. Absolute maximum ratings

Symbol	Parameter	Rating	Unit
3V_IN	AVDD3V1,AVDD3V2,DVDD3V1 ,DVDD3V2	-0.3 to 3.6	V
Core	ADCOUPL1,ADCOUPL2,ADCO UPL3,AVDD18V,DVDD,DXOSC 18V	-0.3 to 2	V
RF_{IN}	Input RF level	10	dBm
T_{STG}	Storage Temperature	-40 to 85	℃

6.2. DC Characteristics

Symbol	Parameter	Min	Typ.	Max	Unit
3V_IN	AVDD3V1,AVDD3V2,DVDD3V1 ,DVDD3V2	2	3.0	3.6	V
V_{IH}	High level input voltage	2.5			V
V_{IL}	Low level input voltage			0.4	V
V_{OH}	High level output voltage	2.5			V
V_{OL}	Low level output voltage			0.4	V
T_A	Air temperature	-40		85	℃

6.3. RF Characteristics (25℃)

6.3.1. Electrical specifications

Condition: EVM Board, at 25℃, 3V_IN=3.0V, F_{req}=2.45GHz, Chip rate =2MCPS

Item		Spec	Remark
Frequency Range		2400 ~ 2480MHz	
Frequency Tolerance		<±20ppm	
Occupied B.W		2MHz	
Output Power (Normal)		9dBm (±1dB)	Min. 7dBm
VSWR		<2.0 : 1	
Flatness		<1.5 dB	
Spurious Emissions 1GHz Under 1GHz ~ 2.4GHz ~ 12GHz		 <-50dBm <-50dBm <-50dBm	
2nd Harmonic		<-42dBm	
3rd Harmonic		<-45dBm	
Inband Spurious		<-45dBm	
Adjacent Channel Rejection	±3.5MHz	>30dBc	
Secondary Radiated Emission		<-59dBm	Limit of secondary radiated emissions.
Phase Noise	100KHz	-80dBc / Hz	
	1MHz	-103dBc / Hz	
	2MHz	-111dBc / Hz	
	3MHz	-113dBc / Hz	
Rx Sensitivity		<-96dBm	
Max. Input Power Level		0 dBm	Per 1% condition
Error Vector Magnitude		<10%	

7. PIN DESCRIPTION

The following [Table 2] and [Table 3] describe the interface signals to be used to communicate with external devices.

Table 2. Left Pin Header(JP1) pins

Pin	Name	Type	Description
1	ACH0	ANALOG IN	(0~VCC) Level Analog ADC0 Input
2	ACH1	ANALOG IN	(0~VCC) Level Analog ADC1 Input
3	ACH2	ANALOG IN	(0~VCC) Level Analog ADC2 Input
4	ACH3	ANALOG IN	(0~VCC) Level Analog ADC3 Input
5	VCC	3.0V	POWER(3.0V)
6	VCC	3.0V	POWER(3.0V)
7	RESETB	INPUT	Active Low RESETB Input
8	ISP	INPUT	Active High In-System-Programming Input
9	P1_6	IN/OUT	General Purpose IO (Port P1.6 / I2C_SCL)
10	P1_7	IN/OUT	General Purpose IO (Port P1.7 / I2C_SDA)
11	P1_3	IN/OUT	General Purpose IO Port P1.3/QUADZA/PTC_GATE3/IR_TX/CLK_OUT
12	P1_4	IN/OUT	General Purpose IO Port P1.4/QUADZB/EXT_RTC_CLK/PTC_GATE4
13	P1_0 / RXD1	IN/OUT	General Purpose IO (8051 Port P1.0) UART1 RXD1
14	P1_1 / TXD1	IN/OUT	General Purpose IO (8051 Port P1.1) UART1 TXD1
15	P3_6	IN/OUT	General Purpose IO (Port P3.6/RTS1/SPICLK)
16	P3_7	IN/OUT	General Purpose IO (Port P3.7/CTS1/SPICSN)
17	P3_4	IN/OUT	General Purpose IO Port P3.4/RTS0/QUADYA/SPIDI/T0
18	P3_5	IN/OUT	General Purpose Port P3.5/CTS0/QUADYB/SPIDO/T1
19	GND	Ground	Ground
20	GND	Ground	Ground

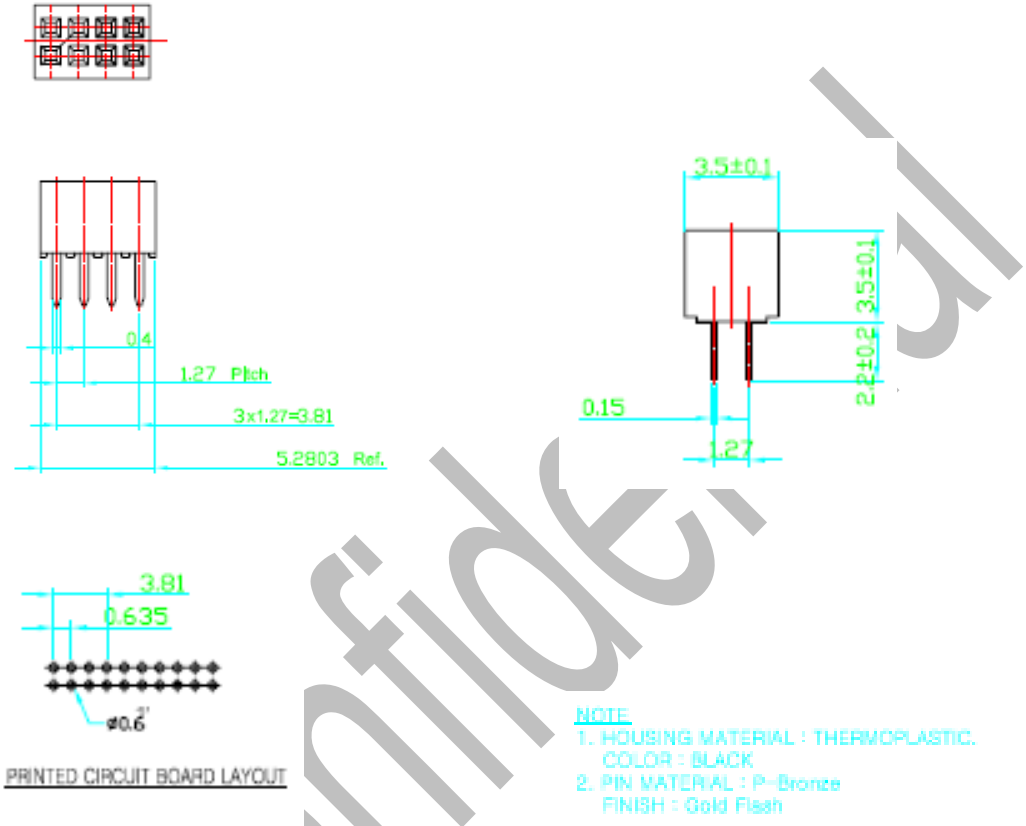
*** Digital I/O ：16mA drive capability

Table 3. Right Pin Header(JP2) pins

Pin	Name	Type	Description
1	P0_1	IN/OUT	General Purpose IO Port P0.1/I2SRX_LRCLK/PWM1
2	P0_0	IN/OUT	General Purpose IO Port P0.0/I2SRX_DI/PWM0
3	P0_2	IN/OUT	General Purpose IO Port P0.2/I2SRX_BCLK/PWM2
4	GND	Ground	Ground
5	P0_3	IN/OUT	General Purpose IO Port P0.3/I2SRX_MCLK/PWM3
6	NC		
7	P0_4	IN/OUT	General Purpose IO Port P0.4/I2STX_DO/PWM4
8	NC		
9	P0_5	IN/OUT	General Purpose IO Port P0.5/I2STX_LRCLK/PTC_GATE0
10	NC		
11	P0_6	IN/OUT	General Purpose IO Port P0.6/I2STX_BCLK/PTC_GATE1
12	NC		
13	P0_7	IN/OUT	General Purpose IO Port P0.7/I2STX_MCLK/PTC_GATE2
14	NC		
15	P3_0 / RXD0	IN/OUT	General Purpose IO (8051 Port P3.0) UART0 RXD0
16	NC		
17	P3_1 / TXD0	IN/OUT	General Purpose IO (8051 Port P3.1) UART0 TXD0
18	GND	Ground	Ground
19	P3_2 / INT0#	IN/OUT	General Purpose IO (8051 Port P3.2) External Active Low Interrupt Input
20	P3_3 / INT1#	IN/OUT	General Purpose IO (8051 Port P3.3) External Active Low Interrupt Input

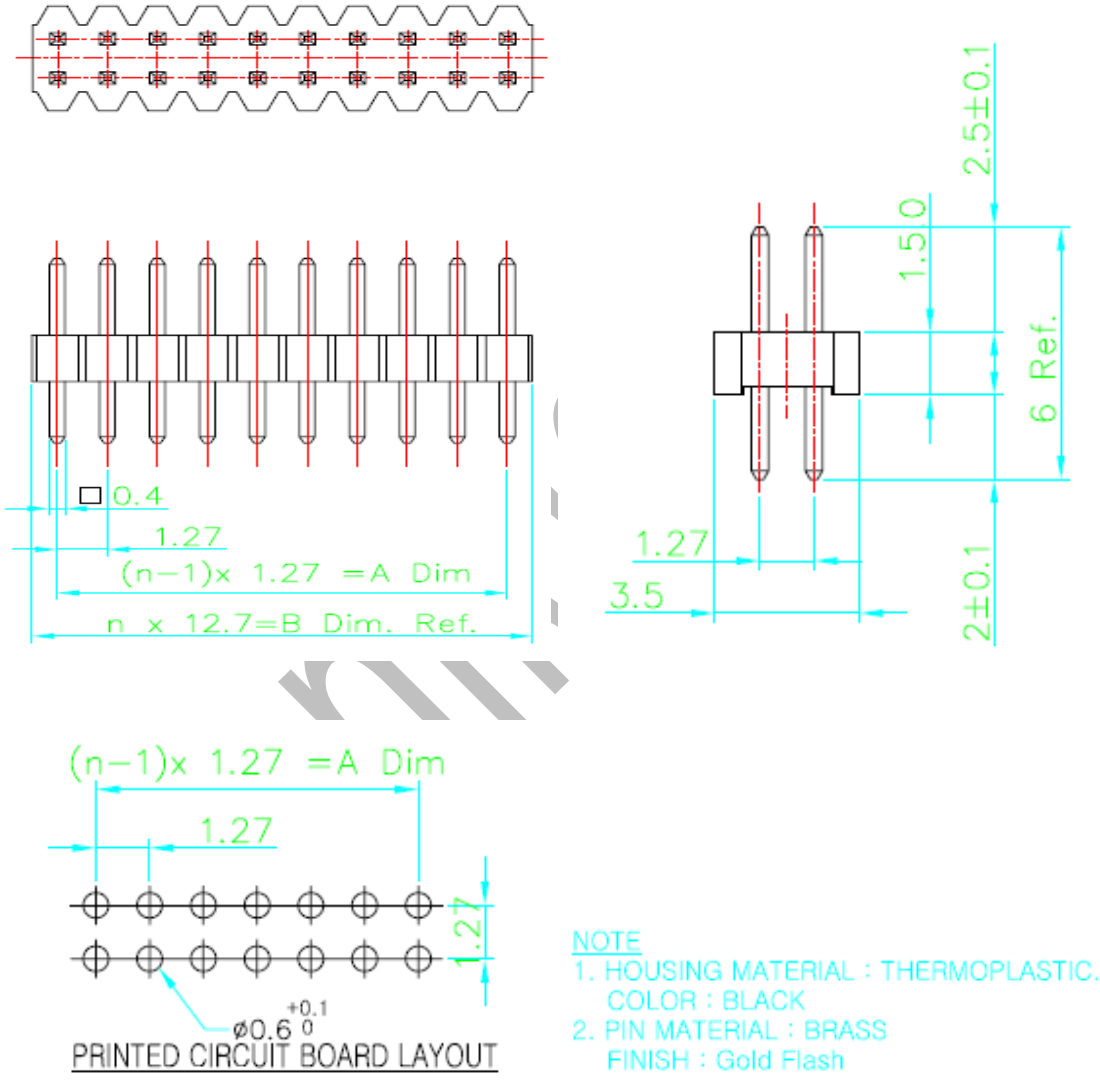
*** Digital I/O : 16mA drive capability

■ **20-Pin Female Connector**



8. CONNECTOR DIMENSION

■ **20-Pin male Connector**



NOTE
1. HOUSING MATERIAL : THERMOPLASTIC.
   COLOR : BLACK
2. PIN MATERIAL : BRASS
   FINISH : Gold Flash
3. Number of Position : 02 ~ 100

FCC compliance Information

FCC Information to User

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

• Reorient or relocate the receiving antenna.

• Increase the separation between the equipment and receiver.

• Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

• Consult the dealer or an experienced radio/TV technician for help.

Caution

Modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Compliance Information : This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation

This device is intended only for OEM integrators under the following conditions:

1) The transmitter module may not be co-located with any other transmitter or antenna,

2) OEM shall not supply any tool or info to the end-user regarding to Regulatory Domain change.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain

laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

To satisfy FCC exterior labeling requirements, the following text must be placed on the exterior of the end product : **Contains Transmitter Module FCC ID : UNTLM2471-EM**

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.