1 Product Concept

The product is a Bluetooth USB multimedia Dongle. It supports the Bluetooth audio streaming and remote control profiles (A2DP and AVRCP profiles).

It can be paired up with a Bluetooth stereo headphone or speaker system to play stereo music.

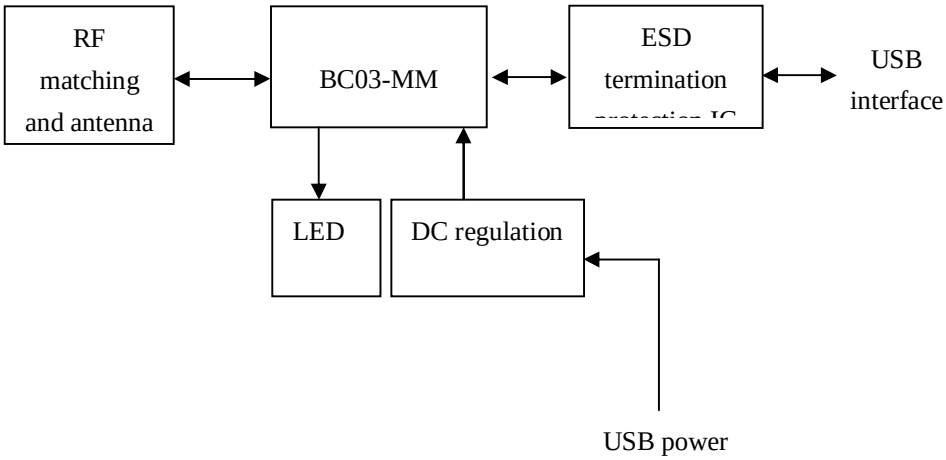
The target positioning is to support PC to stream audio via Bluetooth interface and without any add-on PC software(s) being installed on the PC.

2 Product Design

The system core is BC03-MM from CSR. It provides all the necessary features including the Bluetooth connection, USB interface, audio I/O and MMI.

The firmware platform is based on CSR BlueLab3.3.

The system architecture is depicted in the following figure.



3 BC03-MM Bluetooth Chip Pin Configurations

Radio	Ball	Pad Type	Description
RF_IN	D2	Analogue	Single ended receiver input
PIO[0]/RXEN	D3	Bi-directional with programmable strength internal pull-up/down	Control output for external TX/RX (if fitted)
PIO[1]/TXEN	C4	Bi-directional with programmable strength internal pull-up/down	Control output for external PA (If fitted)
BAL_MATCH	A1	Analogue	Tie to VSS_RADIO
RF_CONNECT	B1	Analogue	50Ω RF matched I/O
AUX_DAC	C2	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	L3	Analogue	For crystal or external clock input
XTAL_OUT	L4	Analogue	Drive for crystal

USB and UART	Ball	Pad Type	Description
UART_TX	J10	CMOS output, tri-state, with weak internal pull-up	UART data output
UART_RX	J11	CMOS input with weak internal pull-down	UART data input
UART_RTS	L11	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
UART_CTS	K11	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	L9	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	L8	Bi-directional	USB data minus

PCM Interface[1]	Ball	Pad Type	Description
PCM_OUT	G10	CMOS output, tri-state, with weak internal pull-down	Synchronous data output
PCM_IN	H11	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G11	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	H10	Bi-directional with weak internal pull-down	Synchronous data clock

PIO Port	Ball	Pad Type	Description
PIO[11]	A5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	A4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	B4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	B3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]/UART_RX[1]/ CLK_OUT	K9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line or programmable frequency clock output
PIO[6]/CLK_REQ/ UART_CTS[1]	K8	Bi-directional with programmable strength internal pull-up/down	PIO line or clock request output to enable external clock for external clock line
PIO[5]/USB_DETACH/ UART_RTS[1]	J9	Bi-directional with programmable strength internal pull-up/down	PIO line or chip detaches from USB when this input is high
PIO[4]/USB_ON/ UART_TX[1]	H9	Bi-directional with programmable strength internal pull-up/down	PIO or USB on (input senses when VBUS is high, wakes BlueCore3-Multimedia)
PIO[3]/USB_WAKE_UP/ HOST_CLK_REQ	B2	Bi-directional with programmable strength internal pull-up/down	PIO or output goes high to wake up PC when in USB mode or clock request input from host controller
PIO[2]/CLK_REQ	C3	Bi-directional with programmable strength internal pull-up/down	PIO or external clock request
AIO[0]	K5	Bi-directional	Programmable input/output line
AIO[1]	J7	Bi-directional	Programmable input/output line
AIO[2]	K7	Bi-directional	Programmable input/output line
AIO[3]	J8	Bi-directional	Programmable input/output line

Test and Debug	Ball	Pad Type	Description
RESET	F9	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
RESETB	G9	CMOS input, with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	C10	CMOS input with weak internal pull-	Chip select for Synchronous Serial Interface active low
SPI_CLK	D10	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	D11	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	C11	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	E9	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	L7	VDD/Regulator input	Linear regulator input
VDD_USB	L10	VDD	Positive supply for UART/USB ports
VDD_PIO	A3	VDD	Positive supply for PIO and AUX DAC[2]
VDD_PADS	E11	VDD	Positive supply for all other digital Input/Output ports [3]
VDD_CORE	F11, C7, L6	VDD	Positive supply for internal digital circuitry and 1.8V regulated output for digital circuitry, see further information in Section 8.14.1
VDD_RADIO	E3	VDD/Regulator sense	Positive supply for RF circuitry
VDD_LO	J2	VDD	Positive supply for local oscillator circuitry
VDD_ANA	L5	VDD/Regulator output	Positive supply for analogue circuitry and 1.8V regulated output
VDD_BAL	F1	VDD	Positive supply for balun
VDD_MEM	C8, B11, K6	VDD	Positive supply for internal memory and AIO ports
VSS_PADS	D9, E10, K10	VSS	Ground connections for input/output
VSS_CORE	F10, C6	VSS	Ground connection for internal digital circuitry
VSS_RADIO	E2, F3, G2	VSS	Ground connections for RF circuitry
VSS_LO	G3, H3	VSS	Ground connections for local oscillator
VSS_ANA	K4	VSS	Ground connections for analogue circuitry
VSS	C9	VSS	Ground connection for internal package shield
VSS_PIO	A2	VSS	Ground connection for PIO and AUX DAC
VSS_BAL	G1	VSS	Ground connection for balun
VSS_MEM	C5	VSS	Ground connection for internal memory, AIO and extended PIO ports
VSS_RF	J1, K1	VSS	Ground connection for RF circuitry

Notes:

(1) Transparent UART port maps directly to main UART port

(2) Positive supply for PIO[3:0] and PIO[11:8]

(3) Positive supply for SPI/PCM ports and PIO[7:4]

Unconnected Terminals	Ball	Description
	A6, A7, A8, A9, A10, A11, B5, B6, B7, B8, B9, B10, C1, D1, E1, F2, H1, H2	Leave unconnected

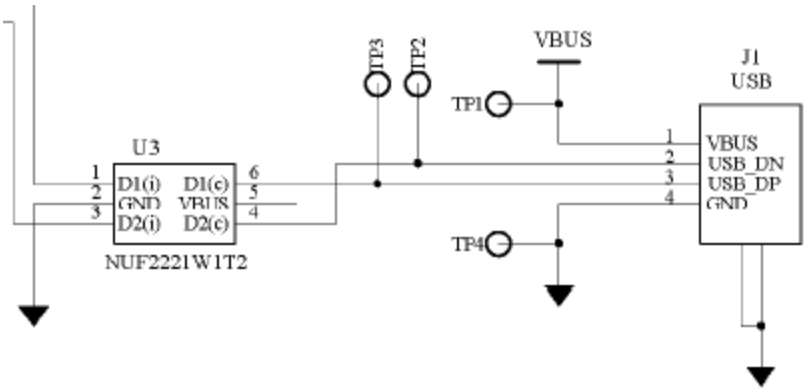
CODEC	Ball	Pad Type	Description
AUDIO_IN_P_LEFT	K2	Analogue	Microphone input positive (left side)
AUDIO_IN_N_LEFT	K3	Analogue	Microphone input negative (left side)
AUDIO_IN_P_RIGHT	L1	Analogue	Microphone input positive (right side)
AUDIO_IN_N_RIGHT	L2	Analogue	Microphone input negative (right side)
AUDIO_OUT_P_LEFT	J4	Analogue	Speaker output positive (left side)
AUDIO_OUT_N_LEFT	J3	Analogue	Speaker output negative (left side)
AUDIO_OUT_P_RIGHT	J6	Analogue	Speaker output positive (right side)
AUDIO_OUT_N_RIGHT	J5	Analogue	Speaker output negative (right side)

4 USB ESD Termination

Features:

Provides USB line Termination Filtering and ESD Protection

Bi-directional EMI Filtering Prevents Noise for Entering/Leaving the syetem



5 Voltage regulator

The XC6204 series are highly precise, low noise,positive voltage LDO regulators manufactured using CMOS processes.The series achieves high ripple rejection and lowdropout and consists or a standard voltage source ,an error correction,limiter and a phase compensation circuit plus a driver transistor.

The CE function enables the output to be turned off,resulting in greatly reduced power consumption.