CIRCUIT DESCRIPTION

FREQUENCY CONFIGURATION

The frequency configuration is shown in Figure 1

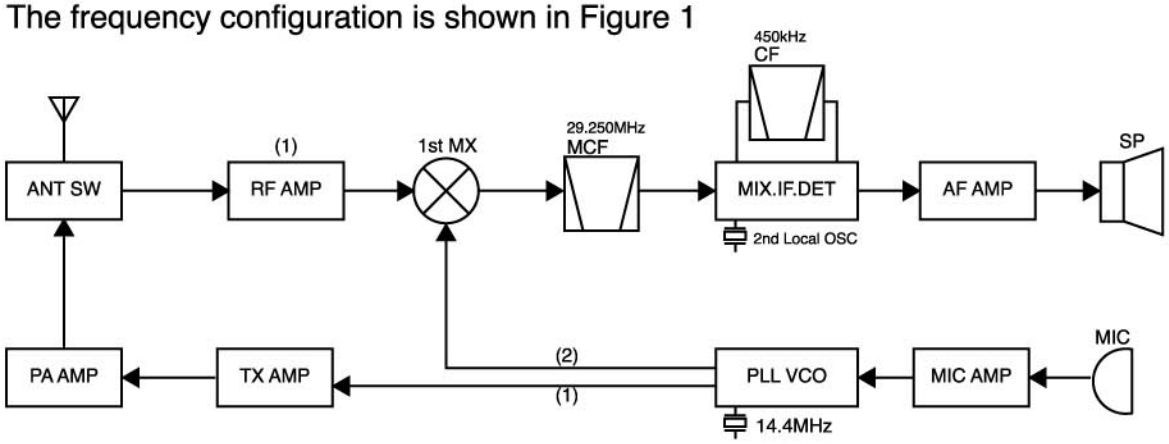

Fig.1

RECEIVER SYSTEM

RF amplifier

The signal from the antenna is passed through a low-pass filter andthe transmission/reception selector circuit D211,D212 input to the RF amplifier. The input signal is amplifier by T231. The unwanted frequency band of the signal is then eliminated by a band-pass filter.

First-stage mixer

The input signal is mixed with the first local oscillator signal from the PLL circuit by the first-stage mixer T251,producing a first IF signal. The unwanted frequency band of the first IF signal is eliminated by a crystal filters.

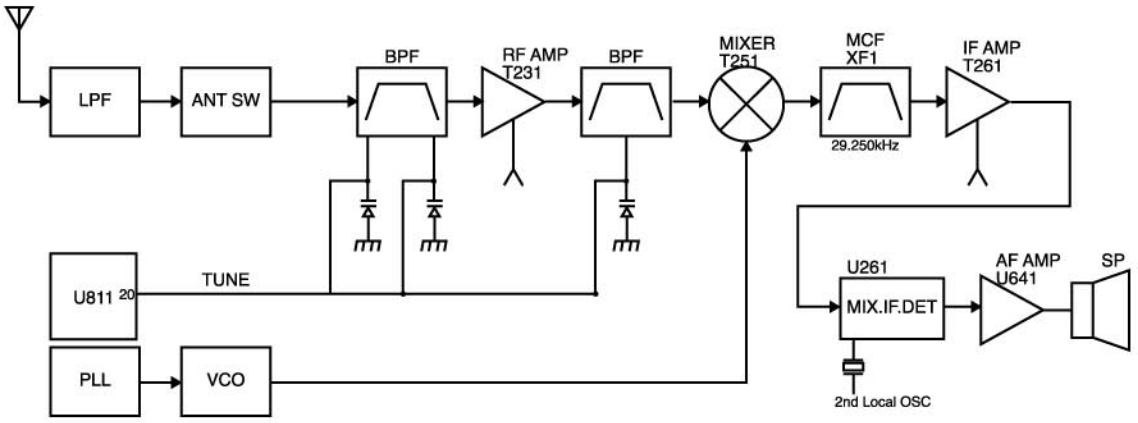

Fig.2

IF amplifier

The first IF signal is amplified by T261 and enters U261(FM signal processing IC), where it is mixed with the second local oscillator signal and so converted into the second IF signal. The unwanted frequency band of the second IF signal is eliminated by ceramic filter FL261. The resulting signal is then amplified and detected.

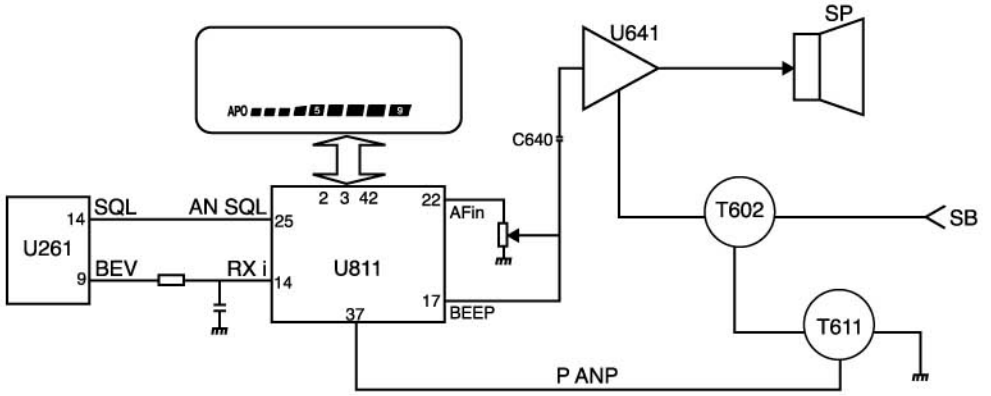

Fig.3

AF amplifier

The audio signal output by the FM detector are corrected by the high-pass filter and de-emphasize circuit. The audio signal is then passed through and AF variable resistor and amplified by power amplifier U641 to obtain the desired output.

Squelch and mute circuits

The output detected by U261 is input to MCU(pin 25), the voltage input to the microprocessor is digitized, and the microprocessor controls the MUTE.,RXI, RXO, thus controlling the audio signal. The microprocessor control this system from level 1-9, it can be programmable by software or keypad.

S meter

The S-meter signal is output from U261 as a direct voltage corresponding to the input signal, converted to a voltage by R278, then input to the microprocessor. The DC voltage is digitized to control the LCD S-meter display.

TRANSMITTING SYSTEM

Microphone amplifier

The audio band of the signal from the microphone is corrected by preem-phasis circuit The signal is amplified and limited by U411B(1/2). Distortion com-ponents exceeding the audio band of the resulting signal are then eliminated by a splatter filter consisting of U411A(2/2). Then input to Pin 15 of the microprocessor, VOX input to Pin 22 of the microprocessor.

Modulation circuit

The signal from the microphone amplifier passes through the modulation adjustment variable resister VR378, is applied to VCO varicap diode D333, and modulated by variable reactance.

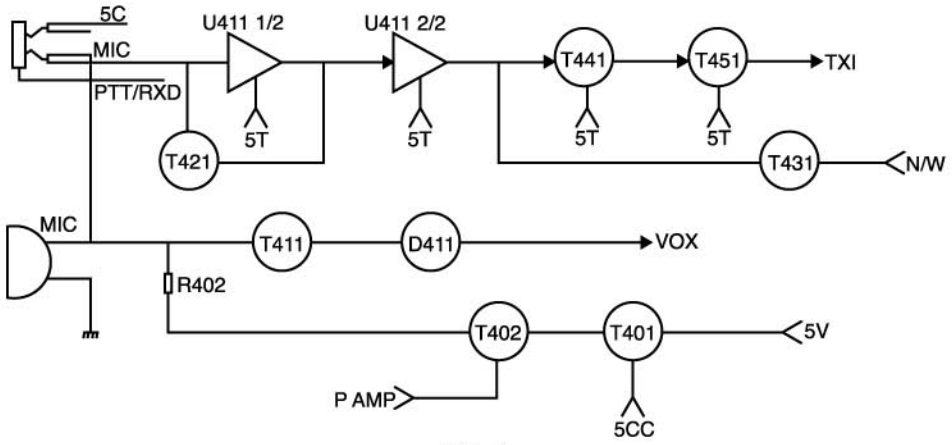

Fig.4

Drive and Final Circuit

The desired signal is produced by the VCO, and amplified by T111. It is then amplified by T121. The amplified signal is input to a two-stage FET amplifier, and increases the power to about 5W/4W.

Transmission/reception selector circuit

The transmission output is passed through the transmission/reception selectorcircuit and low-pass filter to the antenna. The transmission/reception selector circuit,which consists of D156,D211 and D212, is turned on during transmission and offduring reception to switch the signal.

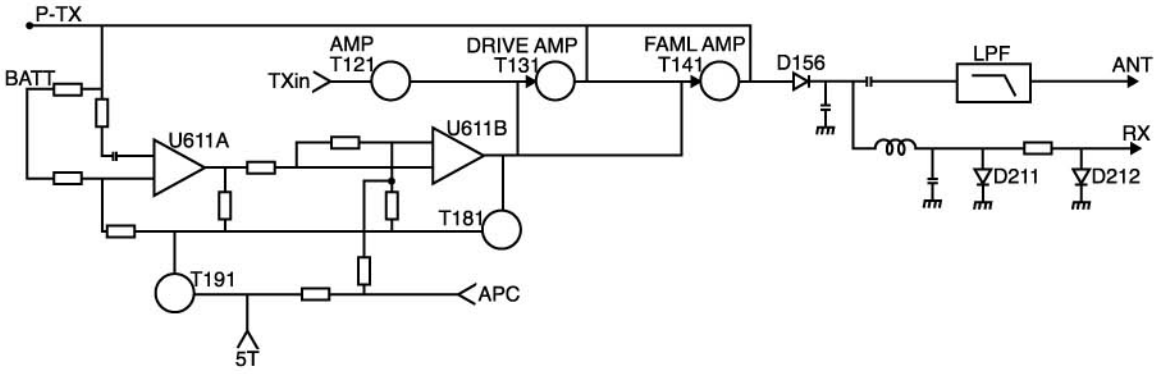

Fig.5

APC and transmission output selector circuits

The automatic power control(APC) circuit is used to obtain a stable transmission current. This circuit detects the drain current in the final stage of the power module and controls the transmission output. For U161, two voltages are applied: one is the reference voltage for transmission output adjustment, another is the detection voltage generated across R171,R173 in proportion to the drain voltage in the final stage. The voltage, proportional to the difference between the reference voltage and the detection voltage, is obtained at the output of U161. This voltage is reversed by T181 to provide the APC voltage. This APC voltage controls the power control pin of the power module and stabilizes the transmission output.

PLL CIRCUIT

PLL

The output from the 14.4Mhz reference oscillator is divided by U377 to produce a 5 kHz or 6.25Khz reference frequency. The comparison frequency is obtained by amplifying the VCO output by T331 and dividing it by the U311. 5,10, 12.5,20, and 25Khz PLL synthesizer is implemented by phase-comparing the reference frequency and comparison frequency obtained when CR311 is divided. The pulse output from Pin 5 of U311 according to the difference between the reference frequency and the comparison frequency is passed through the charge pump. And is removed the ripple by a low-pass filter to produce the lock voltage.

VCO

The desired frequency is directly produced by the Colpitts oscillator configured around FET,T331, and 351. The lock voltage is applied to D331, D332, D351 and D352 to change the oscillator frequency.

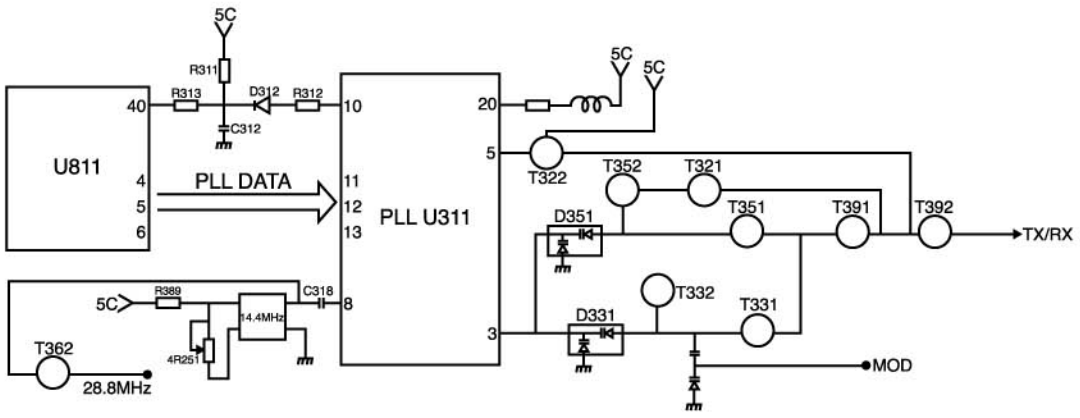

Fig.6

Unlock detection circuit

When the PLL is in the unlock state, the pulse that is output to the LD pin (pin 10) of PLL is waveform shaped by R312,D312,C312 and R313. The LD pin is then made high. The voltage at the LD pin is monitored by the microprocessor to control the transmission or reception selection timing.

DIGITAL CONTROL CIRCUIT

Keys and rotary encoder circuit

The signal from keys and rotary encoder input to microprocessor directly

Reset and backup circuits

When the SB is turned on, a high-level pulse is output from the reset circuit consisting of T881,C883, and R883 to reset microprocessor U881(Pin 32). If SB is turned off, U517 detects a 5V voltage drop, and outputs a low signal. When the microprocessor port goes low, it outputs data to U821 and enters backup mode.

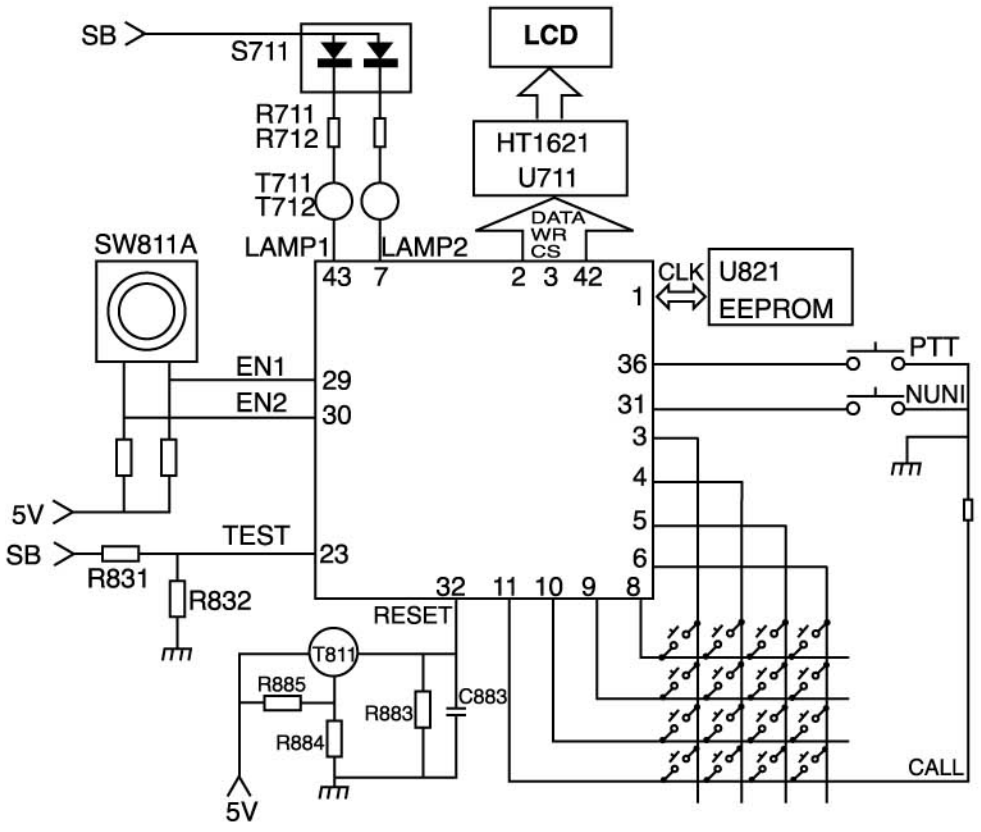

Fig.7

Battery voltage detector circuit

The supply voltage(SB) is divided and input to the analog port(Pin23) of the microprocessor. The voltage input to the microprocessor during transmission is digitized to drive the LCD battery display.

Lamp&LCD circuit

The LCD is turned on or off by directly flowing current to the microprocessor ports.

Battery save circuit

The squelch is switched in during receive. The power circuit enters battery save mode if no key has bean pressed for five seconds. This circuit is controlled by microprocessor.

CTCSS/DCS circuit

The sub-tone signal is produced by the serial data from Pin17(CTCSS) or Pin44(DCS) of microprocessor. When the sub-tone is transmitted, the CTCSS /DCS is output from the microprocessor and modulated, after through LPF. The audio signal detected output to the decoder of microprocessor. The DEV pin is made low when the tone frequency coincides. The microprocessor determines the DEV pin state.

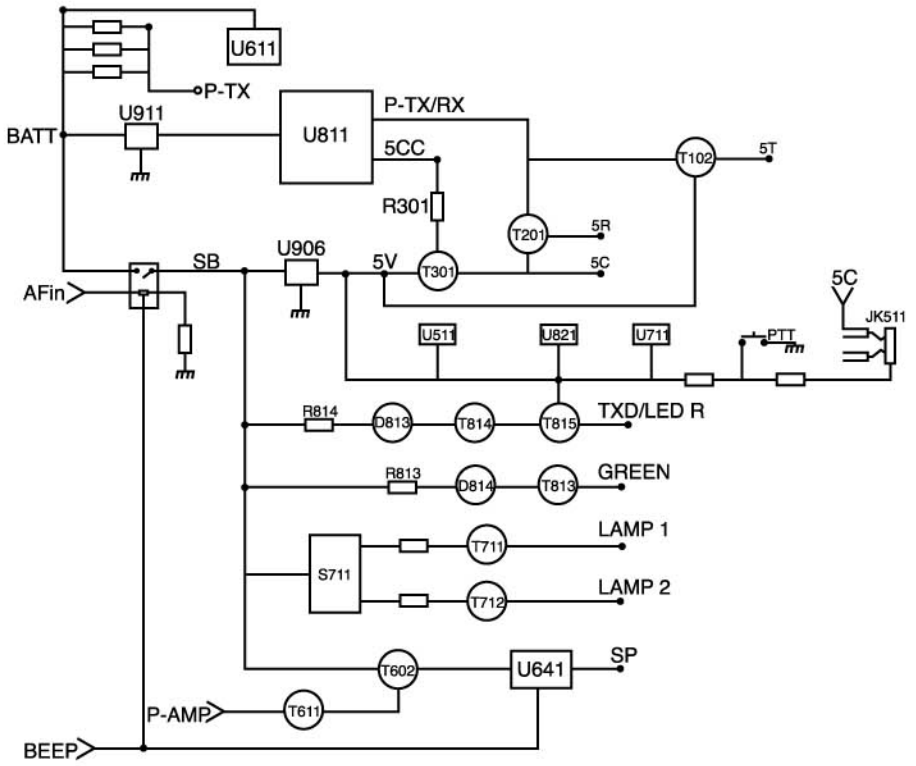

Fig.8

POWER SELECTOR CIRCUIT

The power circuit configuration is shown in Figure 8. The power circuit branches are as follows:

- BATT
  - RB — Power amplifier power supply voltage
  - 5M — Output 5M by U911 stabilized voltage circuit, microprocessor U811, Vdd, Avdd, 5CC control output by Pin38 of U811, VOX control voltage.
    5CC control 5V,output 5C reference voltage supply to VCO, Vdd and CR311,PLL,U311,Vdd.
  - SB
    - S711 Vdd
    - ASB — AF amplifier U641,Vdd.
    - Output 5V by U906 stabilized voltage circuit, P-TX/RX control transfer of Transmission/reception circuit.
      P-TX/RX control 5C,output 5R supply to receive stage voltage U261 Vdd, T261, T251, T231.
    - 5V — 5V output 5T supply to Transmission stage voltage.
      U511 Vdd, U821 Vdd, and U711 Vdd.
    - 5T — Transmission U411 switch, amplify and drive Vdd, protection circuit bias voltage, D156, D211, D212 switch (transmission/reception transfer switch)