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CONFIDENTIAL INFORMATION

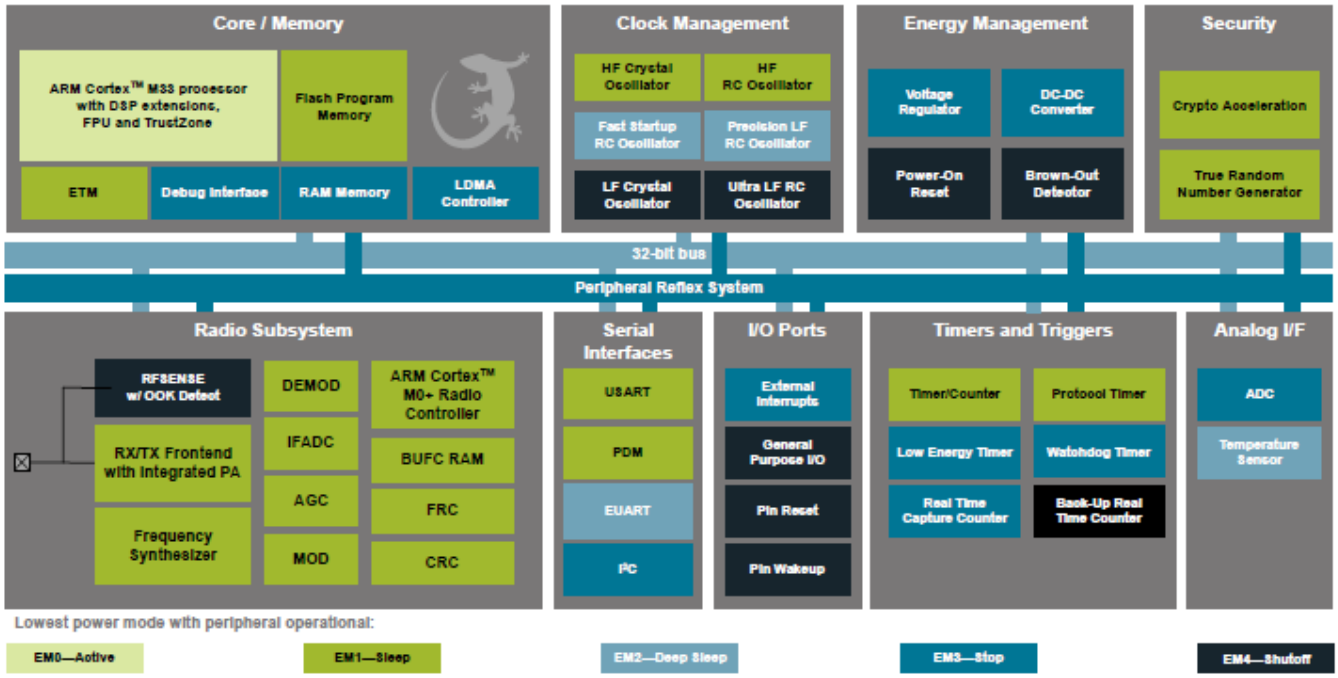
The F1LS3222 Wireless Gecko family of SoCs is part of the Wireless Gecko portfolio. F1LS3222 Wireless Gecko SoCs are ideal for enabling energy-friendly Bluetooth 5.2 networking for IoT devices.

The single-die solution combines a 38.4 MHz Cortex-M33 with a high performance 2.4 GHz radio to provide an industry-leading, energy efficient wireless, SoC for IoT connec-ted applications. Wireless Gecko applications include:

- Asset Tags and Beacons
- Consumer Electronics Remote Controls
- Portable Medical
- Bluetooth Mesh Low Power Nodes
- Sports, Fitness, and Wellness devices
- Connected Home
- Building Automation and Security

KEY FEATURES

- 32-bit ARM® Cortex®-M33 core with 38.4 MHz operating frequency
- Up to 352 kB of flash and 32 kB of RAM
- Energy-efficient radio core with low active and sleep currents
- Bluetooth 5.2
- Integrated PA with up to 6 dBm
- (2.4 GHz) TX power
- Secure Boot with Root of Trust and Secure Loader (RTSL)



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Bluetooth®

1. Feature List

The F1LS3222 highlighted features are listed below.

- **Low Power Wireless System-on-Chip**
  - High Performance 32-bit 38.4 MHz MHz ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient sig-nal processing
  - Up to 352 kB flash program memory
  - Up to 32 kB RAM data memory
  - 2.4 GHz radio operation
- **Radio Performance**
  - -98.9 dBm sensitivity @ 1 Mbit/s GFSK
  - TX power up to 6 dBm
  - 2.5 mA radio receive current
  - 3.4 mA radio transmit current @ 0 dBm output power
  - 7.5 mA radio transmit current @ 6 dBm output power
- **Low System Energy Consumption**
  - 3.6 mA RX current (1 Mbps GFSK)
  - 8.2 mA TX current @ 6 dBm output power
  - 27 µA/MHz in Active Mode (EM0) at 76.8 MHz(optional)
  - 1.40 µA EM2 DeepSleep current (32 kB RAM retention and RTC running from LFXO)
  - 1.75 µA EM2 DeepSleep current (32 kB RAM retention and RTC running from Precision LFRCO)
  - 0.17 µA EM4 current
- **Supported Modulation Format**
  - 2 (G)FSK with fully configurable shaping
  - OQPSK DSSS
  - (G)MSK
- **Protocol Support**
  - Bluetooth Low Energy (Bluetooth 5.2)
  - Proprietary
- **Wide selection of MCU peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - Up to 18 General Purpose I/O pins with output state reten-tion and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 4 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 1 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 1 × Watchdog Timer
  - 2 × Universal Synchronous/Asynchronous Receiver/Trans-mitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - 1 × Enhanced Universal Asynchronous Receiver/Transmit-ter (EUART)
  - 2 × I^2C interface with SMBus support
  - Digital microphone interface (PDM)
  - Precision Low-Frequency RC Oscillator to replace 32 kHz sleep crystal
  - RFSENSE with selective OOK mode
  - Die temperature sensor with +/-1.5 degree C accuracy after single-point calibration
- **Wide Operating Range**
  - 1.71 V to 3.8 V single power supply
  - -40 °C to 85 ℃
- **Security Features**
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - Hardware Cryptographic Acceleration for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, and ECDH
  - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug with lock/unlock
- **Demensions**
  - 9.15 x 15.73 x 1.9mm

Bluetooth®

2. System Overview

2.1 Introduction

The F1LS3222 Module combines an energy-friendly MCU with a high performance radio transceiver. The devices are well suited for secure connected IoT multi-protocol devices requiring high performance and low energy consumption. This section gives a short intro-duction to the full radio and MCU system.

A block diagram of the F1LS3222 is shown in Figure 3.1

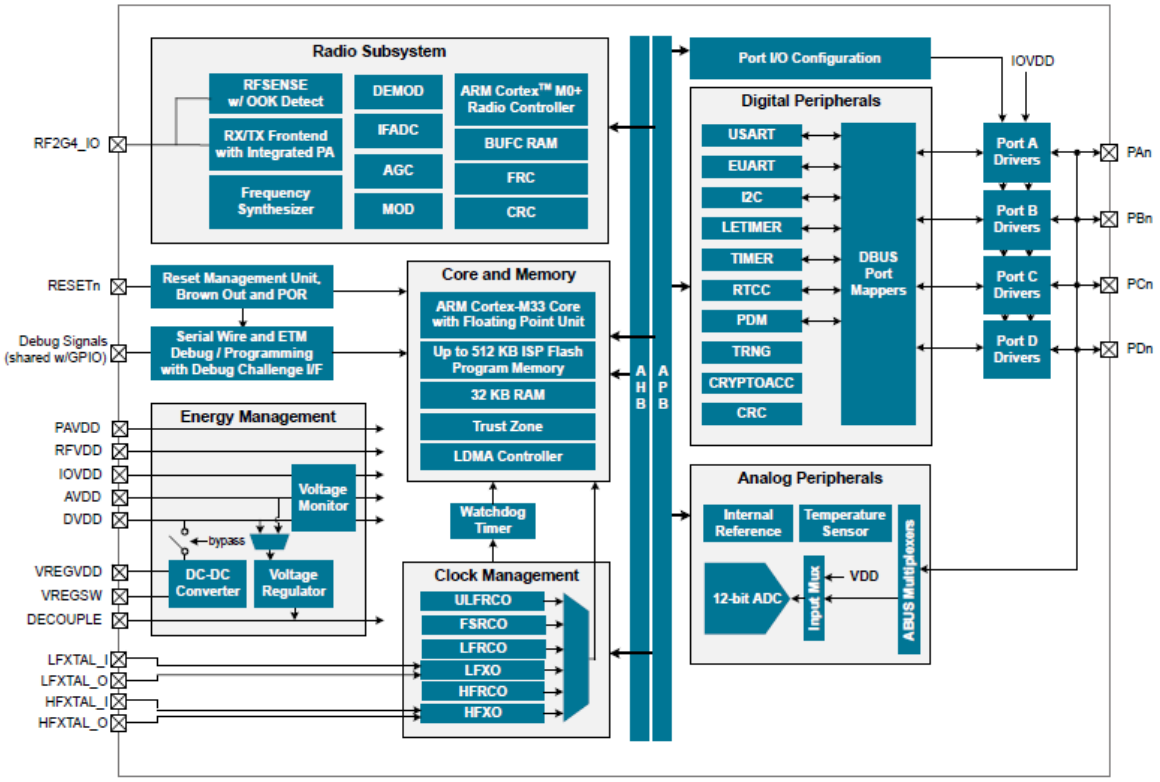

Figure 3.1. Detailed EFR32BG22 Block Diagram

2.2 Radio

The F1LS3222 features a highly configurable radio transceiver supporting the Bluetooth Low Energy wireless proto-col.

2.2.1 Antenna Interface

The F1LS3222 Module includes an integrated chip –antenna . The table below includes performance specifications for the integrated Chip-antenna.

2.2.2 Fractional-N Frequency Synthesizer

The F1LS3222 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency for the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance, frequency resolution better than 100 Hz, and low energy consumption. The synthesizer's fast frequency settling allows for very short receiver and transmitter wake up times to reduce system energy consumption.

2.2.3 Receiver Architecture

The F1LS3222 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, provid-ing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selec-tivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image rejection performance.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow re-ceive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF chan-nel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

2.2.4 Transmitter Architecture

The F1LS3222 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shap-ing.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the F1LS3222. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth be-tween devices that otherwise lack synchronized RF channel access.

2.2.5 Packet and State Trace

The F1LS3222 Frame Controller has a packet and state trace unit that provides valuable information during the development phase.
It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

2.2.6 Data Buffering

The F1LS3222 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

2.2.7 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the F1LS3222. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
  Detailed frame transmission timing, including optional LBT or CSMA-CA

2.2.8 RFSENSE Interface

The RFSENSE block allows the device to remain in EM2, EM3 or EM4 and wake when RF energy above a specified threshold is detec-ted. When operated in selective mode, the RFSENSE block performs OOK preamble and sync word detection, preventing false wake-up events.

2.3 General Purpose Input/Output (GPIO)

F1LS3222 has up to 26 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripher-als. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by Low-Energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have EM4 wake functionality. These pins are listed in the Alternate Function Table.

2.4 Clocking

2.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the F1LS3222. Individual enabling and disabling of clocks to all periph-eral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

2.4.2 Internal and External Oscillators

The F1LS3222 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing refer-ence for the MCU. The HFXO provides excellent RF clocking performance using a 38.4 MHz crystal. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature.

- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.

- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 MHz to 38.4 MHz.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz

- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation without an external crystal. Precision mode enables periodic recalibration against the 38.4 MHz HFXO crystal to improve accuracy to +/- 500 ppm, suitable for BLE sleep inter-val timing.

- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy con-sumption in low energy modes.

2.5 Counters/Timers and PWM

2.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 16-bit or 32-bit counter with up to 3 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers. In addition some timers offer dead-time insertion.

2.5.2 Low Energy Timer (LETIMER)

The unique LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of wave-forms with minimal software intervention. The LETIMER is connected to the Peripheral Reflex System (PRS), and can be configured to start counting on compare matches from other peripherals such as the RTCC.

2.5.3 Real Time Clock with Capture (RTCC)

The Real Time Clock with Capture (RTCC) is a 32-bit counter providing timekeeping down to EM3. The RTCC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined intervals.

A secondary RTC is used by the RF protocol stack for event scheduling, leaving the primary RTCC block available exclusively for appli-cation software.

3.5.4 Back-Up Real Time Counter

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined inver-vals.

2.5.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

2.6 Communications and Other Digital Peripherals

2.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices sup-porting:

- ISO7816 SmartCards
- IrDA
- I^2S

2.6.2 Enhanced Universal Asynchronous Receiver/Transmitter (EUART)

The Enhanced Universal Asynchronous Receiver/Transmitter supports full duplex asynchronous UART communication with hardware flow control, RS-485 and IrDA support. In EM0 and EM1 the EUART provides a high-speed, buffered communication interface.

When routed to GPIO ports A or B, the EUART may also be used in a low-energy mode and operate in EM2. A 32.768 kHz clock source allows full duplex UART communication up to 9600 baud.

2.6.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated trans-fers.

Automatic recognition of slave addresses is provided in active and low energy modes. Note that not all instances of I^2C are avalia-ble in all energy modes.

2.6.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer periph-erals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

2.6.5 Pulse Density Modulation (PDM) Interface

The PDM module provides a serial interface and decimation filter for Pulse Density Modulation (PDM) microphones, isolated Sigma-delta ADCs, digital sensors and other PDM or sigma delta bit stream peripherals. A programmable Cascaded Integrator Comb (CIC) filter is used to decimate the incoming bit streams. PDM supports stereo or mono input data and DMA transfer.

2.7 Security Features

The following security features are available on the F1LS3222:

- Secure Boot with Root of Trust and Secure Loader (RTSL)
- Cryptographic Accelerator
- True Random Number Generator (TRNG)
- Secure Debug with Lock/Unlock

2.7.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).
It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed and protects Over The Air updates.

2.7.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to pro-tect keys.
It supports AES encryption and decryption with 128/192/256-bit keys, Elliptic Curve Cryptography(ECC) to support public key opera-tions and hashes.
Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)
- CCM (Counter with CBC-MAC)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192 and P-256 for ECDH(Elliptic Curve Diffie-Hellman) key derivation and ECDSA (El-liptic Curve Digital Signature Algorithm) sign and verify operations.
Supported hashes include SHA-1, SHA2/224, and SHA-2/256.
This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

2.7.3 True Random Number Generator

The True Random Number Generator module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31 as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

2.7.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

In addition, the Secure Element also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

2.8 Analog

2.8.1 Analog to Digital Converter (IADC)

The IADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style converters. It has a resolution of up to 12 bits at up to 1 Msps. Hardware oversampling reduces system-level noise over multiple front-end samples. The IADC includes integrated voltage references. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

2.9 Power

The F1LS3222 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capaci-tor.

The F1LS3222 device includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

2.9.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to implement system-wide voltage scaling and turn off the power to unused RAM blocks to optimize the energy consumption in the target application. The DC-DC regula-tor operation is tightly integrated with the EMU.

2.9.2 Voltage Scaling

The F1LS3222 supports supply voltage scaling for the LDO powering DECOUPLE, with independent selections for EM0 / EM1 and EM2 / EM3. Voltage scaling helps to optimize the energy efficiency of the system by operating at lower voltages when possible. The default EM0 / EM1 voltage scaling level is VSCALE2, which allows the core to operate in active mode at full speed. The intermediate level, VSCALE1, allows operation in EM0 and EM1 at up to 40 MHz. The lowest level, VSCALE0, can be used to conserve power in EM2 and EM3. The EMU will automatically switch the target voltage scaling level when transitioning between energy modes.

2.9.3 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents, provides high efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 60 mA for device and radio operation. RF noise mitigation allows operation of the DC-DC converter without signifi-cantly degrading sensitivity of radio components. An on-chip supply-monitor signals when the supply voltage is low to allow bypass of the regulator via programmable software interrupt. It employs soft switching at boot and DCDC regulating-to-bypass transitions to limit the max supply slew-rate and mitigate inrush current.

2.9.4 Power Domains

The F1LS3222 has three peripheral power domains for operation in EM2 and EM3, as well as the ability to selectively retain configu-rations for EM0/EM1 peripherals. A small set of peripherals always remain powered on in EM2 and EM3, including all peripherals which are available in EM4. If all of the peripherals in PD0B or PD0C are configured as unused, that power domain will be powered off in EM2 or EM3, reducing the overall current consumption of the device. Likewise, if the application can tolerate the setup time to re-configure used EM0/EM1 peripherals on wake, register retention for these peripherals can be disabled to further reduce the EM2 or EM3 current.

Table 3.1. Peripheral Power Subdomains

Always available in EM2/EM3	Power Domain PD0B	Power Domain PD0C
RTCC	LETIMER0	LFRCO (Precision Mode)
LFRCO (Non-precision mode)[1]	IADC0	
LFXO[1]	I2C0	
BURTC[1]	WDOG0	
RFSENSE[1]	EUART0	
ULFRCO[1]	PRS	
FSRCO	DEBUG	

Note:
1. Peripheral also available in EM4.

2.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the F1LS3222. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

2.11 Core and Memory

2.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 352 kB flash program memory
- Up to 32 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

2.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. In addition to the main flash array where Program code is normally written the MSC also provides an Information block where additional information such as special user information or flash-lock bits are stored. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

2.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling so-phisticated operations to be implemented.

2.12 Memory Map

The F1LS3222 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

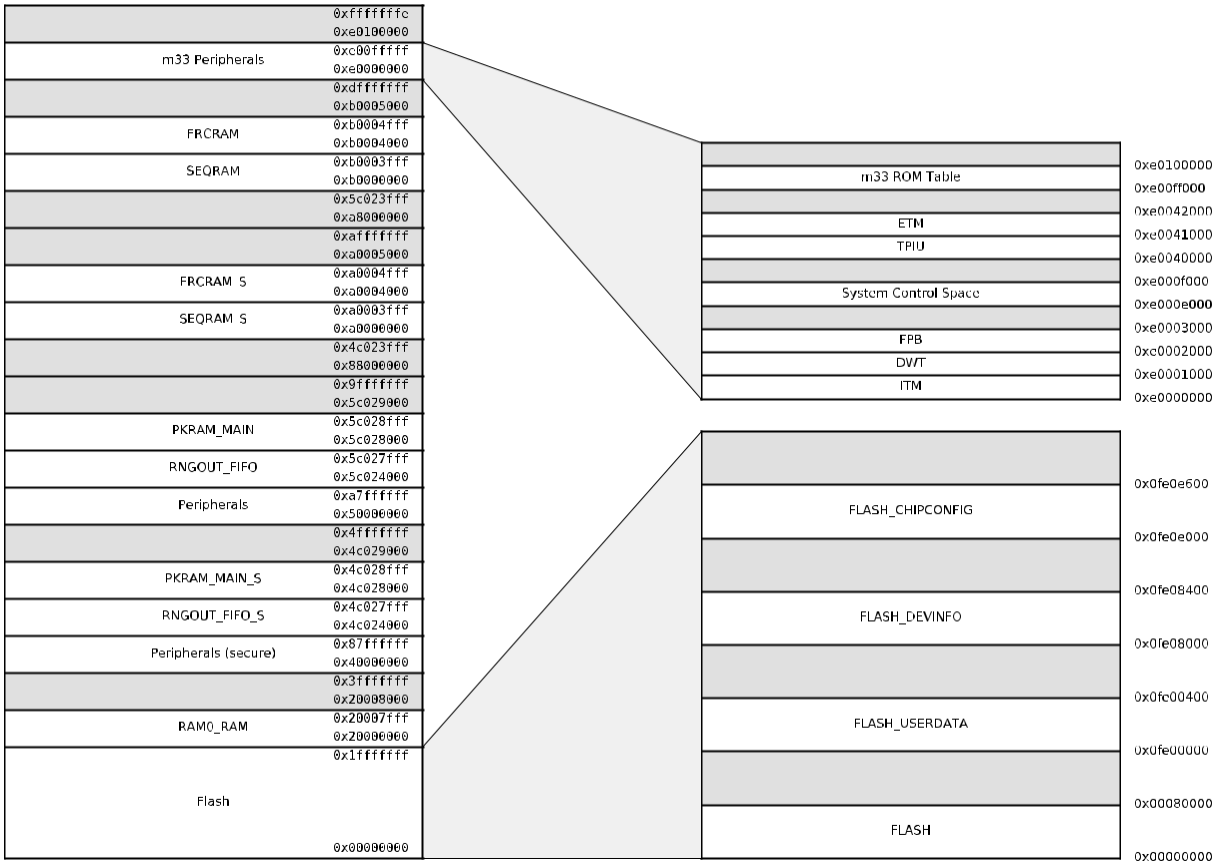

Figure 3.2. F1LS3222 Memory Map — Core Peripherals and Code Space

2.13 Configuration Summary

The features of the F1LS3222 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

Module	Lowest Energy Mode	Configuration
I2C0	EM2[1]	
I2C1	EM1	
IADC0	EM2	
LETIMER0	EM2[1]	
PDM	EM1	2-channel
TIMER0	EM1	32-bit, 3-channels, +DTI
TIMER1	EM1	16-bit, 3-channels, +DTI
TIMER2	EM1	16-bit, 3-channels, +DTI
TIMER3	EM1	16-bit, 3-channels, +DTI
TIMER4	EM1	16-bit, 3-channels, +DTI
EUART0	EM1 - Full high-speed operation EM2[1] - Low-energy operation, 9600 Baud	
USART0	EM1	+IrDA, +I2S, +SmartCard
USART1	EM1	+IrDA, +I2S, +SmartCard

Note:

1. EM2 and EM3 operation is only supported for digital peripheral I/O on Port A and Port B. All GPIO ports support digital peripheral operation in EM0 and EM1.

3. Electrical Specifications

3.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and all supplies at 3.0 V, by production test and/or technology characterization.

- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output pow-er-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

3.2 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	+85	℃
Voltage on any supply pin[1]	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.4	V
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{IOVDD} + 0.3	V
DC voltage on RESETn pin	V_{RESETn}		-0.3	—	3.8	V
Absolute voltage on RF pin RF2G4_IO	V_{MAX2G4}		-0.3	—	V_{PAVDD} + 0.3	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

Note:

1. The maximum supply voltage on VREGVDD is limited under certain conditions when using the DC-DC. See the DC-DC specifica-tions for more details.

3.3 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating temperature range	T_A	- Ambient temperature range	-40	—	+85	℃
DVDD supply voltage	V_{DVDD}	EM0/1	1.71	3.0	3.8	V
		EM2/3/4[2]	1.71	3.0	3.8	V
AVDD supply voltage	V_{AVDD}		1.71	3.0	3.8	V
IOVDDx operating supply voltage (All IOVDD pins)	V_{IOVDDx}		1.71	3.0	3.8	V
PAVDD operating supply voltage	V_{PAVDD}		1.71	3.0	3.8	V
VREGVDD operating supply voltage	$V_{VREGVDD}$	DC-DC in regulation[3]	2.2	3.0	3.8	V
		DC-DC in bypass 60 mA load	1.8	3.0	3.8	V
		DC-DC not in use. DVDD externally shorted to VREGVDD	1.71	3.0	3.8	V
RFVDD operating supply voltage	V_{RFVDD}		1.71	3.0	V_{PAVDD}	V
DECOUPLE output capacitor[4]	$C_{DECOUPLE}$	1.0 µF ± 10% X8L capacitor used for performance characterization.	1.0	—	2.75	µF
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	76.8	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
		VSCALE1, MODE = WS0	—	—	40	MHz
PCLK frequency	f_{PCLK}	VSCALE2	—	—	50	MHz
		VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	76.8	MHz
		VSCALE1	—	—	40	MHz
EM01 Group B clock frequency	$f_{EM01GRPBCLK}$	VSCALE2	—	—	76.8	MHz
		VSCALE1	—	—	40	MHz
Radio HCLK frequency[5]	f_{RHCLK}	VSCALE2 or VSCALE1	—	38.4	—	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. $T_A = T_{JMAX}$ - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_{JMAX} and $THETA_{JA}$.

2. The DVDD supply is monitored by the DVDD BOD in EM0/1 and the LE DVDD BOD in EM2/3/4.

3. The maximum supply voltage on VREGVDD is limited under certain conditions when using the DC-DC. See the DC-DC specifica-tions for more details.
4. Murata GCM21BL81C105KA58L used for performance charaacterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 0.6 µF.

5. The recommended radio crystal frequency is 38.4 MHz. Any crystal frequency other than 38.4 is expressly not supported. See HFXO specifications for more detail on crystal tolerance.

3.4 DC-DC Converter

Test conditions: L_{DCDC} = 2.2 µH (Samsung CIG22H2R2MNE), C_{DCDC} = 4.7 µF (Samsung CL10B475KQ8NQNC), $V_{VREGVDD}$ = 3.0 V, V_{OUT} = 1.8 V, IPKVAL in EM0/1 modes is set to 150 mA, and in EM2/3 modes is set to 90 mA, unless otherwise indicated.

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range at VREGVDD pin[1]	^{V}VREGVDD	DCDC in regulation, I_{LOAD} = 60 mA, EM0/EM1 mode	2.2	3.0	3.8*	V
		DCDC in regulation, I_{LOAD} = 5 mA, EM0/EM1 or EM2/EM3 mode	1.8	3.0	3.8*	V
		Bypass mode	1.8	3.0	3.8	V
Regulated output voltage	^{V}OUT		—	1.8	—	V
Regulation DC accuracy	ACC_{DC}	$V_{VREGVDD}$ ≥ 2.2 V, Steady state in EM0/EM1 mode or EM2/EM3 mode	-2.5	—	3.3	%
Regulation total accuracy	^{ACC}TOT	With mode transitions between EM0/EM1 and EM2/EM3 modes	-5	—	7	%
Steady-state output ripple	V_R	I_{LOAD} = 20 mA in EM0/EM1 mode	—	14.3	—	mVpp
DC line regulation	^{V}REG	I_{LOAD} = 60 mA in EM0/EM1 mode, $V_{VREGVDD}$ ≥ 2.2 V	—	5.5	—	mV/V
DC load regulation	^{I}REG	Load current between 100 µA and 60 mA in EM0/EM1 mode	—	0.27	—	mV/mA
Efficiency	EFF	Load current between 100 µA and 60 mA in EM0/EM1 mode, or between 10 µA and 5 mA in EM2/EM3 mode	—	91	—	%
Output load current	^{I}LOAD	EM0/EM1 mode, DCDC in regulation	—	—	60	mA
		EM2/EM3 mode, DCDC in regulation	—	—	5	mA
		Bypass mode	—	—	60	mA
Nominal output capacitor	^{C}DCDC	4.7 µF ± 10% X7R capacitor used for performance characterization[2]	4.7	—	10	µF
Nominal inductor	^{L}DCDC	± 20% tolerance	—	2.2	—	µH
Nominal input capacitor	^{C}IN		^{C}DCDC	—	—	µF
Resistance in bypass mode	^{R}BYP	Bypass switch from VREGVDD to DVDD, $V_{VREGVDD}$ = 1.8 V	—	1.75	3	Ω
		Powertrain PFET switch from VREGVDD to VREGSW, ^{V}VREGVDD = 1.8 V	—	0.86	1.5	Ω
Supply monitor threshold programming range	^{V}CMP_RNG	Programmable in 0.1 V steps	2.0	—	2.3	V
Supply monitor threshold accuracy	^{V}CMP_ACC	Supply falling edge trip point	TBD	—	TBD	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply monitor threshold hysteresis	^{V}CMP_HYST	Positive hysteresis on the supply rising edge referred to the falling edge trip point	—	4	—	%
Supply monitor response time	^{t}CMP_DELAY	Supply falling edge at -100 mV / µs	—	0.6	—	µs

Note:

1. The supported maximum $V_{VREGVDD}$ in regulation mode is a function of temperature and 10-year lifetime average load current.
2. Samsung CL10B475KQ8NQNC used for performance charaacterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 2.4 µF.

3.6 Current Consumption

3.6.1 MCU current consumption using DC-DC at 3.0 V input

Unless otherwise indicated, typical conditions are: VREGVDD = 3.0 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V from DC-DC. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.5. MCU current consumption using DC-DC at 3.0 V input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	28	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	27	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	37	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	28	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	26	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	38	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	22	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	24	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	27	—	µA/MHz
		1 MHz HFRCO, CPU running	—	159	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	17	—	µA/MHz
		38.4 MHz crystal	—	17	—	µA/MHz
		38 MHz HFRCO	—	13	—	µA/MHz
		26 MHz HFRCO	—	15	—	µA/MHz
		16 MHz HFRCO	—	18	—	µA/MHz
		1 MHz HFRCO	—	150	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	1.40	—	µA
		Full RAM retention and RTC running from LFRCO	—	1.40	—	µA
		Full RAM retention and RTC running from LFRCO in precision mode	—	1.75	—	µA
		24 kB RAM retention and RTC running from LFXO	—	1.32	—	µA
		24 kB RAM retention and RTC running from LFRCO in precision mode	—	1.66	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.21	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.20	—	µA
		8 kB RAM retention and RTC running from LFXO, Radio RAM and CPU cache not retained	—	1.03	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	1.05	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	0.37	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See for a list of the peripherals in each power domain.

3.6.4 Radio current consumption at 3.0V using DCDC

RF current consumption measured with MCU in EM1, HCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indica-ted, typical conditions are: VREGVDD = 3.0V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.8. Radio current consumption at 3.0V using DCDC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System current consumption in receive mode, active pack-et reception	I_{RX_ACTIVE}	1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)[1]	—	3.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1 [1]	—	3.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2 [1]	—	3.9	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System current consumption in receive mode, listening for packet	I_{RX_LISTEN}	1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks	—	3.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1 [1]	—	3.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2 [1]	—	4.0	—	mA
System current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	4.1	—	mA
		f = 2.4 GHz, CW, 6 dBm PA, 6 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	8.2	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1	—	4.3	—	mA
		f = 2.4 GHz, CW, 6 dBm PA, 6 dBm output power, VSCALE1	—	8.4	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE2	—	4.4	—	mA
		f = 2.4 GHz, CW, 6 dBm PA, 6 dBm output power, VSCALE2	—	8.5	—	mA

Note:

1. Direction-finding phy adds approximately 150 µA to the receive current.

3.7 Flash Characteristics

Table 4.9. Flash Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash Supply voltage during write or erase	^{V}FLASH		1.71	—	3.8	V
Flash erase cycles before failure[1]	^{EC}FLASH	$T_A \leq 125$ °C	10,000	—	—	cycles
Flash data retention[1]	^{RET}FLASH	$T_A \leq 125$ °C	10	—	—	years
Program Time	^{t}PROG	one word (32-bits)	42.1	44	45.6	uSec
		average per word over 128 words	10.3	10.9	11.3	uSec
Page Erase Time	^{t}PERASE		11.4	12.9	14.4	ms
Mass Erase Time	^{t}MERASE	Erases all of User Code area	11.7	13	14.3	ms
Program Current	^{I}PROG		—	—	1.45	mA
Page Erase Current	^{I}PERASE	Page Erase	—	—	1.34	mA
Mass Erase Current	^{I}MERASE	Mass Erase	—	—	1.28	mA

Note:
1. Flash data retention information is published in the Quarterly Quality and Reliability Report.

3.8 Wake Up, Entry, and Exit times

Unless otherwise specified, these times are measured using the HFRCO at 19 MHz.

Table 4.10. Wake Up, Entry, and Exit times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
WakeupTime from EM1	t_{EM1_WU}	Code execution from flash	—	3	—	AHB Clocks
		Code execution from RAM	—	1.42	—	µs
WakeupTime from EM2	t_{EM2_WU}	Code execution from flash, No Voltage Scaling	—	13.22	—	µs
		Code execution from RAM, No Voltage Scaling	—	5.15	—	µs
		Voltage scaling up one level[1]	—	37.89	—	µs
		Voltage scaling up two levels[2]	—	50.56	—	µs
WakupTime from EM3	t_{EM3_WU}	Code execution from flash, No Voltage Scaling	—	13.21	—	µs
		Code execution from RAM, No Voltage Scaling	—	5.15	—	µs
		Voltage scaling up one level[1]	—	37.90	—	µs
		Voltage scaling up two levels[2]	—	50.55	—	µs
WakeupTime from EM4	t_{EM4_WU}	Code execution from flash	—	8.81	—	ms
Entry time to EM1	t_{EM1_ENT}	Code execution from flash	—	1.29	—	µs
Entry time to EM2	t_{EM2_ENT}	Code execution from flash	—	5.23	—	µs
Entry time to EM3	t_{EM3_ENT}	Code execution from flash	—	5.23	—	µs
Entry time to EM4	t_{EM4_ENT}	Code execution from flash	—	9.96	—	µs
Voltage scaling in time in EM0[3]	t_{SCALE}	Up from VSCALE1 to VSCALE2	—	32	—	µs
		Down from VSCALE2 to VSCALE1	—	172	—	µs

Note:

1. Voltage scaling one level is between VSCALE0 and VSCALE1 or between VSCALE1 and VSCALE2.
2. Voltage scaling two levels is between VSCALE0 and VSCALE2.
3. During voltage scaling in EM0, RAM is inaccessible and processor will be halted until complete.

3.9 RFSENSE Low-energy Wake-on-RF

Table 4.11. RFSENSE Low-energy Wake-on-RF

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Average current	$I_{RFSENSE}$	RF energy below wake threshold	—	138	—	nA
		Selective mode, RF energy above threshold but no OOK sync detected	—	131	—	nA
RF level above which RFSENSE will detect signal[1]	$THRES_{TRIG}$	Threshold set to -34 dBm	-28	—	—	dBm
		Threshold set to -22 dBm	-19	—	—	dBm
RF level below which RFSENSE will not detect signal[1]	$^{THRES}NOTRIG$	Threshold set to -34 dBm	—	—	-40	dBm
		Threshold set to -22 dBm	—	—	-26	dBm
Sensitivity in selective OOK mode[1]	$SENS_{OOK}$	Sensitivity for > 90% probability of OOK detection[2], threshold set to -34 dBm	-28	—	—	dBm
		Sensitivity for > 90% probability of OOK detection[2], threshold set to -22 dBm	-19	—	—	dBm

Note:

1. Values collected with conducted measurements performed at the end of the matching network.
2. Selective wake signal is 1 kHz OOK Manchester-coded, 8 bits of preamble, 32-bit sync word.

3.10 2.4 GHz RF Transceiver Characteristics

3.10.1 RF Transmitter Characteristics

3.10.1.1 RF Transmitter General Characteristics for the 2.4 GHz Band(Conducted)

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.12. RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	^{F}RANGE		2400	—	2483.5	MHz
Radio-only current consumption while transmitting[1]	^{I}TX_RADIO	f = 2.4 GHz, CW, 6 dBm PA, 6 dBm output power	—	7.5	—	mA
Maximum TX power[2]	$POUT_{MAX}$	6 dBm PA[3]	—	6	—	dBm
Minimum active TX power	$POUT_{MIN}$	6 dBm PA	—	-27	—	dBm
Output power variation vs supply voltage variation, frequency = 2450 MHz	^{POUT}VAR_V	6 dBm PA output power, using DCDC with VREGVDD swept from 1.8 to 3.0 V	—	0.04	—	dB
Output power variation vs temperature, Frequency = 2450 MHz	^{POUT}VAR_T	6 dBm PA at 6 dBm, (-40 to +125 °C)	—	0.18	—	dB
		6 dBm PA at 6 dBm, (-40 to +85 °C)	—	0.17	—	dB
Output power variation vs RF frequency	^{POUT}VAR_F	6 dBm PA, 6 dBm	—	0.20	—	dB
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	^{SPUR}HRM_FCC_R	Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz.	—	-47	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part	^{SPUR}OOB_FCC_R	Restricted bands 30-88 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	^{SPUR}OOB_FCC_NR	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-26	—	dBc
Spurious emissions per ETSI EN300.440	^{SPUR}ETSI440	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-60	—	dBm
		25-1000 MHz, excluding above frequencies. P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-42	—	dBm
		1G-14G, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-36	—	dBm
Spurious emissions out-of-band, per ETSI 300.328	^{SPUR}ETSI328	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-862 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-60	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 862-1000 MHz , P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-42	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-16	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Supply current to radio, supplied by DC-DC with 3.0 V, measured at VREGVDD.
2. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices cov-ered in this data sheet can be found in the Max TX Power column of the Ordering Information Table.
3. The PA is capable of delivering higher than 6 dBm output power. Howev-er, all transmitter characteristics and recommended application circuits are specified at 6 dBm output. If used with the recommen-ded application circuits above 6 dBm, harmonics may be higher than regulatory limits.

3.10.1.2 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate(Conducted)

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.13. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 6 dBm	—	630	—	kHz
Power spectral density limit	^{PSD}LIMIT	P_{out} = 6 dBm, Per FCC part 15.247 at 6 dBm	—	2.9	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	7.1	—	dBm
Occupied channel bandwidth per ETSI EN300.328	^{OCP}ETSI328	P_{out} = 6 dBm 99% BW at highest and lowest channels in band	—	1.1	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 6 dbm, Inband spurs at ± 2 MHz	—	-41	—	dBm
		P_{out} = 6 dBm Inband spurs at ± 3 MHz	—	-47	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

3.10.2 RF Receiver Characteristics

3.10.2.1 RF Receiver General Characteristics for the 2.4 GHz Band(Conducted)

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.18. RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	^{F}RANGE		2400	—	2483.5	MHz
Radio-only current consumption in receive mode[1]	^{I}RX_RADIO		—	2.5	—	mA
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-63	—	dBm
		1 GHz to 12 GHz	—	-53	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	^{SPUR}RX_FCC	216 MHz to 960 MHz, conducted measurement	—	-47	—	dBm
		Above 960 MHz, conducted measurement.	—	-47	—	dBm
2GFSK Sensitivity	^{SENS}2GFSK	2 Mbps 2GFSK signal, 1% PER	—	-93	—	dBm
		250 kbps 2GFSK signal, 0.1% BER	—	-104	—	dBm

Note:

1. Supply current to radio, supplied by DC-DC with 3.0 V, measured at VREGVDD.

3.10.2.2 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate(Conducted)

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz, Packet length is 255 bytes.

Table 4.19. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[1]	—	-98.9	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-97.4	—	dBm
		With non-ideal signals[2 1]	—	-96.9	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	8.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 4 3 5]	—	-6.6	—	dB
		Interferer is reference signal at -1 MHz offset[1 4 3 5]	—	-6.5	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 4 3 5]	—	-40.9	—	dB
		Interferer is reference signal at -2 MHz offset[1 4 3 5]	—	-39.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 4 3 5]	—	-45.9	—	dB
		Interferer is reference signal at -3 MHz offset[1 4 3 5]	—	-46.2	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-23.5	—	dB
Selectivity to image frequency ± 1 MHz	$^{C/I}$IM_1	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 5]	—	-40.9	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5]	—	-6.6	—	dB
Intermodulation performance	IM	n = 3 (see note[6])	—	-17.1	—	dBm

Note:

1. 0.1% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -67 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.
6. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

3.11 Oscillators

3.11.1 High Frequency Crystal Oscillator

Table 4.24. High Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	^{F}HFXO	see note[1]	—	38.4	—	MHz
Supported crystal equivalent series resistance (ESR)	^{ESR}HFXO_38M4	38.4 MHz, CL = 10 pF[2 3]	—	40	TBD	Ω
Supported range of crystal load capacitance[4]	^{C}HFXO_LC	38.4 MHz, ESR = 40 Ohm[3]	—	10	—	pF
Supply Current	^{I}HFXO		—	415	—	µA
Startup Time	^{T}STARTUP	38.4 MHz, ESR = 40 Ohm, CL = 10 pF	—	160	—	µs
On-chip tuning cap step size[5]	^{SS}HFXO		—	0.04	—	pF

3.11.2 Low Frequency Crystal Oscillator

Table 4.25. Low Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	^{F}LFXO		—	32.768	—	kHz
Supported Crystal equivalent series resistance (ESR)	^{ESR}LFXO	GAIN = 0	—	—	80	kΩ
		GAIN = 1 to 3	—	—	100	kΩ
Supported range of crystal load capacitance [1]	^{C}LFXO_CL	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2	10	—	12.5	pF
		GAIN = 3 (see note[2])	12.5	—	18	pF
Current consumption	^{I}CL12p5	ESR = 70 kOhm, CL = 12.5 pF, GAIN[3] = 2, AGC[4] = 1	—	357	—	nA
Startup Time	^{T}STARTUP	ESR = 70 kOhm, CL = 7 pF, GAIN[3] = 1, AGC[4] = 1	—	63	—	ms
On-chip tuning cap step size	^{SS}LFXO		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting[5]	^{C}LFXO_MIN	CAPTUNE = 0	—	4	—	pF
On-chip tuning capacitor value at maximum setting[5]	^{C}LFXO_MAX	CAPTUNE = 0x4F	—	24.5	—	pF

3.11.3 High Frequency RC Oscillator (HFRCO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.26. High Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	^{F}HFRCO_ACC	For all production calibrated frequencies	-3	—	3	%
Current consumption on all supplies [1]	^{I}HFRCO	F_{HFRCO} = 1 MHz	—	28	—	µA
		F_{HFRCO} = 2 MHz	—	28	—	µA
		F_{HFRCO} = 4 MHz	—	28	—	µA
		F_{HFRCO} = 5 MHz	—	30	—	µA
		F_{HFRCO} = 7 MHz	—	60	—	µA
		F_{HFRCO} = 10 MHz	—	66	—	µA
		F_{HFRCO} = 13 MHz	—	79	—	µA
		F_{HFRCO} = 16 MHz	—	88	—	µA
		F_{HFRCO} = 19 MHz	—	92	—	µA
		F_{HFRCO} = 20 MHz	—	105	—	µA
		F_{HFRCO} = 26 MHz	—	118	—	µA
		F_{HFRCO} = 32 MHz	—	141	—	µA
		F_{HFRCO} = 38 MHz	—	172	—	µA
		F_{HFRCO} = 80 MHz	—	289	—	µA
Clock out current for HFRCODPLL [2]	^{I}CLKOUT_HFRCOD PLL	FORECEEN bit of CTRL = 1 and the CLKOUTDIS0 bit of TEST = 1.	—	2.72	—	µA/MHz
		FORECEEN bit of CTRL i= 1 and the CLKOUTDIS1 bit of TEST = 1.	—	0.36	—	µA/MHz
Startup Time [3]	^{T}STARTUP	FREQRANGE = 0 to 7	—	1.2	—	µs
		FREQRANGE = 8 to 15	—	0.6	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Band Frequency Limits[4]	f_{HFRCO_BAND}	FREQRANGE = 0	3.71	—	5.24	MHz
		FREQRANGE = 1	4.39	—	6.26	MHz
		FREQRANGE = 2	5.25	—	7.55	MHz
		FREQRANGE = 3	6.22	—	9.01	MHz
		FREQRANGE = 4	7.88	—	11.6	MHz
		FREQRANGE = 5	9.9	—	14.6	MHz
		FREQRANGE = 6	11.5	—	17.0	MHz
		FREQRANGE = 7	14.1	—	20.9	MHz
		FREQRANGE = 8	16.4	—	24.7	MHz
		FREQRANGE = 9	19.8	—	30.4	MHz
		FREQRANGE = 10	22.7	—	34.9	MHz
		FREQRANGE = 11	28.6	—	44.4	MHz
		FREQRANGE = 12	33.0	—	51.0	MHz
		FREQRANGE = 13	42.2	—	64.6	MHz
		FREQRANGE = 14	48.8	—	74.8	MHz
		FREQRANGE = 15	57.6	—	87.4	MHz

3.11.4 Fast Start_Up RC Oscillator (FSRCO)

Table 4.27. Fast Start_Up RC Oscillator (FSRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FSRCO frequency	f_{FSRCO}		17.2	20	21.2	MHz

3.11.5 Precision Low Frequency RC Oscillator (LFRCO)

Table 4.28. Precision Low Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	^{F}LFRCO		—	32.768	—	kHz
Frequency accuracy	^{F}LFRCO_ACC	Normal mode	-3	—	3	%
		Precision mode[1], across operating temperature range[2]	-500	—	500	ppm
Startup time	^{t}STARTUP	Normal mode	—	204	—	µs
		Precision mode[1]	—	11.7	—	ms
Current consumption	^{I}LFRCO	Normal mode	—	175	—	nA
		Precision mode[1], T = stable at 25 °C [3]	—	655	—	nA

3.11.6 Ultra Low Frequency RC Oscillator

Table 4.29. Ultra Low Frequency RC Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation Frequency	^{F}ULFRCO		0.944	1.0	1.095	kHz

3.12 GPIO Pins (3V GPIO pins)

Table 4.30. GPIO Pins (3V GPIO pins)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	^{I}LEAK_IO	MODEx = DISABLED, IOVDD = 1.71 V	—	1.9	—	nA
		MODEx = DISABLED, IOVDD = 3.0 V	—	2.5	—	nA
		MODEx = DISABLED, IOVDD = 3.8V T_A=85°C	—	—	TBD	nA
		Pins other than PA00, PA03, PB00, PC03, PC04 and PD00; MODEx = DISABLED, IOVDD = 3.8 V T_A = 125 °C	—	—	200	nA
		Pins PA00, PA03, PB00, PC03, PC04 and PD00; MODEx = DISABLED, IOVDD = 3.8 V T_A = 125 °C	—	—	400	nA
Input low voltage[1]	^{V}IL	Any GPIO pin	—	—	0.3*IOVDD	V
		RESETn	—	—	0.3*DVDD	V
Input high voltage[1]	^{V}IH	Any GPIO pin	0.7*IOVDD	—	—	V
		RESETn	0.7*DVDD	—	—	V
Output high voltage	^{V}OH	Sourcing 20mA, IOVDD = 3.0 V	0.8 * IOVDD	—	—	V
		Sourcing 8mA, IOVDD = 1.71 V	0.6 * IOVDD	—	—	V
Output low voltage	^{V}OL	Sinking 20mA, IOVDD = 3.0 V	—	—	0.2 * IOVDD	V
		Sinking 8mA, IOVDD = 1.71 V	—	—	0.4 * IOVDD	V
GPIO rise time	^{T}GPIO_RISE	IOVDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
		IOVDD = 1.71 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	13	—	ns
GPIO fall time	^{T}GPIO_FALL	IOVDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
		IOVDD = 1.71 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	11.9	—	ns
Pull up/down resistance[2]	^{R}PULL	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0	35	44	55	kΩ
		RESETn pin. Pull-up to DVDD	35	44	55	kΩ
Maximum filtered glitch width	^{T}GF	MODE = INPUT, DOUT = 1	—	27	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

3.13 Analog to Digital Converter (IADC)

Specified at 1 Msps, ADCCLK = 10 MHz, OSR=2, unless otherwise indicated.

Table 4.31. Analog to Digital Converter (IADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main analog supply	^{V}AVDD	Normal Mode	1.71	—	3.8	V
Maximum Input Range	^{V}IN_MAX	Maximum allowable input voltage	0	—	AVDD	V
Full-Scale Voltage	^{V}FS	Voltage required for Full-Scale measurement	—	V_{REF} / Gain	—	
Input Measurement Range	^{V}IN	Differential Mode - Plus and Minus inputs	$-V_{FS}$	—	$+V_{FS}$	V
		Single Ended Mode - One input tied to ground	0	—	^{V}FS	V
Input Sampling Capacitance	Cs	Analog Gain = 1x	—	1.8	—	pF
		Analog Gain = 2x	—	3.6	—	pF
		Analog Gain = 4x	—	7.2	—	pF
		Analog Gain = 0.5x	—	0.9	—	pF
ADC clock frequency	^{f}CLK	Normal Mode	—	—	10	MHz
Throughput rate	^{f}SAMPLE	f_{CLK} = 10 MHz	—	—	1	Msps
Current from all supplies, Continuous operation	^{I}ADC_CONT	Normal Mode, 1 Msps, OSR=2, f_{CLK} = 10 MHz	—	290	385	µA
Current in Standby mode. ADC is not functional but can wake up in 1us.	^{I}STBY	Normal Mode	—	16	—	µA
ADC Startup Time	^{t}startup	From power down state	—	5	—	µs
		From Standby state	—	1	—	µs
ADC Resolution	Resolution		—	12	—	bits
Differential Nonlinearity	DNL	Differential Input. (No missing codes OSR =2	-1	+/- 0.25	1.5	LSB12
Integral Nonlinearity	INL	Normal Mode. Differential Input.	-2.5	+/- 0.65	2.5	LSB12
Effective number of bits	ENOB	Differential Input. Gain=1x, f_{IN} = 10 kHz, Internal VREF=1.21V. OSR=2	10.5	11.18	—	bits
Signal to Noise + Distortion Ratio Normal Mode	SNDR	Differential Input. Gain=1x, f_{IN} = 10 kHz, Internal VREF=1.21V	65	69.1	—	dB
		Differential Input. Gain=2x, f_{IN} = 10 kHz, Internal VREF=1.21V	—	68.8	—	dB
		Differential Input. Gain=4x, f_{IN} = 10 kHz, Internal VREF=1.21V	—	66.9	—	dB
		Differential Input. Gain=0.5x, f_{IN} = 10 kHz, Internal VREF=1.21V	—	69.2	—	dB
Total Harmonic Distortion	THD	Differential Input. Gain=1x, f_{IN} = 10 kHz, Internal VREF=1.21V	—	-80.3	-70	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious-Free Dynamic Range	SFDR	Differential Input. Gain=1x, f_{IN} = 10 kHz, Internal VREF=1.21V	72	86.5	—	dB
Common Mode Rejection Ratio	CMRR	Normal Mode. DC to 100 Hz	—	87.0	—	dB
		Normal Mode. AC high frequency	—	68.6	—	dB
Power Supply Rejection Ratio	PSRR	Normal mode. DC to 100 Hz	—	80.4	—	dB
		Normal mode. AC high frequency, using VREF pad.	—	33.4	—	dB
		Normal mode. AC high frequency, using internal VBGR.	—	65.2	—	dB
Gain Error	GE	GAIN=1 and 0.5, using external VREF, direct mode.	-0.3	0.069	0.3	%
		GAIN=2, using external VREF, direct mode.	-0.4	0.151	0.4	%
		GAIN=3, using external VREF, direct mode.	-0.7	0.186	0.7	%
		GAIN=4, using external VREF, direct mode.	-1.1	0.227	1.1	%
		Internal VREF, Gain = 1	—	0.023	—	%
Offset	OFFSET	GAIN=1 and 0.5, Differential Input	-3	0.27	3	LSB
		GAIN=2, Differential Input	-4	0.27	4	LSB
		GAIN=3, Differential Input	-4	0.25	4	LSB
		GAIN=4, Differential Input	-4	0.29	4	LSB
External reference voltage range	^{V}EVREF		1.0	—	AVDD	V
Internal Reference voltage	^{V}IVREF		—	1.21	—	V

3.15 Brown Out Detectors

3.15.1 DVDD BOD

BOD Thresholds on DVDD in EM0 and EM1 only, unless otherwise noted. Typical conditions are at T_A = 25 °C. Minimum and maxi-mum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating tem-perature range.

Table 4.33. DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	^{V}DVVD_BOD	Supply Rising	—	1.64	1.71	V
		Supply Falling	1.62	1.65	—	V
BOD response time	^{t}DVDD_BOD_DE-LAY	Supply dropping at 100mV/µs slew rate[1]	—	0.95	—	µs
BOD hysteresis	^{V}DVDD_BOD_HYST		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

3.15.2 LE DVDD BOD

BOD thresholds on DVDD pin for low energy modes EM2 to EM4, unless otherwise noted.

Table 4.34. LE DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	^{V}DVDD_LE_BOD	Supply Falling	1.5	—	1.71	V
BOD response time	^{t}DVDD_LE_BOD_D ELAY	Supply dropping at 2mV/µs slew rate[1]	—	50	—	µs
BOD hysteresis	^{V}DVDD_LE_BOD_HYST		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

3.15.3 AVDD and IOVDD BODs

BOD thresholds for AVDD BOD and IOVDD BOD. Available in all energy modes.

Table 4.35. AVDD and IOVDD BODs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	^{V}BOD	Supply falling	1.45	—	1.71	V
BOD response time	^{t}BOD_DELAY	Supply dropping at 2mV/µs slew rate[1]	—	50	—	µs
BOD hysteresis	^{V}BOD_HYST		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

3.16 PDM Timing Specifications

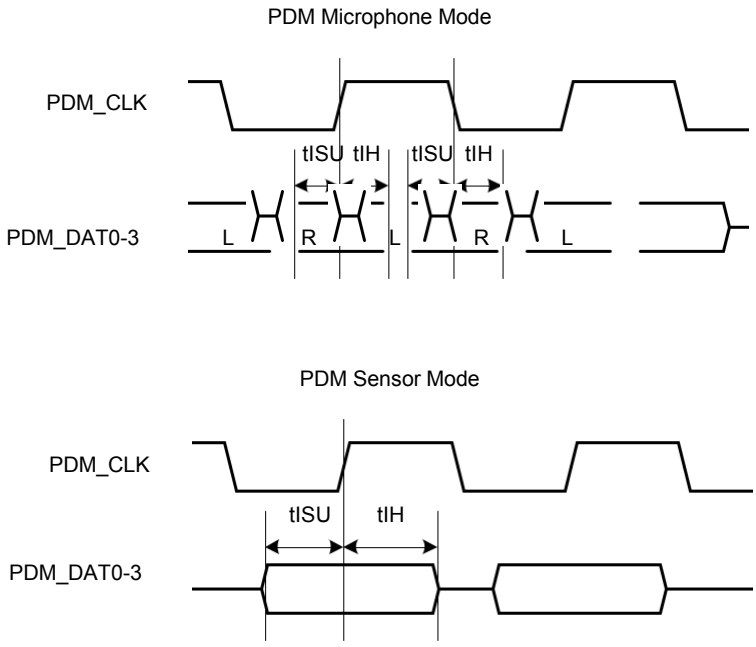


Figure 4.3. PDM Timing Diagrams

3.16.1 Pulse Density Modulator (PDM), Common DBUS

Timing specifications are for all PDM signals routed to the same DBUS (DBUSAB or DBUSCD), though routing to the same GPIO port is the optimal configuration. C_{LOAD} < 20 pF. System voltage scaling = VSCALE1 or VSCALE2. All GPIO set to slew rate = 6. Data delay (PDM_CFG1_DLYMUXSEL) = 0.

Table 4.36. Pulse Density Modulator (PDM), Common DBUS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PDM_CLK frequency during data transfer	^{F}PDM_CLK	Microphone mode	—	—	5	MHz
		Sensor mode	—	—	20	MHz
PDM_CLK duty cycle	^{DC}PDM_CLK		47.5	—	52.5	%
PDM_CLK rise time	t_R		—	—	5.5	ns
PDM_CLK fall time	t_F		—	—	5.5	ns
Input setup time	^{t}ISU	Microphone mode	30	—	—	ns
		Sensor mode	20	—	—	ns
Input hold time	^{t}IH		3	—	—	ns

3.17 USART SPI Master Timing

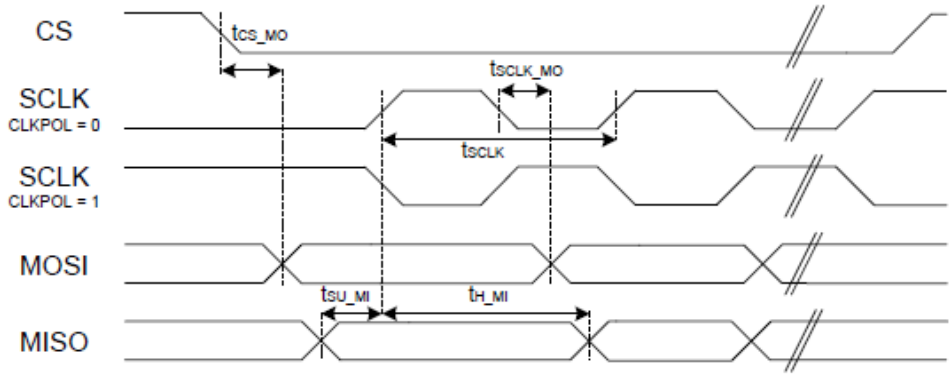


Figure 4.4. SPI Master Timing (SMSDELAY = 0)

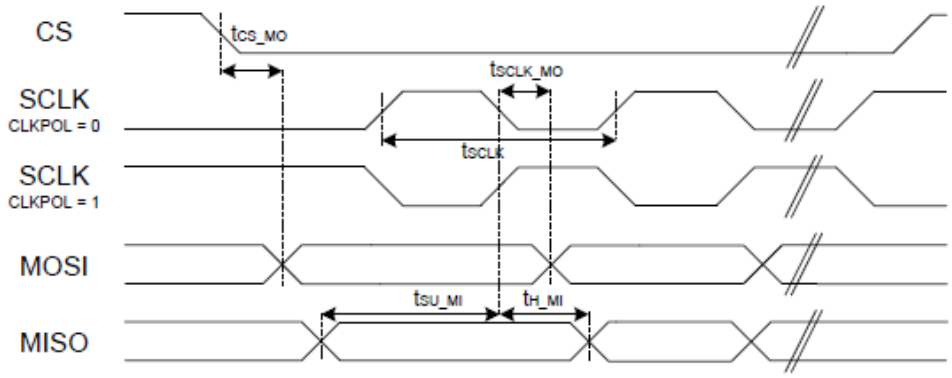


Figure 4.5. SPI Master Timing (SMSDELAY = 1)

3.17.1 SPI Master Timing, Voltage Scaling = VSCALE2

Table 4.37. SPI Master Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1 2 3]	^{t}SCLK		^{2*t}HFPERCLK	—	—	ns
CS to MOSI [1 2]	^{t}CS_MO		-22	—	22.5	ns
SCLK to MOSI [1 2]	^{t}SCLK_MO		-14.5	—	14.5	ns
MISO setup time [1 2]	^{t}SU_MI	IOVDD = 1.62 V	38.5	—	—	ns
		IOVDD = 3.0 V	28.5	—	—	ns
MISO hold time [1 2]	^{t}H_MI		-8.5	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD}.
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

3.17.2 SPI Master Timing, Voltage Scaling = VSCALE1

Table 4.38. SPI Master Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1 2 3]	^{t}SCLK		^{2*t}HFPERCLK	—	—	ns
CS to MOSI [1 2]	^{t}CS_MO		-33	—	34.5	ns
SCLK to MOSI [1 2]	^{t}SCLK_MO		-15	—	26	ns
MISO setup time [1 2]	^{t}SU_MI	IOVDD = 1.62 V	47	—	—	ns
		IOVDD = 3.0 V	39	—	—	ns
MISO hold time [1 2]	^{t}H_MI		-9.5	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD}.
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

3.18 USART SPI Slave Timing

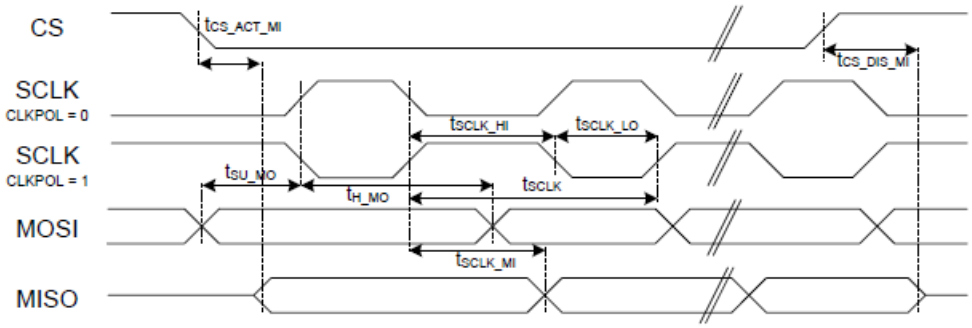


Figure 4.6. SPI Slave Timing

3.18.1 SPI Slave Timing, Voltage Scaling = VSCALE2

Table 4.39. SPI Slave Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2] [3]	t_{SCLK}		[6*]$t_{HFPERCLK}$	—	—	ns
SCLK high time [1] [2] [3]	t_{SCLK_HI}		2.5*$t_{HFPERCLK}$	—	—	ns
SCLK low time [1] [2] [3]	t_{SCLK_LO}		[2.5*]$t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [2]	$t_{CS\_ACT\_MI}$		25	—	47.5	ns
CS disable to MISO [1] [2]	$t_{CS\_DIS\_MI}$		19.5	—	38.5	ns
MOSI setup time [1] [2]	t_{SU_MO}		4.5	—	—	ns
MOSI hold time [1] [2] [3]	t_{H_MO}		5	—	—	ns
SCLK to MISO [1] [2] [3]	t_{SCLK_MI}		22 + 1.5*$t_{HFPERCLK}$	—	33.5 + 2.5*$t_{HFPERCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

3.18.2 SPI Slave Timing, Voltage Scaling = VSCALE1

Table 4.40. SPI Slave Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1 2 3]	^{t}SCLK		^{6*t}HFPERCLK	—	—	ns
SCLK high time [1 2 3]	^{t}SCLK_HI		2.5*$t_{HFPERCLK}$	—	—	ns
SCLK low time [1 2 3]	^{t}SCLK_LO		2.5*$t_{HFPERCLK}$	—	—	ns
CS active to MISO [1 2]	^{t}CS_ACT_MI		30.5	—	57.5	ns
CS disable to MISO [1 2]	^{t}CS_DIS_MI		25	—	55	ns
MOSI setup time [1 2]	^{t}SU_MO		7.5	—	—	ns
MOSI hold time [1 2 3]	^{t}H_MO		8.5	—	—	ns
SCLK to MISO [1 2 3]	^{t}SCLK_MI		24.5 + $^{1.5*t}$HFPERCLK	—	45.5 + $^{2.5*t}$HFPERCLK	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

3.19 I2C Electrical Specifications

3.19.1 I2C Standard-mode (Sm)

CLHR set to 0 in the I2Cn_CTRL register.

Table 4.41. I2C Standard-mode (Sm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	^{f}SCL		0	—	100	kHz
SCL clock low time	^{t}LOW		4.7	—	—	µs
SCL clock high time	^{t}HIGH		4	—	—	µs
SDA set-up time	^{t}SU_DAT		250	—	—	ns
SDA hold time	^{t}HD_DAT		0	—	—	ns
Repeated START condition set-up time	^{t}SU_STA		4.7	—	—	µs
Repeated START condition hold time	^{t}HD_STA		4.0	—	—	µs
STOP condition set-up time	^{t}SU_STO		4.0	—	—	µs
Bus free time between a STOP and START condition	^{t}BUF		4.7	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

3.19.2 I2C Fast-mode (Fm)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.42. I2C Fast-mode (Fm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	^{f}SCL		0	—	400	kHz
SCL clock low time	^{t}LOW		1.3	—	—	µs
SCL clock high time	^{t}HIGH		0.6	—	—	µs
SDA set-up time	^{t}SU_DAT		100	—	—	ns
SDA hold time	^{t}HD_DAT		0	—	—	ns
Repeated START condition set-up time	^{t}SU_STA		0.6	—	—	µs
Repeated START condition hold time	^{t}HD_STA		0.6	—	—	µs
STOP condition set-up time	^{t}SU_STO		0.6	—	—	µs
Bus free time between a STOP and START condition	^{t}BUF		1.3	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

3.19.3 I2C Fast-mode Plus (Fm+)

CLHR set to 1 in the I2Cn_CTRL register.

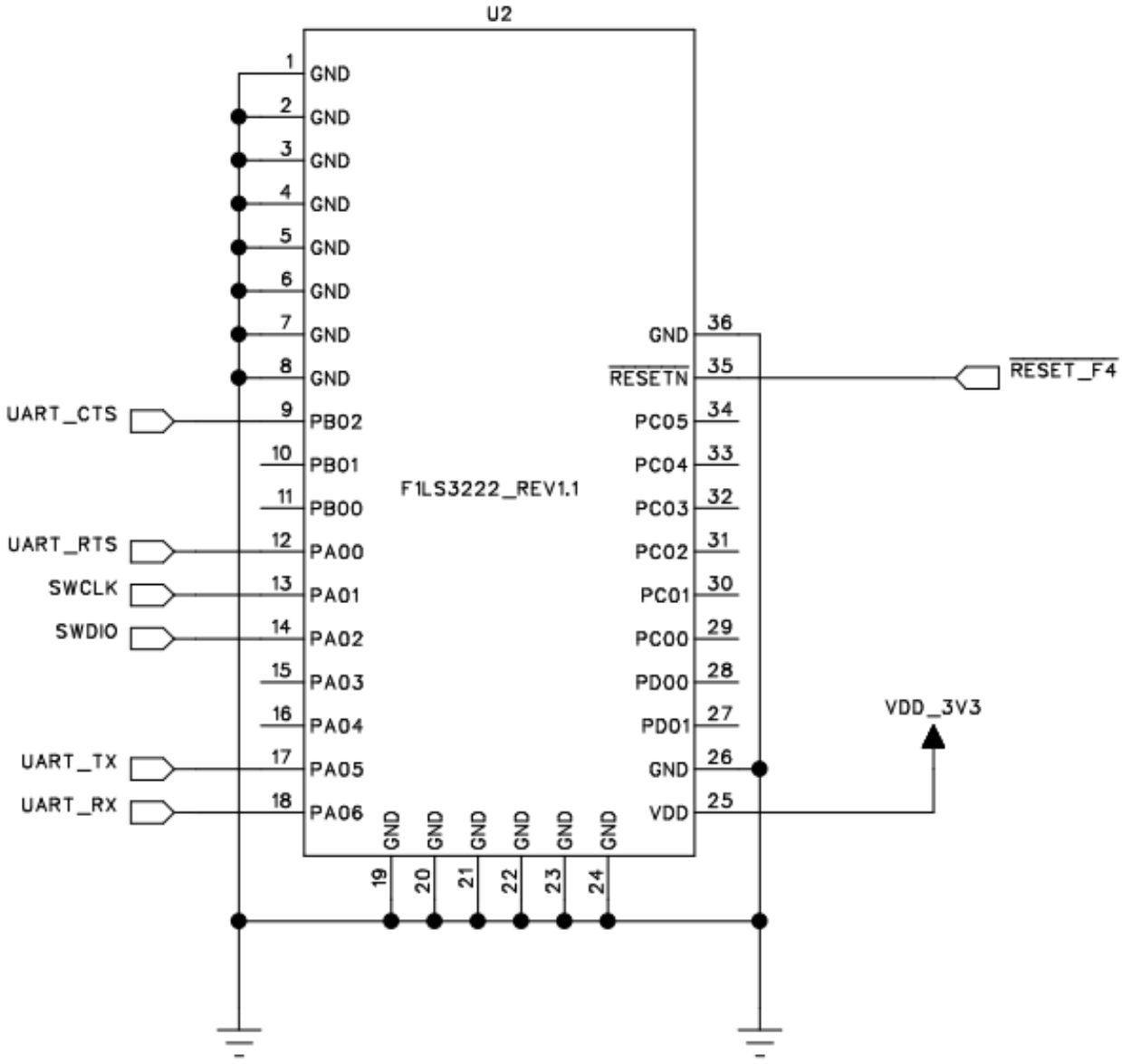
Table 4.43. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
Repeated START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:

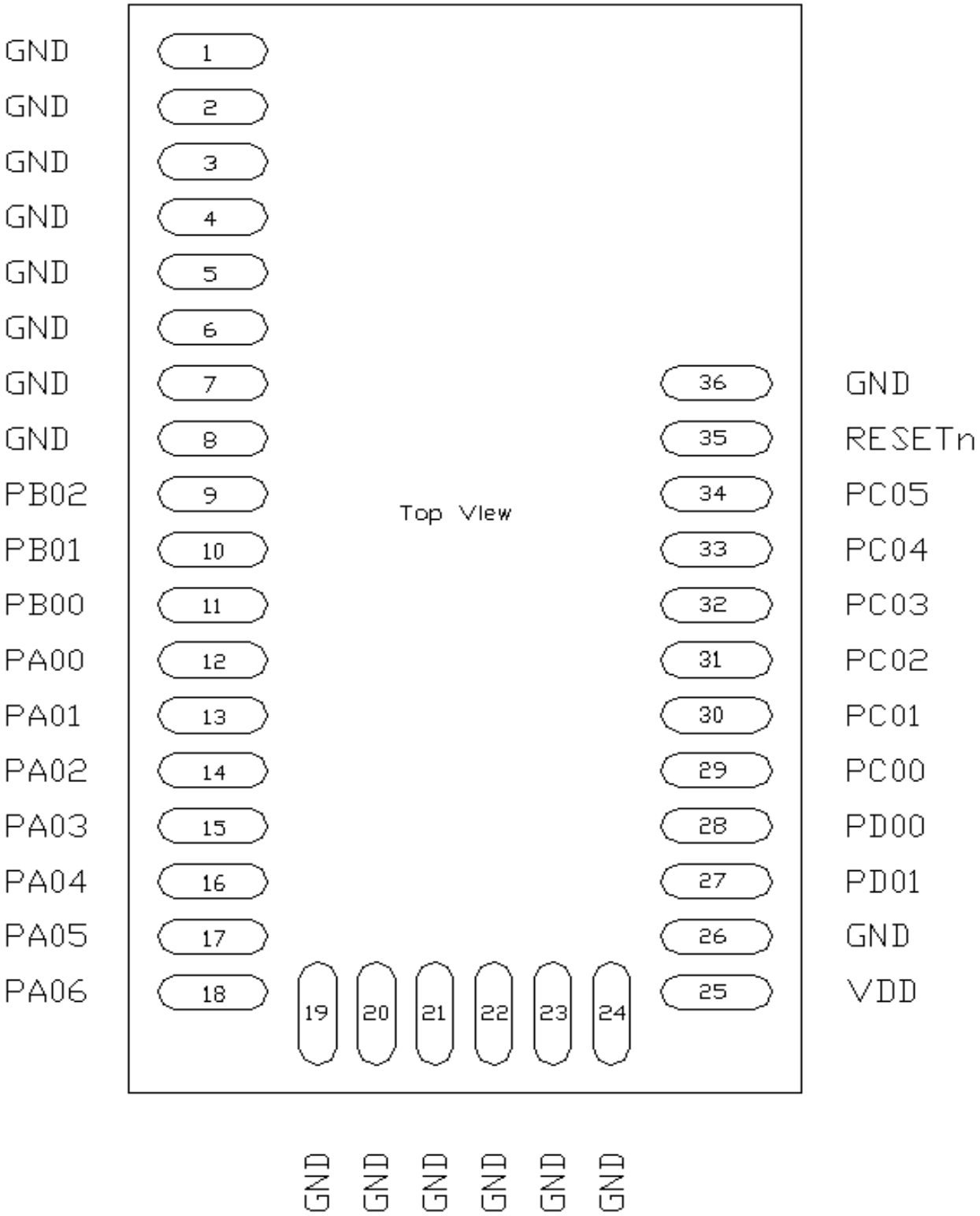
1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.Application Schematic



5. Pin Definitions

5.1 Device Pinout



5.2

Pin Name	Pin(S)	Description	Pin Name	Pin(S)	Description
GND	1	Ground	GND	19	Ground
GND	2	Ground	GND	20	Ground
GND	3	Ground	GND	21	Ground
GND	4	Ground	GND	22	Ground
GND	5	Ground	GND	23	Ground
GND	6	Ground	GND	24	Ground
GND	7	Ground	VDD	25	Power Supply
GND	8	Ground	GND	26	Ground
PB02	9	GPIO	PD01	27	NC
PB01	10	GPIO	PD00	28	NC
PB00	11	GPIO	PC00	29	GPIO
PA00	12	GPIO	PC01	30	GPIO
PA01	13	GPIO	PC02	31	GPIO
PA02	14	GPIO	PC03	32	GPIO
PA03	15	GPIO	PC04	33	GPIO
PA04	16	GPIO	PC05	34	GPIO
PA05	17	GPIO	RESETn	35	Reset Pin. The RESETn pin is internally pulled up to VDD
PA06	18	GPIO	GND	36	Ground

5.3 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows what functions are available on each device pin.

Table 6.4. GPIO Alternate Function Table

GPIO			Alternate Function		
PC00	GPIO.EM4WU6	GPIO.THMSW_EN	GPIO.THMSW_HALFSWITCH		
PC05	GPIO.EM4WU7				
PC07	GPIO.EM4WU8				
PB03	GPIO.EM4WU4				
PB01	GPIO.EM4WU3				
PB00	IADC0.VREFN				
PA00	IADC0.VREFP				
PA01	GPIO.SWCLK				
PA02	GPIO.SWDIO				
PA03	GPIO.SWV	GPIO.TDO	GPIO.TRACEDA-TA0		
PA04	GPIO.TDI	GPIO.TRACECLK			
PA05	GPIO.EM4WU0				
PD02	GPIO.EM4WU9				
PD01	LFXO.LFXTAL_I	LFXO.LF_EXTCLK			
PD00	LFXO.LFXTAL_O				

5.4 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are avali-able on each GPIO port. When a differential connection is being used Positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is avaliable on all pins. See the device Reference Manual for more details on the ABUS and analog peripherals.

Table 6.5. ABUS Routing Table

Peripheral	Signal		PA		PB		PC		PD	
		EVEN		ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
IADC0	ana_neg	Yes		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ana_pos	Yes		Yes	Yes	Yes	Yes	Yes	Yes	Yes

5.5 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are avalia-ble on each GPIO port.

Table 6.6. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUART0.CTS	Available	Available	Available	Available
EUART0.RTS	Available	Available	Available	Available
EUART0.RX	Available	Available	Available	Available
EUART0.TX	Available	Available	Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		

Peripheral.Resource	PA	PB	PC	PD
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PDM.CLK	Available	Available	Available	Available
PDM.DAT0	Available	Available	Available	Available
PDM.DAT1	Available	Available	Available	Available
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		

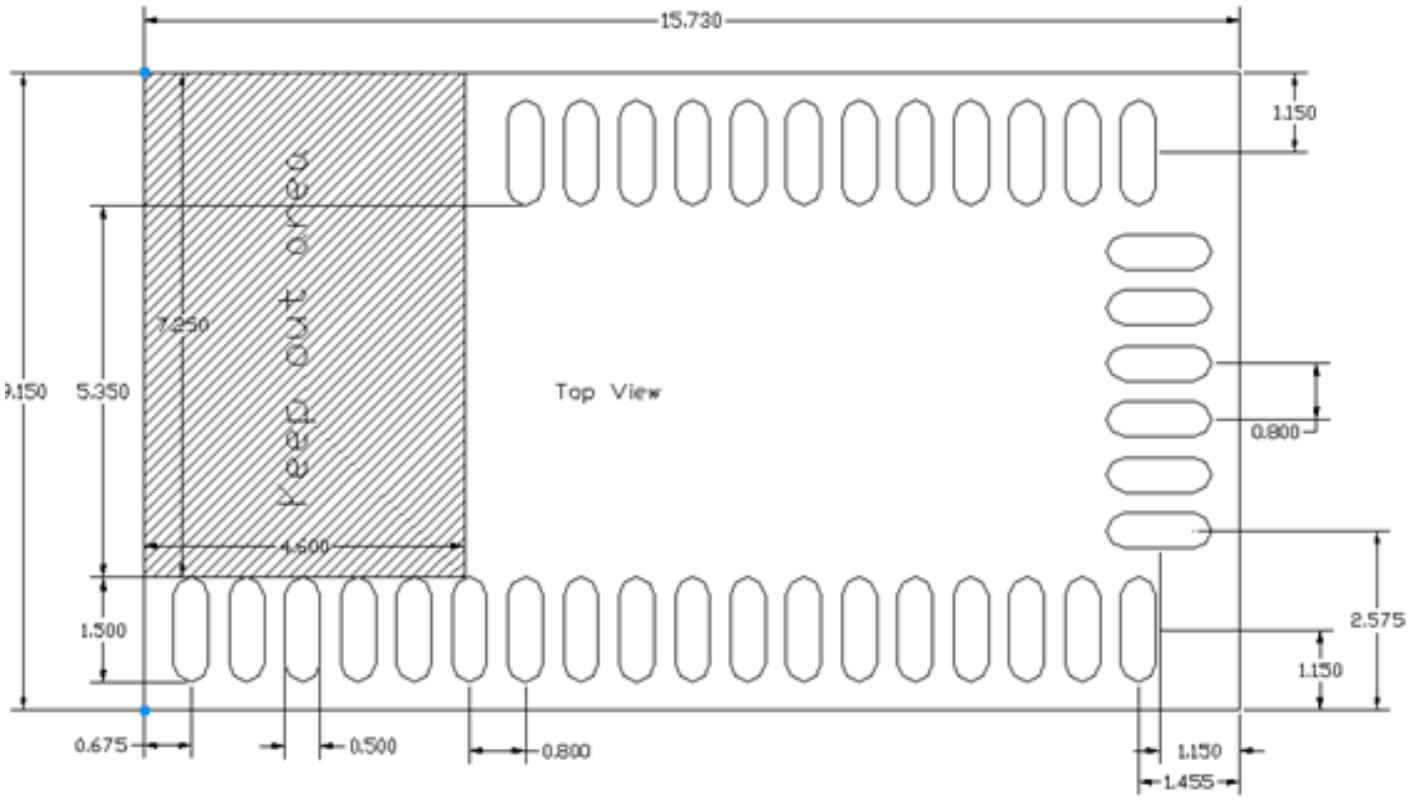
Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available
USART1.CLK	Available	Available		
USART1.CS	Available	Available		
USART1.CTS	Available	Available		
USART1.RTS	Available	Available		
USART1.RX	Available	Available		
USART1.TX	Available	Available		

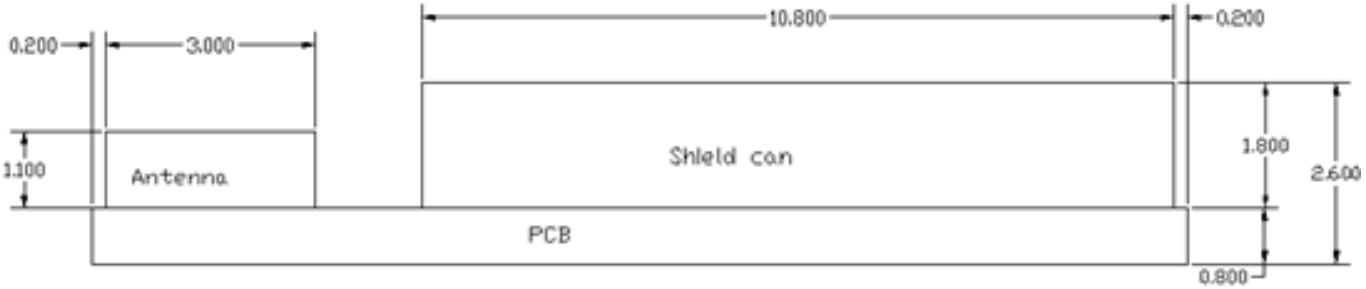
6.Module Package Specifications

6.1 dimensions

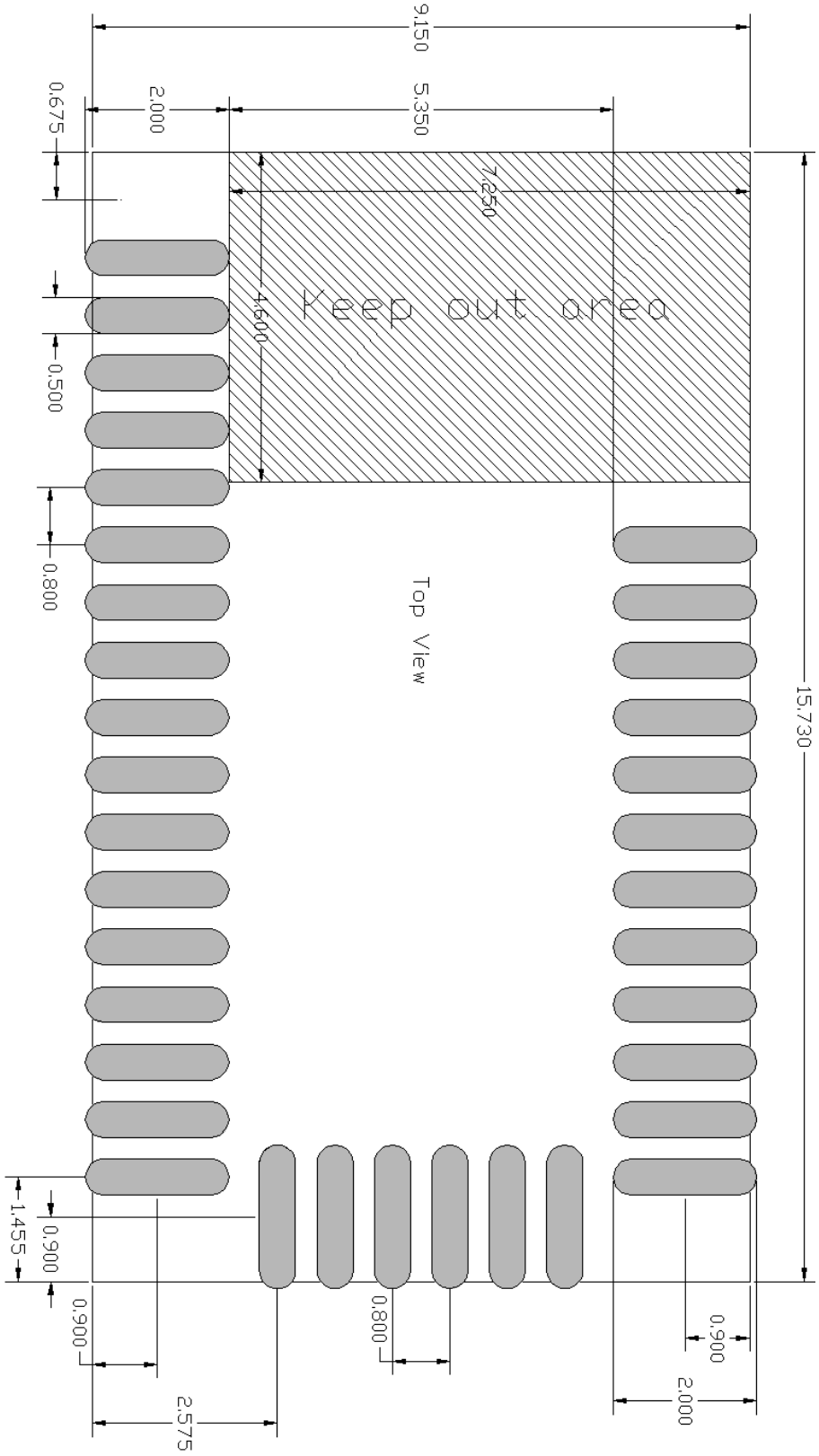
F1LS3222 Rev1.0 DIMENSION

1. TOP VIEW(Unit : mm)





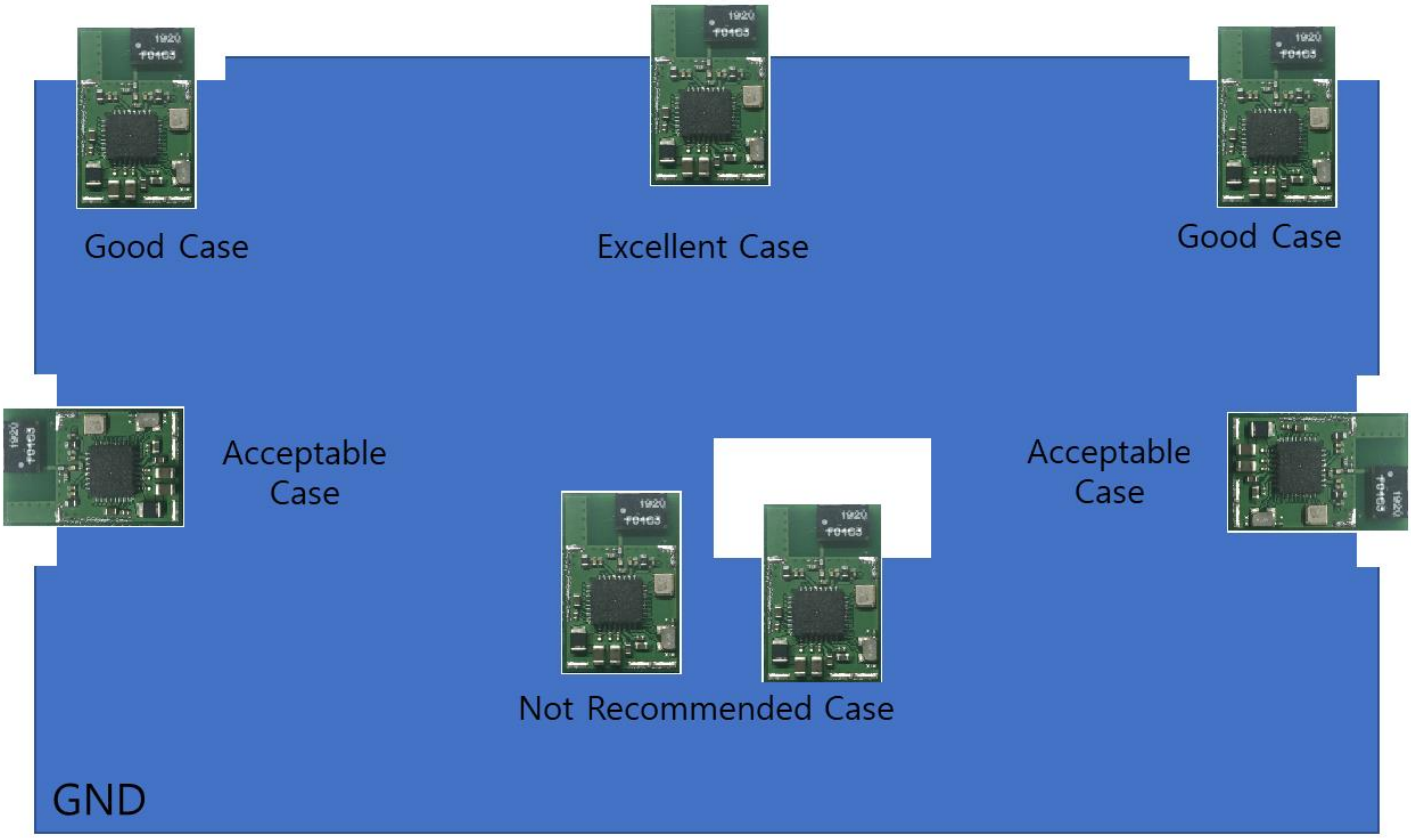
6.2 F1LS3222 PCB Layout



6.3 F1LS3222 Placement rule

On the main PCB, the areas under the antenna should not contain any top, inner layer, or bottom copper as shown in Figure. For the best range performance, keep all external metal away from the chip antenna at least 45 mm. In all cases, the performance of the antenna can vary depending on GND.

F1LS3222 EVB



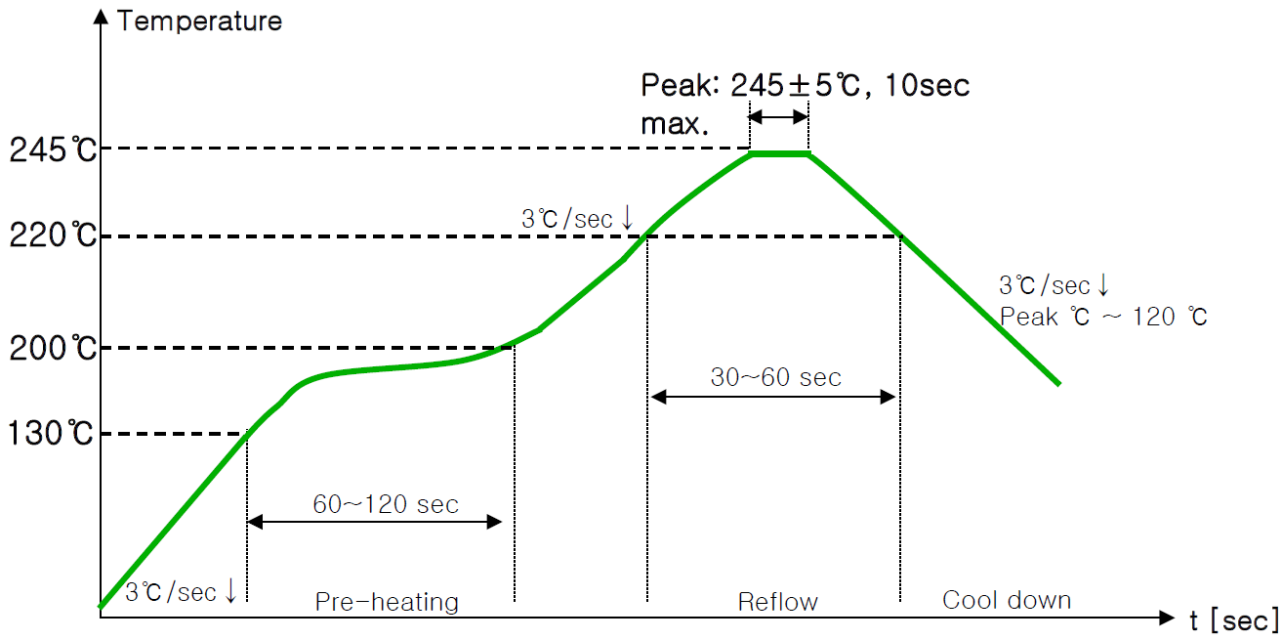
7. Soldering Recommendations

7.1 Soldering Recommendations

This section describes the soldering recommendations regarding F1LS3222 Module.
F1LS3222 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven, and particular type of solder paste used.

• Refer to technical documentations of particular solder paste for profile configurations.
• Avoid usining more than two reflow cycles.
• Aperture size of the stencil should be 1:1 with the pad size.
• A no-clean, type-3 solder paste is recommended.
• For further recommendation, please refer to the JEDEC/IPC J-STD-020, IPC-SM-782 and IPC 7351 guidelines.

7.2 Reflow Temperature Profile



- Please use the reflow within 2 times.

FCC MODULAR APPROVAL INFORMATION EXAMPLES for Manual

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference.

(2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION: Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

OEM INTEGRATION INSTRUCTIONS:

This device is intended only for OEM integrators under the following conditions:

The module must be installed in the host equipment such that 20 cm is maintained between the antenna and users, and the transmitter module may not be co-located with any other transmitter or antenna. The module shall be only used with the internal on-board antenna that has been originally tested and certified with this module. External antennas are not supported. As long as these 3 conditions above are met, further transmitter test will not be required.

However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). The end-product may need Verification testing, Declaration of Conformity testing, a Permissive Class II Change or new Certification. Please involve a FCC certification specialist in order to determine what will be exactly applicable for the end-product.

Validity of using the module certification:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization. In such cases, please involve a FCC certification specialist in order to determine if a Permissive Class II Change or new Certification is required.

Upgrade Firmware:

The software provided for firmware upgrade will not be capable to affect any RF parameters as certified for the FCC for this module, in order to prevent compliance issues.

End product labeling:

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains FCC ID: 2APDI-BCM-DA100-AS" .

Information that must be placed in the end user manual:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.