3.2 CIRCUIT DESCRIPTION

The transmitter consists of three circuit boards, two power supply modules and the associated wiring and connectors. Both of the power supplies are fully approved bought in modules and won't be discussed electrically except for the connections to the other boards where appropriate.

The three PCB's previously mentioned are the combo board, the power amplifier board and the control / LCD board. The wiring and connection between the boards can be seen in the internal case diagram.

The combo board contains
1. Audio limiter with pre-emphasis capability
2. High spec over-sampled digital stereo encoder
3. High spec low distortion PLL exciter
4. Power supply circuitry to supply various voltages to the different sections
5. A logic / control section to interface to external equipment
6. Control connections to the LCD control board

The Power amplifier board contains
1. A 2 stage 150/300 Watt FM amplifier
2. Low pass harmonic filter
3. VSWR bridge / coupler and power sniff circuitry
4. Temperature sensing circuitry

The Control / LCD board contains
1. A 122x32 LCD graphics display
2. Three front panel buttons for LCD control
3. Power control adjustment and transmitter fault / protection circuitry
4. An 8 bit microcontroller to control all the LCD functions, metering and alarm monitoring

We will describe the electrical workings of the transmitter from the audio input through to the RF output and will attempt to explain how the three boards tie together and form the complete unit.

We will start at the audio input sockets on the back panel which are part of the combo board.

3.21 COMBO BOARD

The description of the circuitry describes the right channel path where stereo sections are mentioned. The component for the left channel is bracketed next to the right channel component.

Audio limiter description

Left and right audio signals are applied to balanced input XLR sockets on the back panel. The balanced audio signals are fed to IC1(IC4) which are configured as differential amplifiers to convert the balanced inputs to unbalanced for the rest of the limiters circuitry. The output from the differential op-amps feed a pre-emphasis filter which can be switched in or out of circuit via the on board jumpers J2(J3). The audio is then fed from the pre-emphasis filters to one half of dual op-amps IC2(IC3) where input gain can be adjusted through the rear panel input gain control VR1(VR2) which forms the feedback path for the op-amp. The audio is then fed into the other half of IC2(IC3). These dual op-amps are also the limiter gain control and output for the limiter.
The output of the input gain op-amps also feed the full wave rectifier circuitry which provides a DC representation of the audio signal. This DC voltage is applied to a time constant circuit which provides the attack and release parameters for the limiter. The time constant capacitors C54 and C55 together with R58 and R59 provide a programme dependent interactive time constant for clear punchy sound at all levels of limiting. After passing through the time constant filter the DC signal is buffered by IC7 and then fed to IC6 which drives PNP transistors T1(T2) which controls the current passing through the gain control element, transconductance amplifier IC5.
Transconductance amplifier IC5 is configured as a variable resistor which is placed in the feedback path of the gain control op-amps. IC5 varys its resistance in accordance with the level of audio drive so that the output of the gain control op-amps is fixed at 0dB. LED1(LED2) provide clipping of any overshoots that get through the limiter. This clipper can be switched in and out of circuit by jumper J6(J7). This provides significantly more loudness than can be obtained by making the attack time quicker to catch the overshoots. The amount of clipping can be controlled by J4(J5). These provide more drive to the gain control op-amps by putting resistor R53(R69) in parallel

with R47(R68) . This has the effect of a more “commercial loud sound” when in loud mode compared to a more true to the original sound when in clarity mode due to less clipping taking place. VR3(VR4) is connected across the inputs of the transconductance amplifier and provide offset adjustment to null any distortions introduced by offsets inherent in the op-amps

Stereo encoder description

The stereo encoder section is based around a high speed switch which is used to generate the multiplex at 38 kHz. The switch is controlled by microcontroller IC13 which supplies the timing signals to the switch at 304 kHz. The high speed enables an over-sampled 38KHz subcarrier to be generated that is rock steady and spectrally clean. As the signal is generated digitally no adjustments or setups are required for the encoder. The only adjustments on the encoder section are the stereo/mono control and the level of the stereo subcarrier. The 19KHz pilot tone is also generated by the microcontroller and because of this the stereo separation is excellent due to the perfect timing between the pilot and the subcarrier. The 19 kHz pilot is also generated by over-sampling techniques to produce a very low distortion pilot tone.
The audio path through the encoder starts at 15 kHz brickwall filter FIL1(FIL2). These provide over 40 dB of protection by 17 kHz, 50 dB by 20 kHz as well as a notch at 19 kHz to protect the pilot signal even further. The output from the filters are buffered by op-amp IC10(IC11). These buffer op-amps can also be used as clippers, which can be used to remove any overshoots introduced by ringing in the 15 kHz filters. The buffer op-amps drive into the analogue switches. The switches are controlled by the microcontroller IC17 and the output from the switches feed into three resistors R100,101,102 to provide a D/A type function producing the multiplex signal. The resistors are carefully chosen to provide sine weighting for the reconstruction, which keeps the lower order harmonic content down to almost zero. These three resistors are combined in virtual earth mixer op-amp IC14. The stereo pilot tone emerges from the microcontroller as a 4 bit word which has sine weighting applied to it by resistors R93 to R98. At this point, apart from 19 kHz, the pilot has no significant energy below 304 kHz. The pilot is fed through VR6 for adjustment of the pilot level before being combined with the subcarrier at the virtual earth mixer op-amp IC14. The complete stereo multiplex signal emerges from IC14 and is fed into a low-pass filter formed by L1,L2 and C78 to C84. This filter removes any high frequency products due to the sample rate. The filter is buffered by output op-amp IC15 which also provides a fixed output level of +6dBu, which is fed to the multiplex output BNC socket on the back panel, as well as to one side of the loopthrough jumper J1.

Exciter description

The frequency determining elements are inductor L3 and varicap diode VD1 together with capacitors C20 - C23. These components, together with transistors T4 and T5, form a cascade oscillator whose output is then buffered by RF transistor T6. The RF output from T6 is impedance matched to the base of P.A. transistor T7 by RFT1, a 4 to 1 matching transformer. The one watt power output from P.A. transistor T7 is impedance matched by coils L4 and L5 and associated capacitors C30-34 to the 50 ohm output socket CON7. These components also provide harmonic filtering. A coaxial cable carries the RF output from this socket to the RF input connector on the main power amplifier PCB.

The PLL circuit is primarily IC18 which is a serially programmable PLL chip. The microcontroller IC17 reads the dial switches at power up and outputs a serial code to the PLL chip in a format that determines the output frequency that the PLL will lock the transmitter to. If the microcontroller IC17 detects that the switches are set to 4440 then the microcontroller IC17 will talk to the microcontroller on the control / LCD board to request the LCD display control system stored frequency. The PLL chip delivers raw control pulses to the loop filter built around op-amp IC20. The loop filter is a low-pass filter that takes the raw rectangular differential outputs from the PLL chip and creates a DC voltage to apply to the frequency determining component, varicap diode VD1. The main time constant in the loop filter is formed by resistor R6 driving C8 and R5 driving C9. The high resistance of R5 and R6 allows slow charging of C9 and C6 from the PLL chip. The DC voltage derived from the output of the op-amp will be slow to change in response to the raw PLL pulses due to the slow charging of those capacitors. This slow DC voltage change is converted to slow frequency change by the varicap diode. IC19 is an analogue switch that shorts out the two high resistance resistors in the loop filter to allow faster charging of C9 and C6, and so, a faster change of the output DC voltage from the filter. This faster changing voltage can allow the transmitter to get on frequency faster. When the transmitter is on frequency the analogue switch stops shorting out the high resistance resistors and the slow loop takes control, which greatly improves the audio response of the transmitter. The microcontroller IC17 determines when to switch the analog switch in and out by reading the lock detect signals from the PLL chip. The microcontroller can also use this information to switch off transistor T6 with open collector configured T11 which mutes the RF output when the transmitter is out of lock. LED5 provides visual indi-

cation of the PLL locked condition. The front panel control system will also display the locked condition when in the frequency display screen.

Audio is fed into the modulation input of the exciter from external multiplex input connector CON2 which is a BNC type or from the internal stereo encoder section by having jumper J1 set to loopthrough. The modulation level can be adjusted from the back panel by the adjustment of variable resistor VR5 which is in the feedback loop of op-amp IC18. The output of the op-amp feeds the modulation element, varicap diode VD1, via potential divider R31 and R18.

CON8 provides an interface to the control / LCD board. This ribbon cable interface provides connections for the alarm signals to the back panel D-type from the microcontroller on the LCD board together with connections for the modulation, the limiter gain reduction level and a serial interface which provides frequency and status information between the PLL microcontroller on the combo board and the main system microcontroller on the LCD board.

3.22 LCD CONTROL BOARD

The LCD control board is the heart of the transmitter. The board contains an eight bit microcontroller, LCD display, a voltage regulator and a dual op-amp together with a few passive components.

CON1 provides a 10 way interface to the power amplifier board and its sensors. Some of the connections of CON1 are routed around to the power supply modules. CON2 provides a 16 way interface to the combo board providing power to the combo board as well as routing signals to the back panel D-type sockets for alarms/RS232 and returning modulation and limiter gain reduction signals to the main microcontroller.

The voltage regulator REG1 and decoupling capacitors C1 and C2 takes the 18 volt auxillary supply from CON1 and regulate it down to 5 volts for the microcontroller and LCD circuitry. The microcontroller is a 40 pin 8 bit type running at 8 MHz. The microcontroller has several ports that have various functions and connect to external components.

PORTA (6 bits) is primarily used for the analogue voltage inputs. Bit 0 is the limiter gain reduction, Bit 1 the modulation, Bit 2 the AUX volts and Bit 3 the Fwd RF power. Bit 4 is not used and bit 5 of PORTA has a control connection to the LCD display.

PORTB (8 bits) has a few different functions. Bits 7,6 and 3 of the port are the alarm signal outputs and are routed off via CON2 to the D-type on the back of the combo board. Bit's 5,4 and 2 are connected to the front panel buttons to allow navigation of the LCD functions. Bits 1 and 0 provide a 2 wire interface to the PLL microcontroller on the combo board.

PORTC (8 bits) bits 0 and 1 are used to write information to the LCD display. Bit 2 is the pulse width modulator output (PWM) and connects into unity gain DC amplifier op-amp IC2A. The voltage generated by the PWM is set by the software in the microcontroller. This PWM level is then fed through potentiometer VR2 and smoothed by C13 before being buffered by the aforementioned op-amp. PORTC bits 3-5 are not used. Bit’s 6 and 7 of PORTC are used by the UART inside the microcontroller. These pins are RXD and TXD for the RS232 interface. They are routed via CON2 to the back panel D-type.

PORTD's 8 bit's are interfaced to the 8 bit data bus of the LCD display. The data byte on PORTD can be latched into the LCD display by the LCD control bits on PORTC.

PORTE (3 bits) has the remaining A/D inputs. Bit 0 is the PA volts, Bit 1 is the Rev RF power and bit 2 is for the PA temperature.

The microcontrollers software reads all the analogue voltages, converts and displays them where neccessary and outputs alarm signals in the event of a transmitter error. There are various passive components associated with IC1. Each A/D port has input current limiting resistors R1-11 and decoupling capacitors C5-11. X1, C3 and C4 provide the 8 MHz signal for the clock of the microcontroller. R12 and R13 provide pull downs for correct operation of the internal processor communications channel. C12 provides supply decoupling for the microcontroller and VR1 sets the contrast of the LCD display.

IC2 is a dual op-amp whose purpose is to control the output power of the transmitter. Side A of the op-amp is configured as a unity gain buffer for the PWM and was described previously. VR2 provides an adjustable DC level to side B of the op-amp. Side B is configured as a DC amplifier with the gain set by R17, R18, R19, R20 and R25. The larger the DC signal provided by side A and the larger the DC signal at the output of Side B. This DC signal is used to turn down the output of the Power amplifiers power supply and with it the RF power output level.

LED3 and R20 provide a connection from the reverse RF power sensor into the input the non inverting input of side B of the op-amp. LED3 only allows DC through above a certain level. Any DC above this level will increase the output voltage from the op-amp and the RF power level will decrease. This forms the VSWR protection for the transmitter. LED1 and LED2 also provide the same function but with the DC level this time being supplied by the temperature sensor on the PA board. Too high a temperature will cause the DC level to exceed the turn on point of the two diodes and voltage will once again turn up the op-amps voltage and turn down the RF power level which should lower the temperature of the transmitter. The output from side B is fed to the switched mode power supply of the power amplifier via R21 and CON1. R22 and C15 provide supply decoupling for the op-amp. C14,15,16,17,18 provide further decoupling and feedback for the power control feedback loop formed around side B of the op-amp.

3.23 POWER AMPLIFIER BOARD

PSU interface

The voltage from the PSU arrives at input of REG1 thorugh 36-pin EDGE connector. REG1 is a switching regulator. The 52kHz output signal from REG1 is half rectified by D1 and smoothed out through L1, C2 and C3. The resulting DC voltage is used to drive the transmitter fans. R1 which is in the feedback loop of REG1, adjusts the maximum voltage to accommodate different fan types. Also part of the feedback loop is a temperature sensor (placed on the bus bar board), making the amount of airflow in the transmitter temperature dependent. LED D2 indicates there is an output voltage present.

Bus bar board

A bus bar board accommodates the mentioned temperature sensor R1 which is extrudes into the main heatsink, provides further voltage smoothing for fans and routes the supply voltages from CON1 to appropriate sections of the power amplifier.

Controller board

The controller board controls the power output of an output amplifier based on forward VSWR detection, reverse VSWR detection, forward power signal form the LCD board and temperature. All op-amps are supplied with +18V from the AUX power supply line, buffered by the capacitors C1, C2, C8 and C15.

Detected reverse VSWR (sniffed of the power amplifier's main RF output line) arrives through CON2 and input filter C5-R7 to the IC2A. The gain of the op-amp is set by R22 and R23. Amplified signal is smoothed by C13 and C14 and fed to the OR-ing circuit on the input of IC1B.

Detected forward VSWR (sniffed of the power amplifier's main RF output line) arrives through CON1 and input filter C7-R24 to the IC2B. The gain of the op-amp is set by R9, R10 and VR2. Amplified signal is smoothed by C12 and fed to the OR-ing circuit on the input of IC1B.

Forward power control signal comes from the micro controller on the LCD board to the inverting input of IC1A through R4 and C10. A voltage divider R12 and R13 sets the voltage reference to the non-inverting input to be half of the AUX power supply rail. The gain of the op-amp is set by R4 and R5. Output signal is fed directly to the IC1B.

IC1B includes an OR-ing circuit on the input and a summer (R32-R34) to combine the reverse VSWR, forward VSWR and PA control signals together. Output of IC1B is then a final control signal that controls the output of the power amplifier by controlling it's power supply voltage. R27 and VR3 set the voltage reference to the inverting input of IC1B.

A temperature sensor circuit is located close to the main RF transistors. This temperature sensor is mounted into the heatsink and consists of the sensor itself which is located under the board and an op-amp circuit for level adjustment. The op-amp IC3A provides a suitable voltage reference while IC3B and associated components convert the output signal from the temperature sensor to a level more suitable for the micro controller and protection circuitry on the LCD board.

15W driver board

The RF signal from the exciter section of the combo board arrives at the MCX RF input connector CON1 via a coaxial cable. From here the 50 ohm input impedance is matched to the gate of the FET transistor T1 by the impedance matching network formed by C8, C3, L2, C9 and L3. R3, D2, R9, R5 and VR2 provide bias control to the gate of T1 from the output of REG1 which is a switching regulator. PLL signal coming through R6 from the exciter section, can pull the T1 bias voltage low, effectively reducing the power output of T1.

R4, FB1, L5 and C5 provide supply voltage to T1's drain as well as providing some impedance matching to the output of T1. Further impedance matching from T1's drain is composed of L4, C6 and C10.
Switching regulator REG1 generates 50 kHz signal from the +50V main power supply line, which is rectified by commutating diode D1, low pass filtered by L6, L1, R1, R2, C4 and decoupled by capacitors C1 and C4 to produce +25V DC voltage for the T1.

Double pallet

The RF signal from the 15W driver board arrives at the input connector CON1. From here the 50 ohm input impedance is distributed to two branches via a bridge consisting of two quarter-length 70 Ohm lines. In each branch a RTF3 (RTF4) impedance matching balun provides an unbalanced to balanced connection to the two gates of gemini packaged FET transistor T1 (T2). Transistors are biased through R9 (R17), VR1 (VR2), R1, R2, R5 and R6. In case of excessive VSWR, a sniffed signal from the output combiner coming through VR3 will turn the diodes D5 and D6 on, and negatively bias transistors T1 and T2 off.

The drain outputs of T1 (T2) are connected to another balun transformer RFT1 (RTF2) which provides impedance step up as well as proving a DC feed to the transistors drains via a center tapped winding. The DC power applied to the center of balun comes from the main adjustable power supply module which can control the RF power output by having it's output voltage adjusted. C6-7 (C12-13), FB1 (FB2), R10-11 (R14-15), and C7 (C12) provide filtering and RF decoupling to the power feed into the center tap of balun RFT1 (RTF2).

Output combiner

Two output signals from RTF1 and RTF2 are combined together via a bridge consisting of two quarter-length 70 Ohm lines. On each line there is a sniffed signal that drives LEDs D5 and D7 in case of excessive VSWR and/or bridge unbalance. Another RF sense circuit consisting of R1, R2, C1, C2, D1 and R3 produces a negative voltage in the event of excessive VSWR on the combined output which shuts transistors T1 and T2 on the double pallet off.

The output of the bridge is fed into a low pass output filter. These components reduce the level of any harmonic products generated by the power amplifier. The output of the low pass filter is sniffed by VSWR sensors R4, R5, C3, D2, C4 and R6, R7, C5, D3, C6 which generate forward and reverse RF power measurements for metering and for VSWR fault protection and alarms.