AzureWave Technologies, Inc.

AW-XM646x Series

IEEE 802.11 a/b/g/n/ac/ax Wireless LAN 1T1R and BLE/802.15.4 Solution Family 12 x 12 LGA Module

Datasheet

Rev. B

DF

For Standard

Features

WLAN

- 1x1 dual-band 2.4 GHz/5 GHz Wi-Fi 6 radio
- Integrated Wi-Fi PA, LNA, and T/R switch, up to +23 dBm TX power
- 20 MHz channel operation
- Wi-Fi 6 Target Wake Time (TWT) support
- Wi-Fi 6 Extended Range (ER) and Dual Carrier Modulation (DCM)
- Low-power Wi-Fi idle, standby, and sleep modes
- WPA2/WPA3 security
- Support for Matter over Wi-Fi

Bluetooth

- Bluetooth Low Energy 5.4
- Bluetooth LE 1 Mbps and 2 Mbps high-speed uncoded modes, and Long Range operation (125 kbps and 500 kbps coded data rates)
- IEEE 802.15.4-2015 compliant MAC
- Support for Matter over Thread

802.15.4

- IEEE 802.15.4-2015 compliant supporting Thread in 2.4 GHz band
- Shared transmitter and antenna pin with Bluetooth
- Simultaneous receive with Wi-Fi and Bluetooth
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers

Revision History

Document NO: R2-2646-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2024/12/12	DCN033008	Initial version	Vigil Tsai	N.C. Chen
B	2025/03/18	DCN033820	● Update RF specification ● Update Specifications Table ● Update packing information	Roger Liu	N.C. Chen

Table of Contents

1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the IEEE 802.11a/b/g/n/ac/ax 1x1 dual band WLAN, BLE/802.15.4, module – **AW-XM646.** With full-feature Wi-Fi subsystem integrated into a module, **AW-XM646** provides the best and most convenient SMT process. The module is targeted to smart entertainment, gateways, hubs, bridges, smart home, industrial, point of sale (POS) terminal, smart appliances which need convenient SMT process.

By using **AW-XM646**, the customers can easily integrate the Wi-Fi, BLE, by a combo module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11 a/b/g/n/ac/ax standard, the **AW-XM646** uses **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using **AW-XM646**.

The **AW-XM646** supports standard interface **USB 2.0 / SDIO3.0 for WLAN**, **USB 2.0 / UART for BLE, SPI for 802.15.4**. **AW-XM646** is suitable for multiple mobile processors for different applications. With the combo functions and the good performance, the **AW-XM646** is the best solution for the consumer electronics and smart applications.

1.2 Block Diagram

TBD

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi 6 with BLE/802.15.4 Combo Solution
Major Chipset	NXP IW610B/CF/G WLCSP (114pins)
Host Interface	WiFi + BLE + 802.15.4 ● SDIO + UART + SPI (Optional) ● USB + USB + SPI (Optional)
Dimension	12 mm X 12 mm x 2 mm(Max)
Form Factor	LGA module, 48 pins
Antenna	ANT1(Main)：WiFi/BLE/802.15.4 → TX/RX
Weight	TBD

AW-XM646x variants

Product name	Features
AW-XM646B-USB	1x1 Single -band (2.4 GHz) Wi-Fi 6 + BLE
AW-XM646B-SUR	1x1 Single -band (2.4 GHz) Wi-Fi 6 + BLE
AW-XM646C-USB	1x1 Single -band (2.4 GHz) Wi-Fi 6 + BLE/802.15.4
AW-XM646C-SUR	1x1 Single -band (2.4 GHz) Wi-Fi 6 + BLE/802.15.4
AW-XM646F-USB	1x1 Dual-band (2.4 / 5 GHz) Wi-Fi 6 + BLE
AW-XM646F-SUR	1x1 Dual-band (2.4 / 5 GHz) Wi-Fi 6 + BLE
AW-XM646G-USB	1x1 Dual-band (2.4 / 5 GHz) Wi-Fi 6 + BLE/802.15.4
AW-XM646G-SUR	1x1 Dual-band (2.4 / 5 GHz) Wi-Fi 6 + BLE/802.15.4

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi 6
Frequency Range	2.4 GHz ISM Bands 2.412-2.462 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for US/Canada and Europe 5.725-5.895 GHz (FCC UNII-high band) for US/Canada
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM, 256-QAM, OFDMA

<table>
<tr><td>Number of Channels</td><td>2.4GHz:
■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11
■ China, Australia, Most European Countries - 1 ~ 13
■ Japan, 1 ~ 13

5GHz:
■ USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165
■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140
■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165</td></tr>
<tr><td>Output Power
(Board Level Limit)*</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps)
@EVM<35%</td><td>17.5</td><td>19</td><td>20.5</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)
@EVM≦-25 dB</td><td>15.5</td><td>17.</td><td>18.5</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-27 dB</td><td>14.5</td><td>16</td><td>17.5</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS9)
@EVM≦-32 dB</td><td>13.5</td><td>15</td><td>16.5</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps)
@EVM≦-25 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-27 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8)
@EVM≦-30 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS9)
@EVM≦-32 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>Receiver Sensitivity</td><td>
2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td>-</td><td>-89</td><td>-86</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>-</td><td>-75</td><td>-72</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-72</td><td>-69</td><td>dBm</td></tr>
<tr><td>11ax (HE20 MCS9)</td><td>-</td><td>-65</td><td>-62</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td>-</td><td>-74</td><td>-71</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-71</td><td>-68</td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8)</td><td>-</td><td>-67</td><td>-64</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS9)</td><td>-</td><td>-64</td><td>-61</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Data Rate</td><td>WLAN:
802.11b : 1, 2, 5.5, 11Mbps
802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n : Maximum data rates up to 72 Mbps
802.11ac: Maximum data rates up to 86 Mbps
802.11ax: Maximum data rates up to 115 Mbps</td></tr>
<tr><td>Security</td><td>■ WiFi: WPA3, WPA2, WPA2 and WPA mixed mode, WEP
■ BT: AES</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth LE 5.4 certified</td></tr>
<tr><td>Frequency Range</td><td>2402MHz~2480MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>Low Energy 1M</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity</td><td>BT Sensitivity (PER<30.8%)
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>Low Energy 1M</td><td></td><td>-96</td><td>-93</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

1.3.4 802.15.4

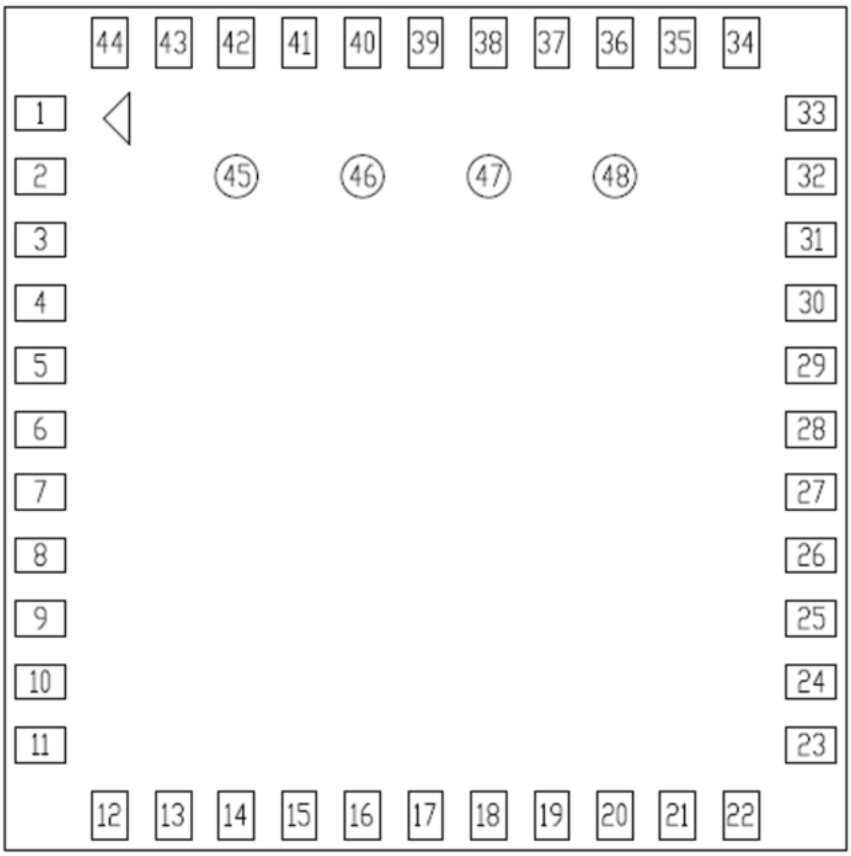
Features	Description
Thread Standard	IEEE 802.15.4-2015 compliant supporting Matter over Thread in 2.4 GHz band
Frequency Range	2400MHz~2480MHz
Modulation	O-QPSK
Output Power	<table><tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr><tr><td>Thread</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr></table>

1.3.5 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V +-5%
Operating Temperature	-40 ºC to +85 ºC
Operating Humidity	Less than 85% R.H.
Storage Temperature	-40 ºC to +85 ºC
Storage Humidity	Less than 60% R.H.

2. Pin Definition

2.1 Pin Map



AW-XM646 Pin Map (top view)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND1	Ground	---	---
2	RF_ANT	RF pin out	---	I/O
3	GND	Ground	---	---
4	SPI_TXD	SPI receive output signal. GPIO[6]	VDDIO	I/O
5	SPI_RXD	SPI receive input signal. GPIO[7]. PCM mode PCM sync signal	VDDIO	I/O
6	HOST_WAKE_ BT	GPIO Mode : GPIO[17]. Host wake BLE/802.15.4 device	VDDIO	I/O
7	BT_WAKE_Host	JTAG_TDO mode test data output signal. GPIO[5]. BLE/802.15.4 device wake Host	VDDIO	O
8	SPI_FRM	SPI_FRM - SPI frame signal. GPIO[8]	VDDIO	I/O
9	VBAT	3.3V power voltage source input	3.3V	P
10	JTAG_TMS	JTAG test mode select input signal. GPIO[3]	VDDIO	I/O
11	SPI_CLK	SPI_CLK - SPI clock signal. GPIO[9]	VDDIO	I/O
12	PDn	Full Power-down (input) (active low) 0 = full power-down mode 1 = normal mode (Has pull high 51k resistor to 3.3V internally)	3.3V	I
13	WL_WAKE_Host	JTAG_TDI Mode test data input signal. GPIO[4]. Wake up mode WIFI wake host output signal	VDDIO	I/O
14	SDIO_DATA2	SDIO Data line Bit[2]	VDDIO	I/O
15	SDIO_DATA3	SDIO Data line Bit[3]	VDDIO	I/O
16	SDIO_CMD	SDIO Command	VDDIO	I/O
17	SDIO_CLK	SDIO Clock input	VDDIO	I
18	SDIO_DATA0	SDIO Data line Bit[0]	VDDIO	I/O
19	SDIO_DATA1	SDIO Data line Bit[1]	VDDIO	I/O
20	GND	Ground	---	---
21	DCDC_1V8_OUT	Internal DC-DC output (Need external 1uH power inductor and 22μF capacitance)	1.8V	P
22	VDDIO	1.8V/3.3V Digital I/O Power Supply	1.8V/3.3V	P
23	DCDC_1V8_IN	1.8V power voltage source input	1.8V	P
24	NC	Floating Pin, No connect to anything.	---	Floating
25	NC	Floating Pin, No connect to anything.	---	Floating
26	NC	Floating Pin, No connect to anything.	---	Floating
27	NC	Floating Pin, No connect to anything.	---	Floating
28	NC	Floating Pin, No connect to anything.	---	Floating
29	NC	Floating Pin, No connect to anything.	---	Floating
30	NC	Floating Pin, No connect to anything.	---	Floating
31	GND	Ground	---	---
32	NC	Floating Pin, No connect to anything.	---	Floating
33	GND	Ground	---	---

34	RST_NB	Host-to-BT reset /IND_RST_BT – Independent. GPIO[11]	VDDIO	I
35	JTAG_TCK	JTAG test clock input signal. GPIO[2]	VDDIO	I
36	GND	Ground	---	---
37	USB_DM	USB Serial Differential Data Minus	3.3V	I/O
38	USB_DP	USB Serial Differential Data Plus	3.3V	I/O
39	GND	Ground	---	---
40	HOST_WAKE_WL	Host wake WLAN radio input signal. GPIO[16].	VDDIO	I
41	UART_RTS_N	UART_RTSn (active low)	VDDIO	O
42	UART_TXD	UART_SOUT	VDDIO	O
43	UART_RXD	UART_SIN	VDDIO	I
44	UART_CTS	UART_CTS(active low)	VDDIO	I
45	GND	Ground	---	---
46	RST_WL	Independent software reset for Wi-Fi. GPIO[10]	VDDIO	I/O
47	NC	Floating Pin, No connect to anything.	VDDIO	I/O
48	SPI_INT	SPI interrupt signal / BOOT3	VDDIO	I/O

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	-	3.3	3.96	V
VDDIO	I/O power supply	-	3.3	3.96	V
		-	1.8	2.16	

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	3.14	3.3	3.46	V
VDDIO	1.8V/3.3V digital I/O power supply	3.14	3.3	3.46	V
		1.71	1.8	1.89	

3.3 Digital IO Pin DC Characteristics

3.3.1 1.8V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output high voltage	VIO-0.4	-	-	
V_{OL}	Output low voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.2 3.3V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output High Voltage	VIO-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.4 Host Interface

3.4.1 SDIO Interface

The AW-XM646 supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-XM646 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

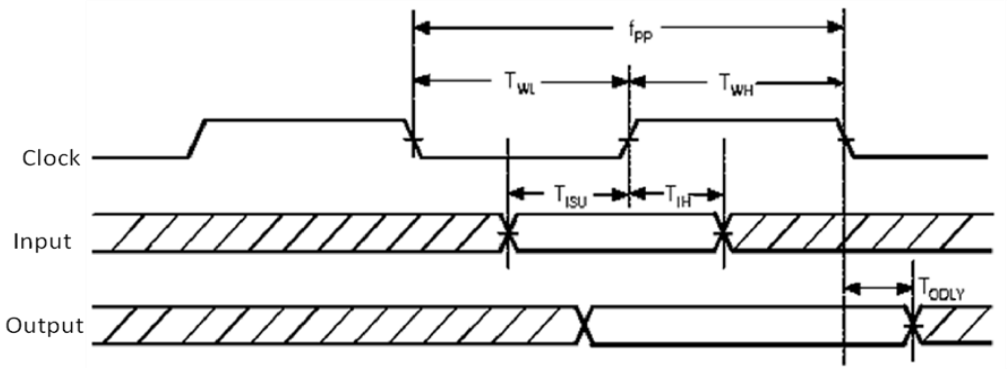
- Support SDIO 3.0 Standard.
- On-chip memory used for CIS.
- Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- Special interrupt register for information exchange.
- Allows card to interrupt host.

SDIO Interface Signals

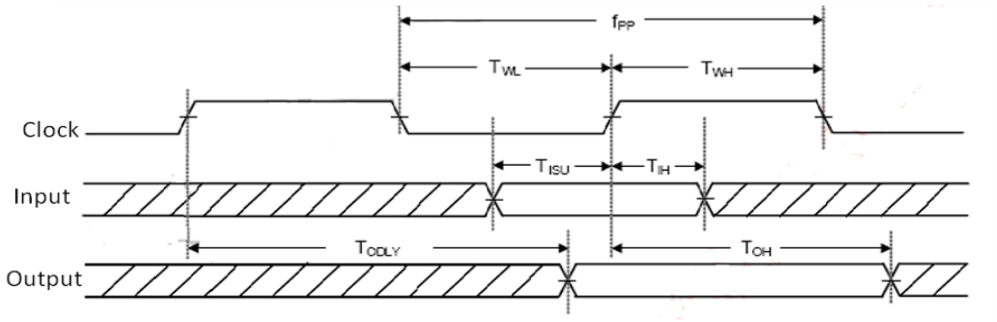
AW-XM646 SDIO Pin Name	Type	Description
SDIO_CLK	I	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
SDIO_CMD	I/O	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
SDIO_DATA3	I/O	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
SDIO_DATA2	I/O	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
SDIO_DATA1	I/O	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
SDIO_DATA0	I/O	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line

3.4.2 SDIO Protocol Timing

3.4.2.1 Default Speed, High-Speed Modes (3.3V)



SDIO protocol timing Diagram - Default mode. (3.3V)

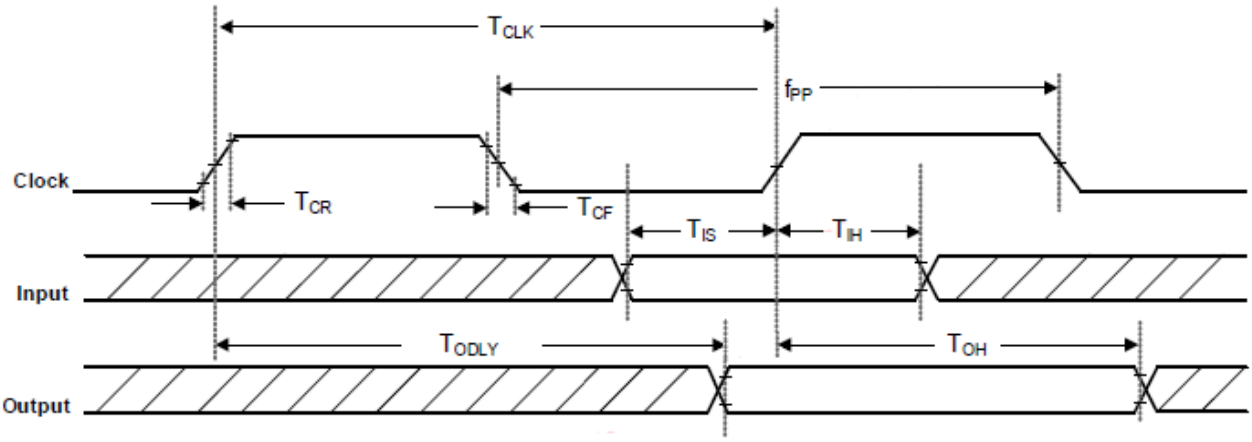


SDIO protocol timing Diagram - High Speed mode. (3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
fpp	CLK Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WH}	CLK High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{WL}	CLK Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time	Normal	--	--	14	ns
	CL ≦ 40pF (1 card)	High Speed	--	--	14	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

SDIO Timing Data – Default Speed / High-Speed modes. (3.3V)

3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

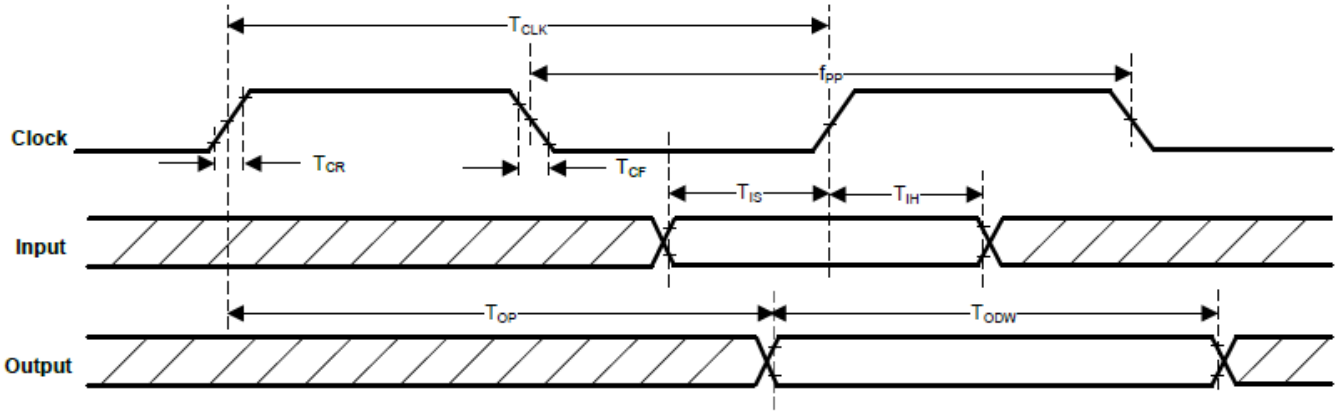


SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes (up to 100 MHz)(1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR12/25/50	25	-	100	MHz
T_{CLK}	Clock Time	SDR12/25/50	10	-	40	ns
T_{IS}	Input Setup Time	SDR12/25/50	3	-	-	ns
T_{IH}	Input Hold Time	SDR12/25/50	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR ,TCF <2ns(max) at 100MHz CCARD =10pF	SDR12/25/50	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output Delay Time CL ≦ 30pF	SDR12/25/50	-	-	7.5	ns
T_{OH}	Output Hold Time CL =15pF	SDR12/25/50	1.5	-	-	ns

SDIO Timing Data - SDR12/25/50 modes. (1.8V)

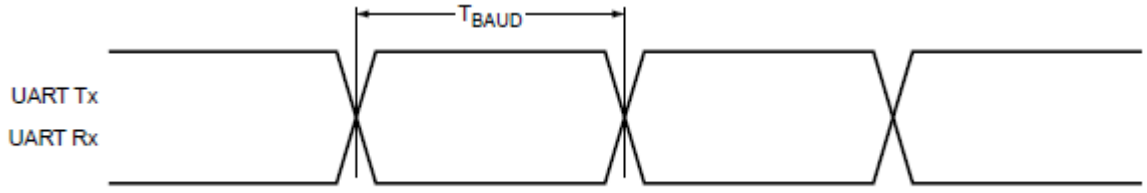
3.4.2.3 SDR104 mode (208MHz) (1.8V)



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR104	0	-	208	MHz
T_{CLK}	Clock Time	SDR104	4.8	-	-	ns
T_{IS}	Input Setup Time	SDR104	1.4	-	-	ns
T_{IH}	Input Hold Time	SDR104	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR,TCF<0.96ns(max) at 208MHz CCARD =10pF	SDR104	-	-	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	-	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	-	-	ns

3.4.3 High-Speed UART Interface

The AW-XM646 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.



Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	26MHz or 40MHz input clock	250	-	-	ns

3.4.4 USB Interface

3.4.4.1 USB LS driver and receiver parameters

Symbol	Parameter	Min	Typ	Max	Units
BR	Valid power to PDn deasserted	-	1.5	-	Mbit/s
BR_{PPM}	Input high voltage	-15000.0	-	15000.0	ppm
Driver specifications					
V_{OH}	Output single ended high Defined with 1.425 kΩ pull-up resistor to 3.6V	2.8	-	3.6	V
V_{OL}	Output single ended low Defined with 1.425 kΩ pull-down resistor to ground	0.0	-	0.3	V
V_{CRS}	Output single crossover voltage	1.3	-	2.0	V
T_{LR}	Data fall time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75.0	-	300.0	ns
T_{LF}	Data rise time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75.0	-	300.0	ns
T_{LRFM}	Rise and fall time matching	80.0	-	125.0	%
T_{UDJ1}	Source jitter total: to next transition • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of	-95.0	-	95.0	ns

	differential data signals.				
T_{UDJ2}	Source jitter total: for paired transitions • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-150.0	-	150.00	ns
Receiver specifications					
V_{IH}	Input single ended high	2.0	-	-	V
V_{IL}	Input single ended low	-	-	0.8	V
V_{DI}	Differential input sensitivity	0.2	-	-	V

3.4.4.2 USB FS driver and receiver parameters

Symbol	Parameter	Min	Typ	Max	Units
BR	Baud rate	-	12.0	-	Mbit/s
BR_{PPM}	Baud rate tolerance	-2500.0	-	2500.0	ppm
Driver specifications					
V_{OH}	Output single ended high Defined with 1.425 kΩ pull-up resistor to 3.6V.	2.8	--	3.6	V
V_{OL}	Output single ended low Defined with 1.425 kΩ pull-down resistor to ground	0.0	--	0.3	V
V_{CRS}	Output single crossover voltage	1.3	-	2.0	V
T_{FR}	Data fall time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4.0	-	20.0	ns
T_{FL}	Data rise time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4.0	-	20.0	ns
T_{DJ1}	Source jitter total: to next transition • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-3.5	-	3.5	ns
T_{DJ2}	Source jitter total: for paired transitions • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-4.0	-	4.0	ns

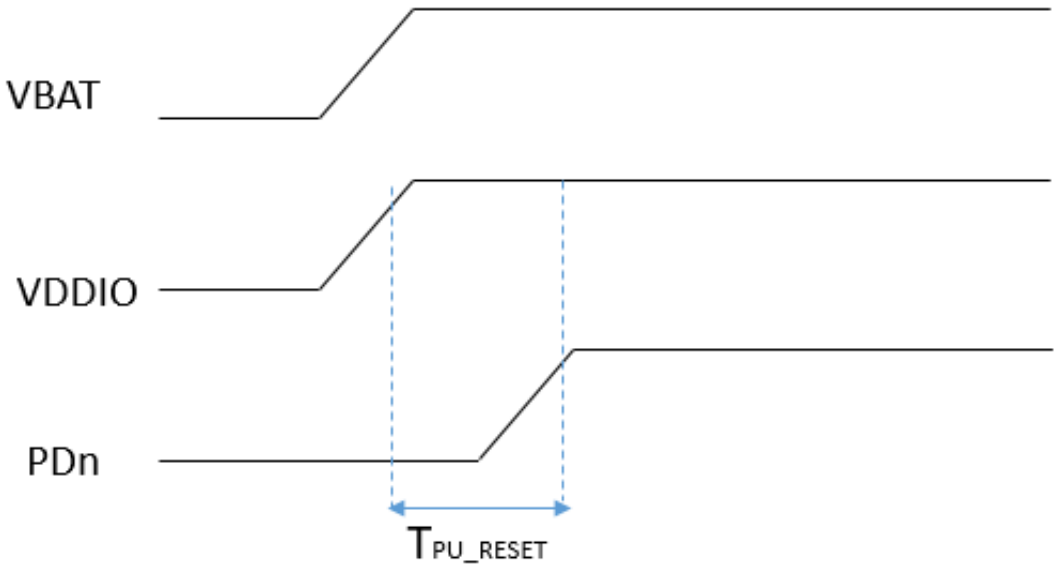
T_{FDEOP}	Source jitter for differential transition to SE0 transition Defined at crossover point of differential data signals.	-2.0	-	5.0	ns
Receiver specifications					
V_{IH}	Input single ended high	2.0	-	-	V
V_{IL}	Input single ended low	-	-	0.8	V
V_{DI}	Differential input sensitivity	0.2	-	-	V
TJR1	Receiver jitter: to next transition Defined at crossover point of differential data signals.	-18.5	-	18.5	ns
TJR2	Receiver jitter: for paired transitions Defined at crossover point of differential data signals.	-9.0	-	9.0	ns

3.4.4.3 USB HS driver and receiver parameters

Symbol	Parameter	Min	Typ	Max	Units
BR	Baud rate	-	480.0	-	Mbit/s
BR_{PPM}	Baud rate tolerance	-500.0	-	500.0	ppm
Driver specifications					
V_{HSOH}	Data signaling high	360.0	-	440.0	mV
V_{HSOL}	Data signaling low	-10.0	-	10.0	mV
T_{HSR}	Data rise time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	500.0	-	-	ns
T_{HSF}	Data fall time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-500.0	-	-	ns
Receiver specifications					
V_{HSCM}	Input single ended low	-50	-	500.00	mV

3.5 Timing Sequence

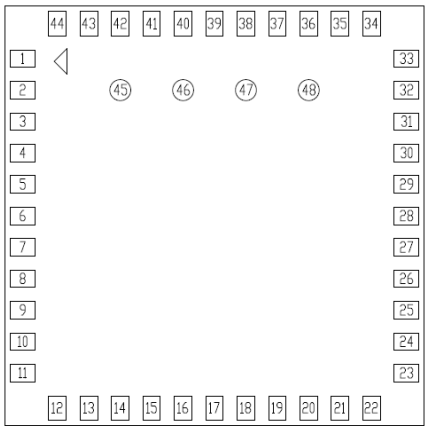
AW-XM646 power up timing sequence.



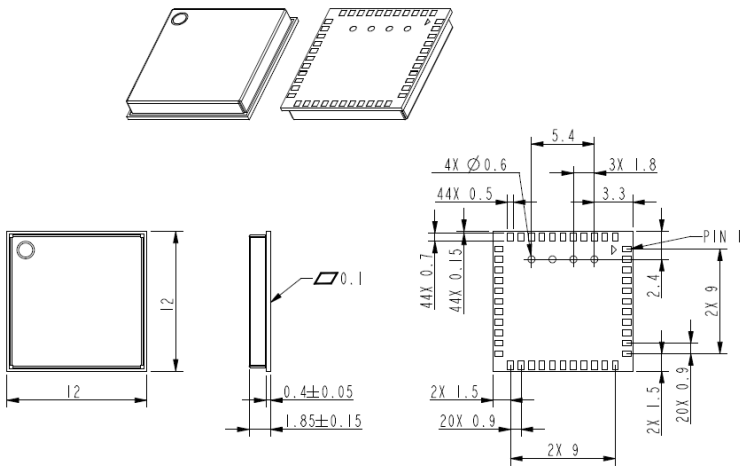
Symbol	Parameter	Min	Typ	Max	Units
TPU_RESET	Valid power to PDn deasserted	0	-	-	ms
V_{IH}	Input high voltage	1.75	-	3.63	V
V_{IL}	Input low voltage	-0.4	-	0.2	V

4. Mechanical Information

4.1 Mechanical Drawing



PIN DEFINED (TOP VIEW)



TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

FCC:

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE:

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

IMPORTANT NOTE:

This module is intended for OEM integrator. This module is only FCC authorized for the specific rule parts listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.
Additional testing and certification may be necessary when multiple modules are used.
OEM integrators that they must use the equivalent antennas or C2PC will be required.

The host manufacturer should reference KDB Publication 996369 D04 Module Integration Guide.

USERS MANUAL OF THE END PRODUCT:

In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following " Contains TX FCC ID: TLZ-XM646".

This equipment complies with FCC mobile radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

Ant list

Ant.	Brand	Model Name	Antenna Type	Connector	Gain (dBi)
1	ARISTOTLE	RFA-27-JP326MHF4C198	PIFA Antenna	I-PEX	Note1

Note1:

Ant.	Gain (dBi)	
	WLAN 2.4GHz/Bluetooth/802.15.4	WLAN 5GHz/6GHz
1	3.5	5

This device is restricted for indoor use.
The antenna is limited as the antenna listed.

AW-XM646x Series

IEEE 802.11 a/b/g/n/ac/ax Wireless LAN 1T1R and BLE/802.15.4 Solution Family 12 x 12 LGA Module

Layout Guide

Rev. 01

(For Standard)

Revision History

Version	Revision Date	Description	Initials	Approved
01	2025/03/05	• Initial Version	Roger Liu	N.C. Chen

INTRODUCTION

This document provides key guidelines and recommendations to be followed when creating AW-XM646 layout. It is strongly recommended that layouts be reviewed by the AzureWave engineering team before being released for fabrication.

The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

- GENERAL RF GUIDELINES
- Ground Layout
- Power Layout
- Digital Interface
- RF Trace
- Antenna
- Antenna Matching
- GENERAL LAYOUT GUIDELINES
- THE OTHER LAYOUT GUIDE INFORMATION

1. GENERAL RF GUIDELINES

Follow these steps for optimal WLAN performance.

1. Control WLAN 50 ohm RF traces by doing the following:
   - Route traces on the top layer as much as possible and use a continuous reference ground plane underneath them.
   - Verify trace distance from ground flooding. At a minimum, there should be a gap equal to the width of one trace between the trace and ground flooding. Also keep RF signal lines away from metal shields. This will ensure that the shield does not detune the signals or allow for spurious signals to be coupled in.
   - Keep all trace routing inside the ground plane area by at least the width of a trace.
   - Check for RF trace stubs, particularly when bypassing a circuit.

2. Keep RF traces properly isolated by doing the following:
   - Do not route any digital or analog signal traces between the RF traces and the reference ground.
   - Keep the balls and traces associated with RF inputs away from RF outputs. If two RF traces are close each other, then make sure there is enough room between them to provide isolation with ground fill.
   - Verify that there are plenty of ground vias in the shield attachment area. Also verify that there are no non-ground vias in the shield attachment area. Avoid traces crossing into the shield area on the shield layer.

3. Consider the following RF design practices:
   - Confirm antenna ground keep-outs.
   - Verify that the RF path is short, smooth, and neat. Use curved traces or microwave corners for all turns; never use 90-degree turns. Avoid width discontinuities over pads. If trace widths differ significantly from component pad widths, then the width change should be mitered. Verify there are no stubs.
   - Do not use thermals on RF traces because of their high loss.
   - The RF traces between AW-XM646 RF_ANT pin and antenna must be made using 50Ω controlled-impedance transmission line.

2. Ground Layout

Please follow general ground layout guidelines. Here are some general rules for customers' reference.

- The layer 2 of PCB should be a complete ground plane. The rule has to be obeyed strictly in the RF section while RF traces are on the top layer.
- Each ground pad of components on top layer should have via drilled to PCB layer 2 and via should be as close to pad as possible. A bulk decoupling capacitor needs two or more.
- Don't place ground plane and route signal trace below printed antenna or chip antenna to avoid destroying its electromagnetic field, and there is no organic coating on printed antenna. Check antenna chip vendor for the layout guideline and clearance.
- Move GND vias close to the pads.

3. Power Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

- A 4.7uF capacitor is used to decouple high frequency noise at digital and RF power terminals. This capacitor should be placed as close to power terminals as possible.
- In order to reduce PCB's parasitic effects, placing more via on ground plane is better.

4. Digital Interface

Please follow power and ground layout guidelines. Here are some general rules for customers' reference.

- The digital interface to the module must be routed using good engineering practices to minimize coupling to power planes and other digital signals.
- The digital interface must be isolated from RF trace.

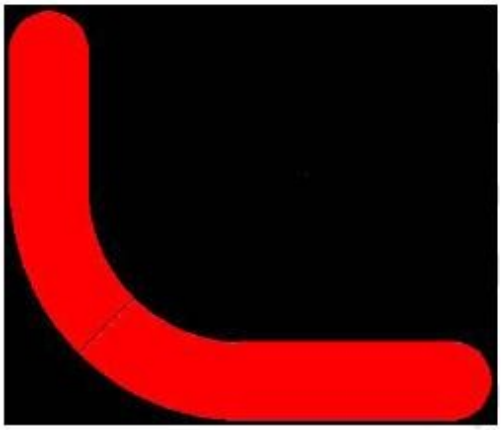
5. RF Trace and RF PAD

A. RF Trace

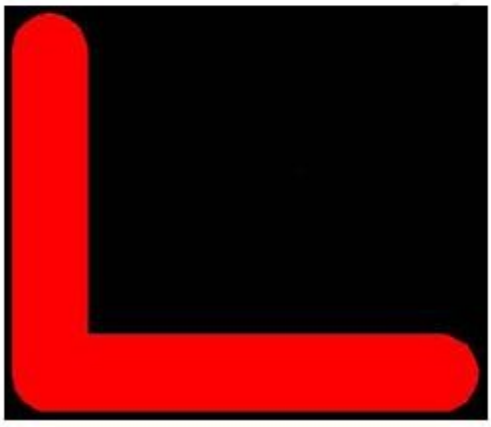
The RF trace is the critical to route. Here are some general rules for customers' reference.

- The RF trace impedance should be 50Ω between ANT port and antenna matching network.
- The length of the RF trace should be minimized.
- To reduce the signal loss, RF trace should laid on the top of PCB and avoid any via on it.
- The CPW (coplanar waveguide) design and the microstrip line are both recommended; the customers can choose either one depending on the PCB stack of their products.
- The RF trace must be isolated with aground beneath it. Other signal traces should be isolated from the RF trace either by ground plane or ground vias to avoid coupling.
- To minimize the parasitic capacitance related to the corner of the RF trace, the right angle corner is not recommended.

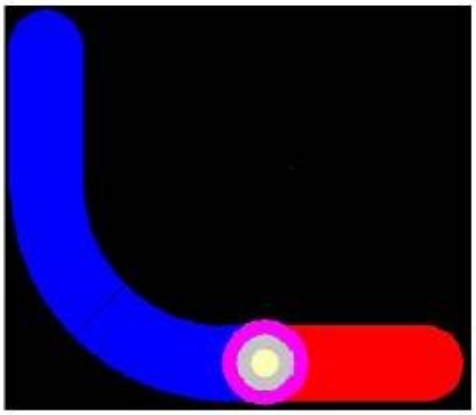
If the customers have any problem in calculation of trace impedance, please contact AzureWave.



Correct RF trace



Right-angled corner

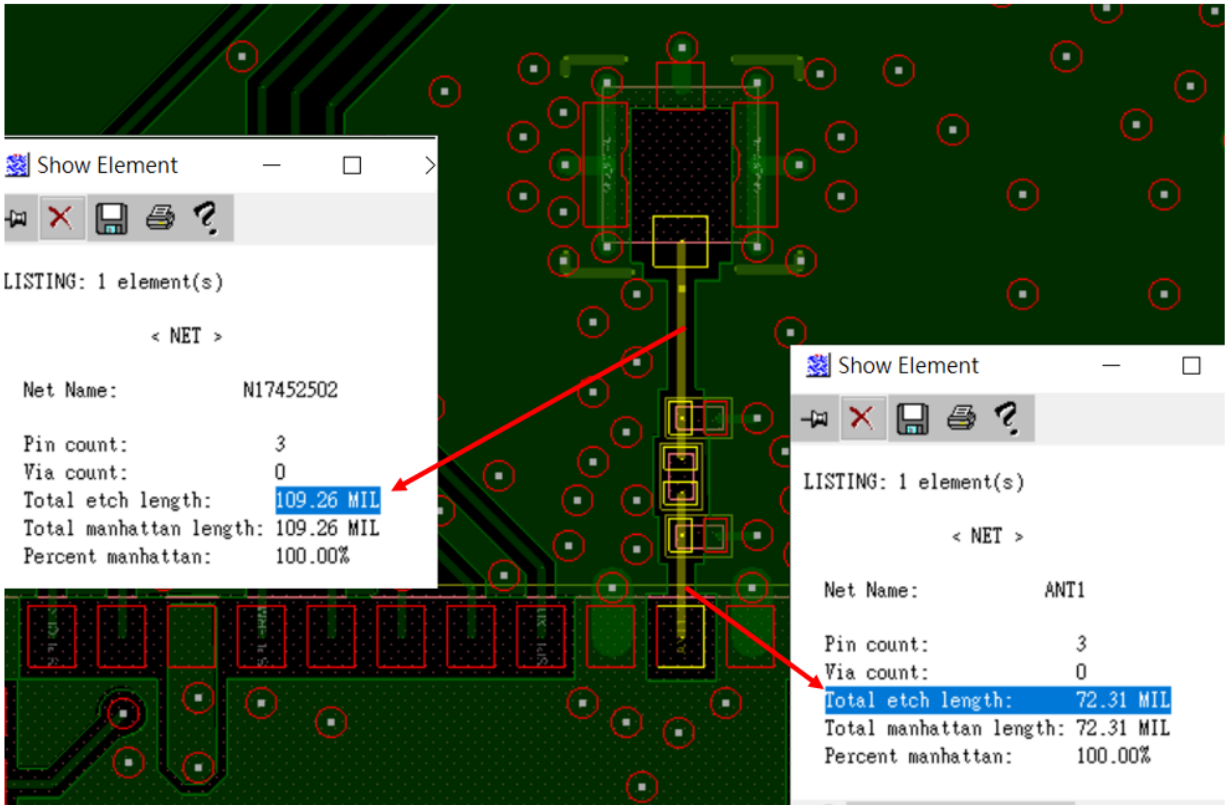


Via on RF trace

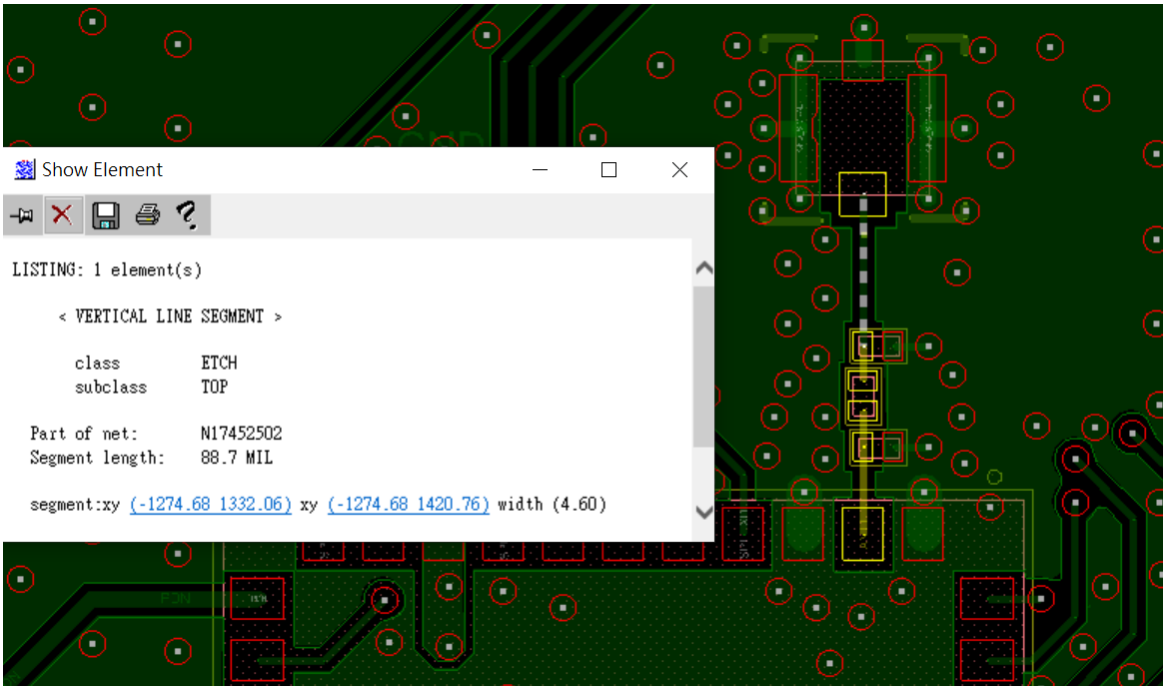
Incorrect RF trace

AW-XM646 RF trace should be follow the rules as below

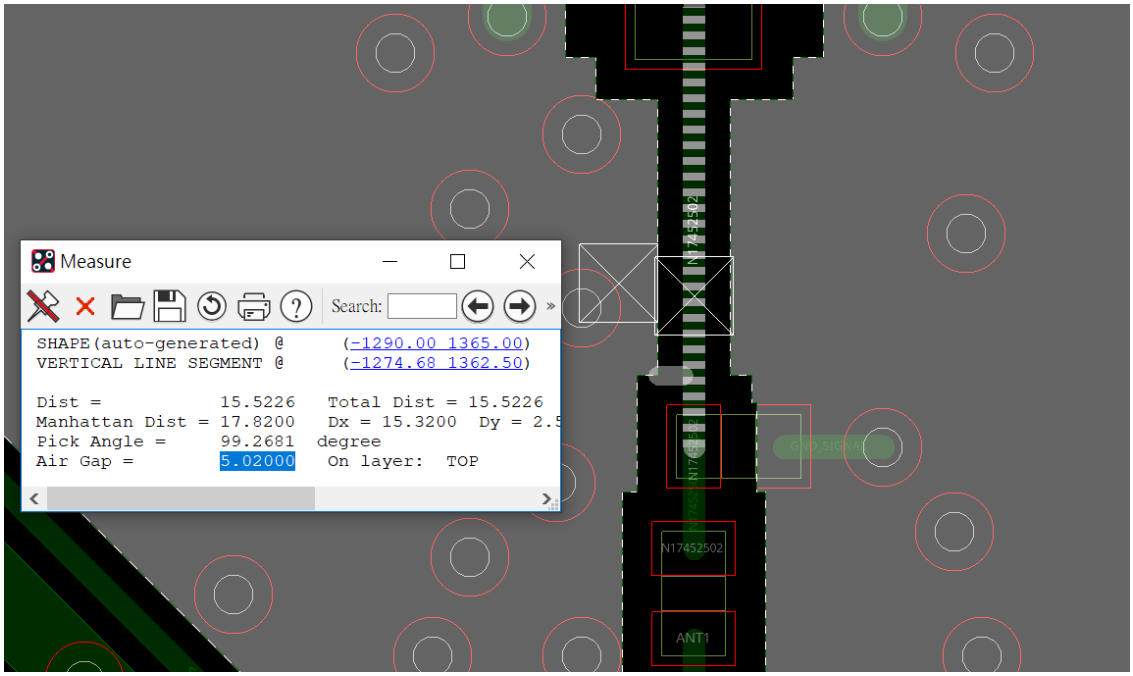
a. Line length of Antenna trace about 109.26 mil and 72.31 mil



b. Line width of Antenna trace about 4.6 mil

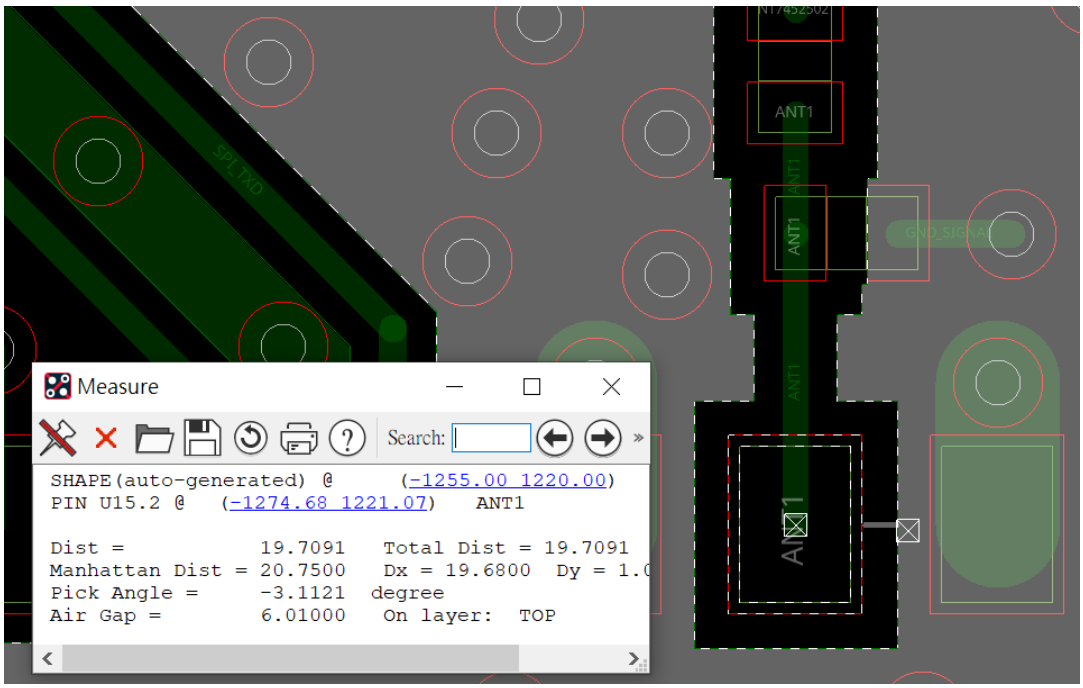


c. Air gap between RF trace and ground about 5 mil

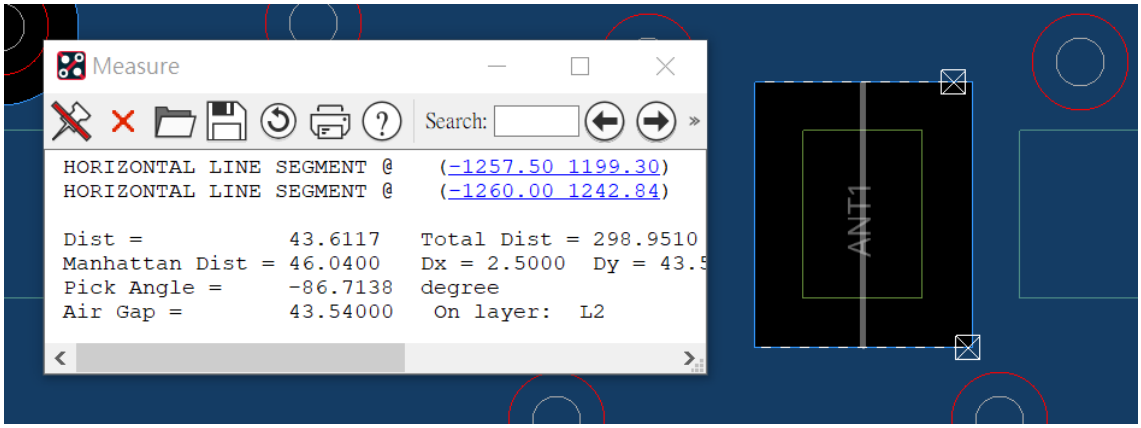


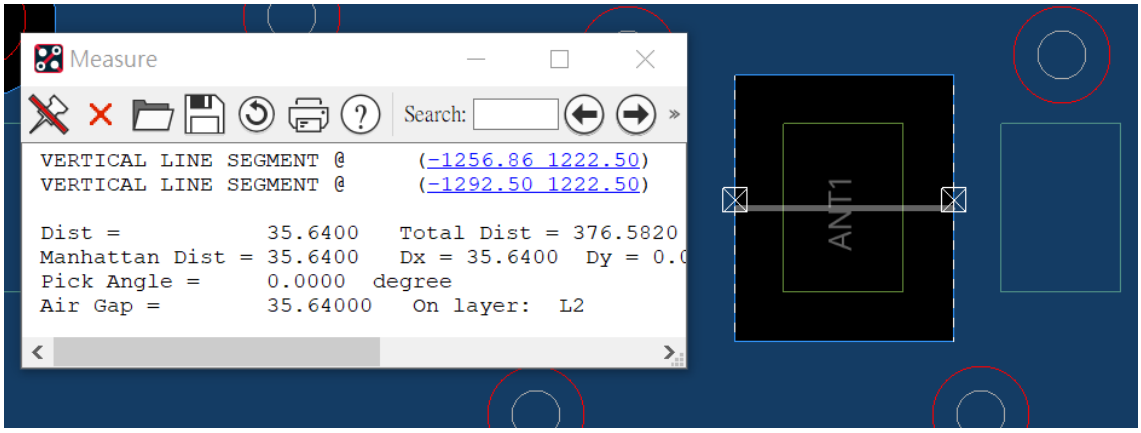
B. RF PAD

TOP layer: Air gap between RF PAD and ground is 6 mil

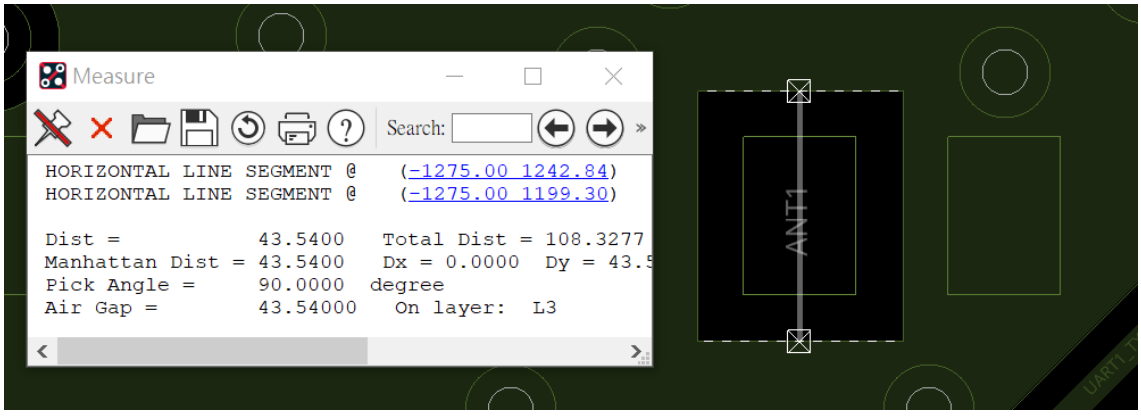


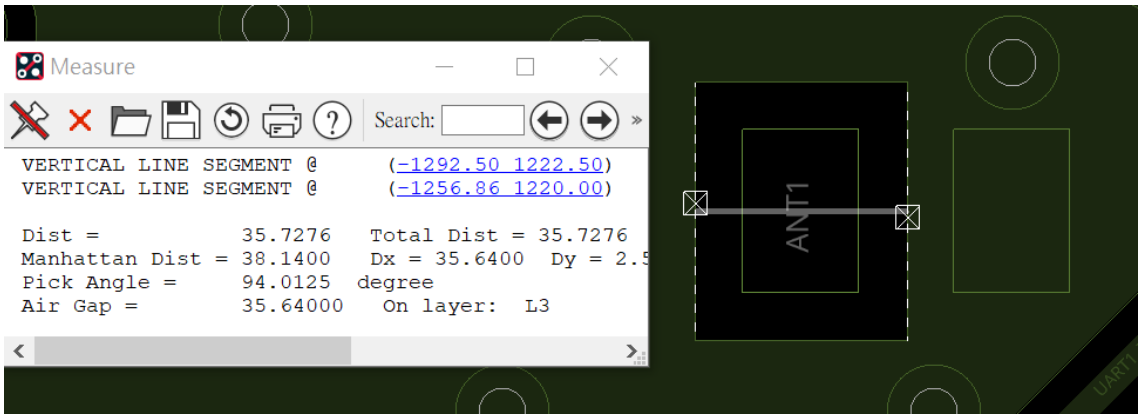
Inner Layer (L2): the length and width of keep out under RF PAD is 43.5 and 35.6 mil.





Inner Layer (L3): the length and width of keep out under RF PAD is 43.5 and 35.6 mil.





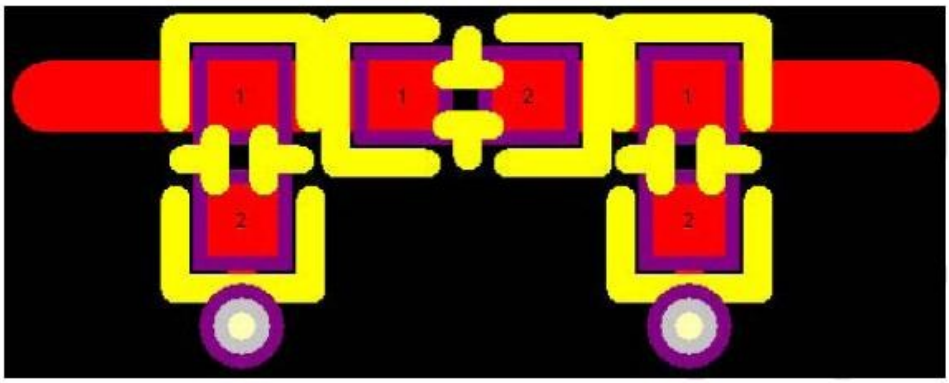
Bottom Layer: must be continuous reference ground plane

6. Antenna

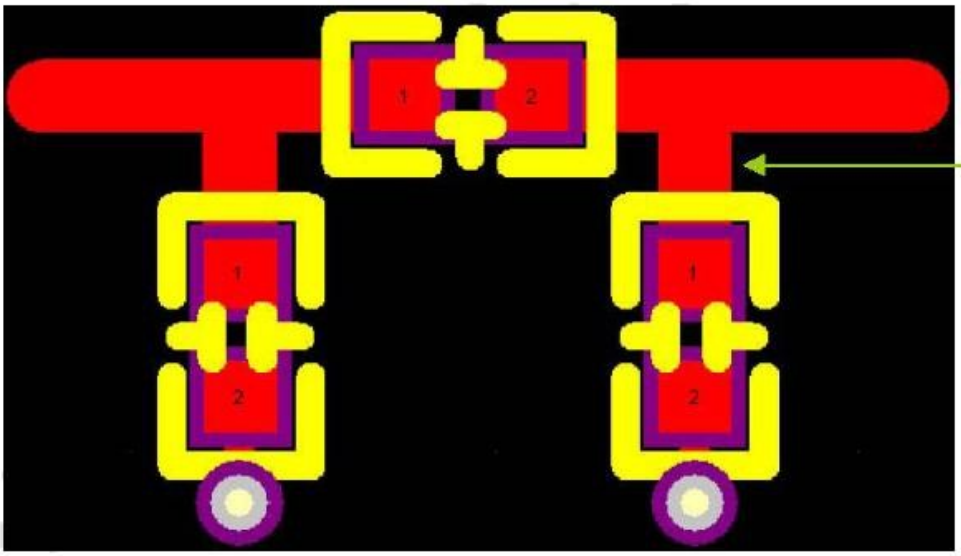
All the high-speed traces should be moved far away from the antenna. For the best radiation performance, check antenna chip vendor for the layout guideline and clearance.

7. Antenna Matching

PCB designer should reserve an antenna matching network for post tuning to ensure the antenna performance in different environments. Matching components should be close to each other. Stubs should also be avoided to reduce parasitic while no shunt component is necessary after tuning.



Correct layout for antenna matching



Incorrent layut for antenna matching

8. SHIELDING CASE

Magnetic shielding, ferrite drum shielding, or magnetic-resin coated shielding is highly recommended to prevent EMI issues.

9. GENERAL LAYOUT GUIDELINES

Follow these guidelines to obtain good signal integrity and avoid EMI:

1. Place components and route signals using the following design practices:
   - Keep analog and digital circuits in separate areas.

- Identify all high-bandwidth signals and their return paths. Treat all critical signals as current loops. Check each critical loop area before the board is built. A small loop area is more important than short trace lengths.
- Orient adjacent-layer traces so that they are perpendicular to one another to reduce crosstalk.
- Keep critical traces on internal layers, where possible, to reduce emissions and improve immunity to external noise.
- However, RF traces should be routed on outside layers to avoid the use of vias on these traces.
- Keep all trace lengths to a practical minimum. Keep traces, especially RF traces, straight wherever possible. Where turns are necessary, use curved traces or two 45-degree turns. Never use 90-degree turns.

2. Consider the following with respect to ground and power supply planes:
   - Route all supply voltages to minimize capacitive coupling to other supplies. Capacitive coupling can occur if supply traces on adjacent layers overlap. Supplies should be separated from each other in the stack-up by a ground plane, or they should be coplanar (routed on different areas of the same layer).
   - Provide an effective ground plane. Keep ground impedance as low as possible. Provide as much ground plane as possible and avoid discontinuities. Use as many ground vias as possible to connect all ground layers together.
   - Maximize the width of power traces. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.

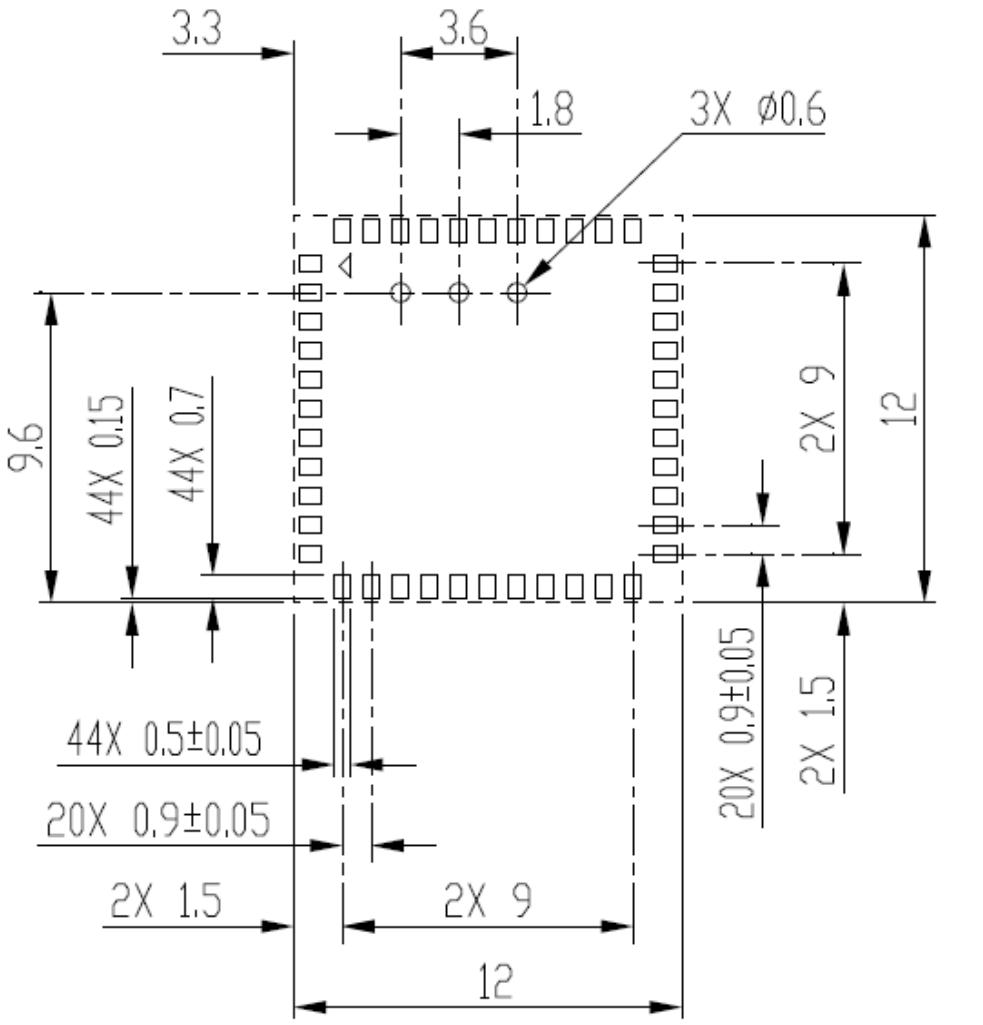
3. Consider these power supply decoupling practices:
   - Place decoupling capacitors near target power pins. If possible, keep them on the same side as the IC they decouple to avoid vias that add inductance. If a filter component cannot be directly connected to a given power pin with a very short and fat etch, do not connect it by a copper trace. Instead, make the connection directly to the associated planes using vias.
   - Use appropriate capacitance values for the target circuit, and consider each capacitor's self-resonant frequency.

10. Module stencil and Pad opening Suggestion

- Stencil thickness：0.10~0.12mm
- Function Pad opening size suggestion: Max. 1:1

  PS: This opening suggestion is just for customer reference, please discuss with AzureWave's Engineer before you start SMT.

- Solder Printer Opening and Customer PCB Footprint suggestion.
- Example:



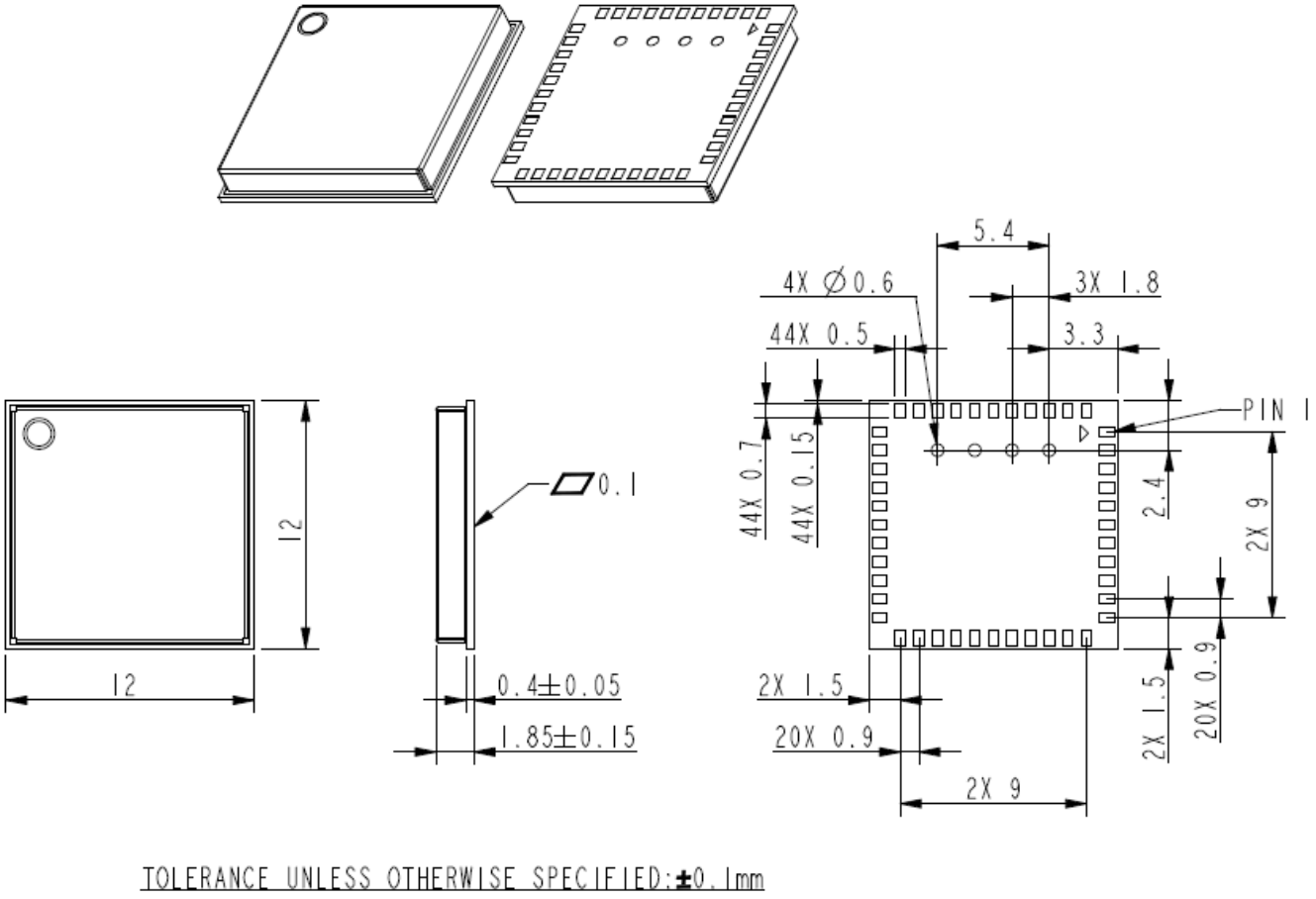
(Top View)

11. The other layout guide Information

- Make sure every power traces have good return path (ground path).
- Connect the input pins of unused internal regulators to ground.
- Leave the output pins of unused internal regulators floating.
- High speed interface (i.e. UART/SDIO/HSIC) shall have equal electrical length. Keep them away from noise sensitive blocks.
- Good power integrity of VDDIO will improve the signal integrity of digital interfaces.
- Good return path and well shielded signal can reduce crosstalk, EMI emission and improve signal integrity.
- RF IO is around 50 ohms, reserve Pi or T matching network to have better signal transition from port to port.
- Smooth RF trace help to reduce insertion loss. Do not use 90 degrees turn (use two 45 degrees turns or one miter bend instead).
- Well-arranged ground plane near antenna and antenna itself will help to reduce near field coupling between other RF sources (e.g. GSM/CDMA … antennas).
- Discuss with AzureWave Engineer after you finish schematic and layout job.

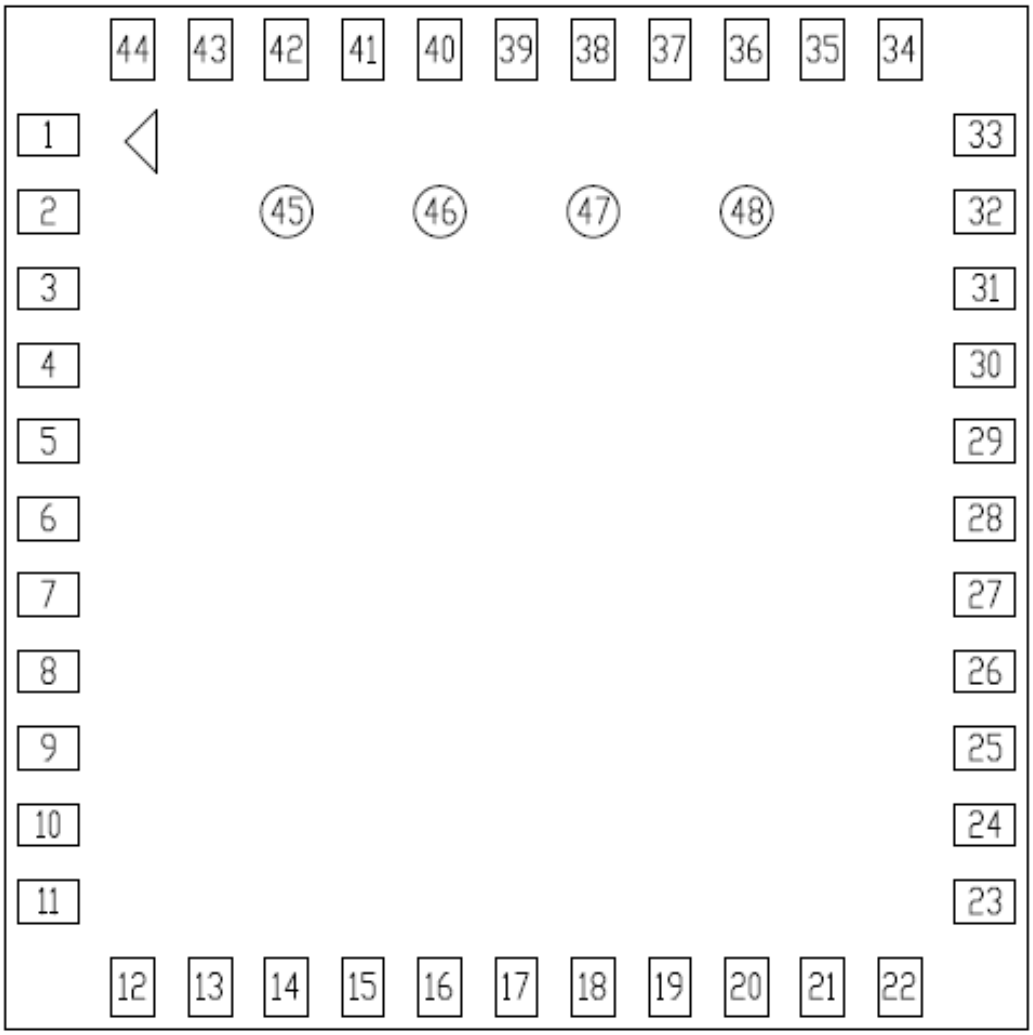
12. Mechanical Drawing

- **Package Outline Drawing**



TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

- **Top View of PCB Layout Foot Print**



PIN DEFINED (TOP VIEW)