AzureWave Technologies, Inc.

AW-XM606

IEEE 802.11a/b/g/n/ac/ax Wi-Fi with Bluetooth

Combo LGA Module

Datasheet

Rev. D

DF

(For Standard)

AzureWave Technologies, Inc.

Features

WLAN

- IEEE 802.11a/b/g/n/ac/ax compliant
- Tri-band (2.4 GHz/5 GHz/6 GHz)
- 1x1 with 20 MHz channels supporting PHY data rates up to 802.11ax (MCS11 1024-QAM 5/6)
- Wi-Fi 6 release features
  - OFDMA uplink and downlink as STA
  - Downlink multi-user MIMO as STA
  - Individual target-wake-time (TWT)
  - BSS color
- - Interfaces
  - SDIO 2.0/3.0 : up to 100 Mbps sustained throughput
  - GSPI: up to 20 Mbps sustained throughput
- Modes: STA, SoftAP, Wi-Fi Direct
- Security
  - TKIP, WEP, WPA2 (Personal/Enterprise), WPA3 (Personal/Enterprise/192b)

Bluetooth

- Bluetooth® 5.4 (BDR + EDR + Bluetooth® Low Energy)
- All Bluetooth® 5.0/5.1/5.2/5.3/5.4 optional features
  - Host to Controller Encryption Key Control Enhancements
  - LE long range
  - LE 2Mbps
  - LE mesh
  - Advertising extensions
  - LE audio with LC3 codec in ROM in offload mode or HCI mode with LC3 codecs on host
  - LE Isochronous Channels
- Bluetooth® LNA can be shared with WLAN LNA for reduced antenna count
- Dedicated Bluetooth® LNA for improved RF and coexistence performance
- 0, +13, and +20 dBm Bluetooth® PA paths optimized for best efficiency, output power options adjustable in 4dB steps.
- UART interface (4-wire)
- Two audio interfaces, supporting hands free profile (HFP), A2DP, and LE audio.
- TDM1, TDM2 supporting inter-IC sound (I2S) (2-channels) and PCM (8-channels), 8k to 96k sample rates, and16- and 24-bit sample widths
- Bidirectional PCM (TDM and I2S) with 8k, 16k sample rates and 16-bit sample width for HFP. Multiplexed with TDM2 through second audio interface.
- Single-direction I2S with 44.1k. The 48k sample rates and 16-bit sample width for A2DP. Multiplexed with TDM2 through second audio interface.

- On-chip memory includes 768 KB SRAM and 2048 KB ROM

Revision History

Document NO: R2-2606-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2024/03/27	DCN031274	● Initial version	QM.Tan	N.C.Chen
B	2024/06/14	DCN031748	● Update ESD Specification ● Update Pin Map Description ● Update Power Consumption	QM.Tan	N.C.Chen
C	2024/11/13	DCN032641	● Update RF specification ● Update Operating Conditions ● Update Pin Table ● Update Power Consumption ● Removed JTAG	Tom Hsieh	N.C.Chen
D	2025/03/25	DCN033828	● Update Pin Table ● Update Frequency Reference	Tom Hsieh	N.C.Chen
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1. Introduction

1.1 Product Overview

The AW-XM606 is an low-power, single-chip device that supports single-stream, tri-band, Wi-Fi 6/6E, IEEE802.11ax-compliant Wi-Fi MAC/baseband/radio and Bluetooth®/Bluetooth® Low Energy 5.4. In 802.11ax mode, the device supports rates up to 1024 QAM MCS11 in 20 MHz channels. All legacy rates in the 802.11a/b/g/n/ac are also supported. Included on-chip are 2.4 GHz, 5-7 GHz transmit power amplifiers (PA) and low-noise amplifiers (LNA). An SDIO v3.0 interface or GSPI are available for interfacing with the host.

The AW-XM606 includes a Bluetooth® subsystem that is Bluetooth® 5.4-compliant, supporting basic rate, enhanced data rate (EDR) and Bluetooth® Low Energy. The device supports Bluetooth® Low Energy 2 Mbps, Bluetooth® Low Energy 1 Mbps, low-energy mesh, low-energy long range (LR), advertising extensions. The device can support Bluetooth® Low Energy audio, with LC3 codec running on the device enabling typical Smart watch audio use cases. A pair of time-division multiplexing (TDM) interfaces enables a flexible interface for various audio use cases and a PDM interface is available for connecting digital microphones. The device includes on-chip power amplifiers supporting three different output power paths optimized for best efficiency, 0 dBm, +13 dBm, and +20 dBm path for driving poor antennas in wearable devices. A 4-wire UART interface is available for interfacing with the host.

The CYW55513 is designed to address the needs of Internet on Things (IoT) devices that require minimal power consumption and compact size. It includes a power management unit (PMU), and a internal 37.4 MHz crystal which provides the system reference clock, and can operate from an external 32.768 kHz crystal (eLPO) for higher accuracy.

The AW-CM606 operates over the TBD temperature range, and is available in 12x12 mm package.

1.2 Block Diagram

TBD

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11a/b/g/n/ac/ax Wi-Fi with Bluetooth Combo LGA Module
Major Chipset	Infineon CYW55513(WLBGA-143-ball)
Host Interface	Wi-Fi: SDIO , BT: UART/PCM
Dimension	12mm(L) 12xmm(W) x 1.75 mm(H) (Typical)
Form factor	LGA Module 63 pin
Antenna	1T1R for WiFi/BT ANT1(Main)：WiFi/Bluetooth → TX/RX
Weight	0.5g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11a/b/g/n/ac/ax, Wi-Fi compliant
Frequency Rage	WLAN: 2.4 / 5 / 6 GHz Band
Modulation	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9), 1024-QAM(MCS10~11)
Number of Channels	**2.4GHz** ■ USA, NORTH AMERICA, Canada and Taiwan – 1 ~ 11 ■ China, Australia, Most European Countries – 1 ~ 13 **5GHz** ■ USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165 **6GHz** ■ CH1~CH233

Output Power[1][2][3] (Board Level Limit)*

2.4G

	Min	Typ	Max	Unit
11b (11Mbps) @ EVM≦-9 dB	17	19	21	dBm
11g (54Mbps) @EVM≦-25 dB	16	18	20	dBm
11n (HT20 MCS7) @EVM≦-27 dB	15	17	19	dBm
11ax (HE20 MCS11) @EVM≦-35 dB	13	15	17	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps) @EVM≦-25 dB	14.5	16.5	18.5	dBm
11n (HT20 MCS7) @EVM≦-27 dB	13	15	17	dBm
11ac (VHT20 MCS8) @EVM≦-30 dB	12	14	16	dBm
11ax (HE20 MCS11) @EVM≦-35 dB	11	13	15	dBm

6G

	Min	Typ	Max	Unit
11ax (HE20 MCS11) @EVM≦-35 dB	8	10	12	dBm

Receiver Sensitivity

2.4G

	Min	Typ	Max	Unit
11b (11Mbps)		-89	-86	dBm
11g (54Mbps)		-76	-73	dBm
11n (HT20 MCS7)		-76	-73	dBm
11ax (HE20 MCS11)		-63	-60	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps)		-74	-71	dBm
11n (HT20 MCS7)		-74	-71	dBm
11ac (VHT20 MCS8)		-70	-67	dBm

[1] EVM Spec are under typical test conditions.
[2] Output Power means measurement power inside the range (Min and Max) with spectral mask and EVM compliance.
[3] Tx power variation +3.0 dB for process, voltage, and temperature variation across -40'C to +85°C.

	11ax (HE20 MCS11) | | -60 | -57 | dBm **6G** | | Min | Typ | Max | Unit | | 11ax (HE20 MCS11) | | -61 | -56 | dBm |
Data Rate	802.11b: 1, 2, 5.5, 11Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n: MCS0~7 HT20 802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11ac: MCS0~8 VHT20 802.11ax: MCS10~11 HE20
Security	● WEP,WPA/WPA2/WPA3 Enterprise with 192-bit Encryption, hardware accelerator (AES) ● AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility. ● Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS).

*** If you have any certification questions about output power please contact FAE directly.**
**** Project is in engineering stage, RF performance is still being verified.**

1.3.3 Bluetooth

Features	Description
Bluetooth Standard	BT5.4+Enhanced Data Rate (EDR)
Bluetooth VID/PID	N/A
Frequency Rage	2402MHz~2480MHz
Modulation	Header GFSK Payload 2M: 4-DQPSK Payload 3M: 8DPSK
Output Power	| | Min | Typ | Max | Unit | | BR | 3 | 6.5 | 10 | dBm | | BLE(1M) | 3 | 6.5 | 10 | dBm | | BLE(2M) | 3 | 6.5 | 10 | dBm |
Receiver Sensitivity[3]	| | Min | Typ | Max | Unit | | BR | | -86 | -83 | dBm | | BLE(1M) | | -89 | -86 | dBm | | BLE(2M) | | -86 | -83 | dBm |

1.3.4 Operating Conditions

Operating Conditions

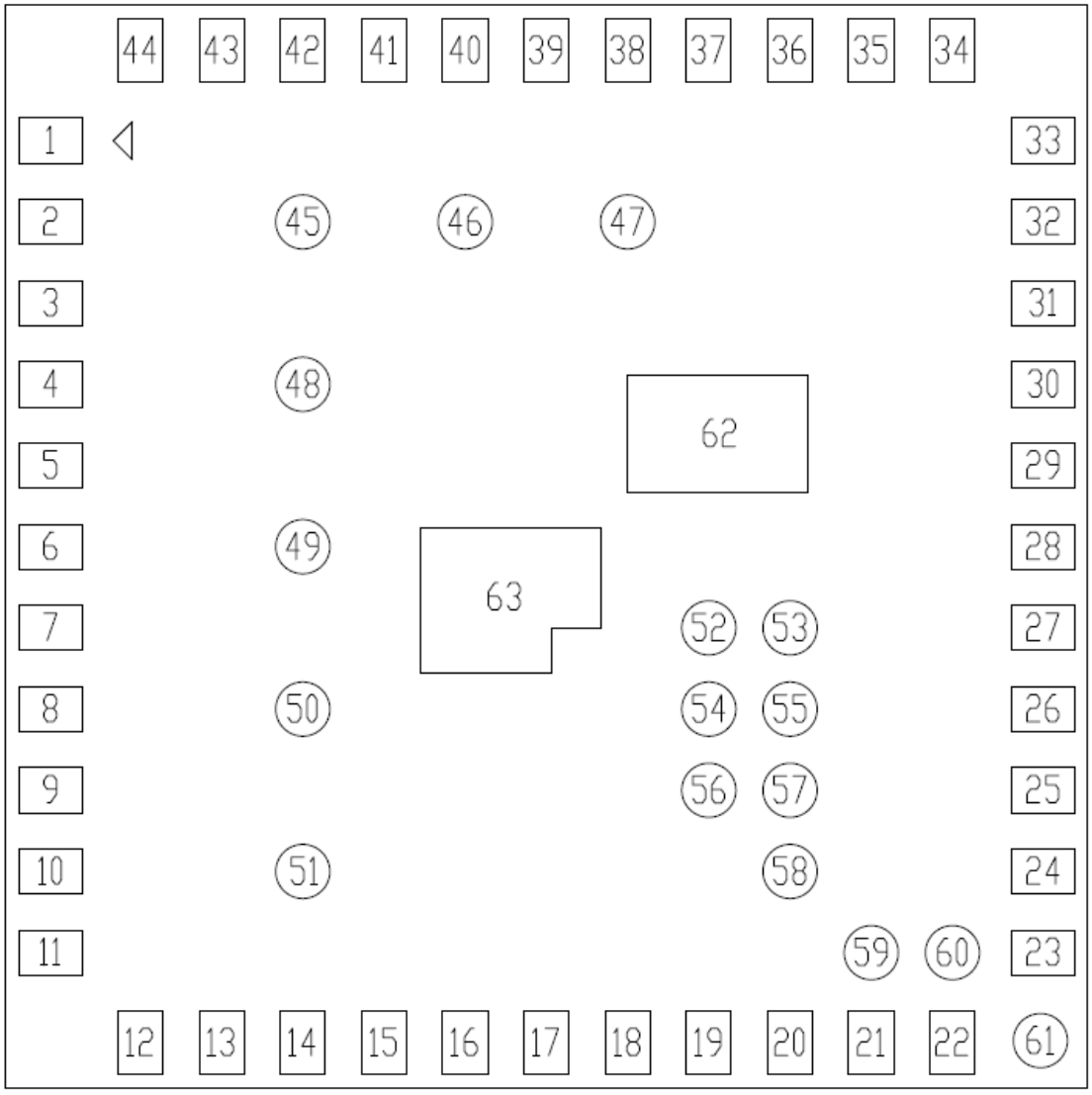
[3] Tested by sLNA.

Voltage	Power supply for host:3.3V
Operating Temperature	-40℃~85℃[4]
Operating Humidity	less than 85% R.H.
Storage Temperature	-40℃~85℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	±2000V
Changed Device Model	±250V

[4] -40℃~85℃ is Functional operation, for detail please check with AzureWave FAE.

2. Pin Definition

2.1 Pin Map



AW-XM606 Pin Map (Top View)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND	Ground.		GND
2	WL_BT_ANT	WLAN/BT RF TX/RX path.		RF
3	GND	Ground.		GND
4	GPIO_2	GPIO configuration pin	VDDIO	I/O
5	GPIO_3	GPIO configuration pin	VDDIO	I/O
6	BT_DEV_WAKE	BT Device Wake	VDDIO	I
7	BT_HOST_WAKE	BT Host Wake	VDDIO	O
8	GPIO_4	GPIO configuration pin		I/O
9	VBAT	3.3V power pin	VBAT	VCC
10	NC	Floating Pin, No connect to anything.		Floating
11	NC	Floating Pin, No connect to anything.		Floating
12	WL_REG_ON	Used by PMU to power up or power down the internal regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in reset. This pin has an internal 50 KΩ pull down resistor that is auto enabled and disabled upon recognizing high on this pin.. It can be disabled through programming.	VDDIO	I
13	WL_SDIO_HOSTWAKE	WL Host Wake	VDDIO	O
14	SDIO_DATA2	SDIO Data Line 2	VDDIO	I/O
15	SDIO_DATA3	SDIO Data Line 3	VDDIO	I/O
16	SDIO_CMD	SDIO Command Input	VDDIO	I/O
17	SDIO_CLK	SDIO Clock Input	VDDIO	I
18	SDIO_DATA0	SDIO Data Line 0	VDDIO	I/O
19	SDIO_DATA1	SDIO Data Line 1	VDDIO	I/O
20	GND	Ground.		GND
21	VIN_LDO_OUT	Internal Buck voltage generation pin	1.12V(typ)	VCC

22	VDDIO	1.8V VDDIO supply for WLAN and BT	VDDIO	VCC
23	VIN_LDO	Internal Buck voltage generation pin	1.12V(typ)	VCC
24	SUSCLK_IN	External 32.768K or RTC clock		I
25	TDM2_DO/BT_PCM_OUT	TDM2_DO/PCM data Out	VDDIO	O
26	TDM2_SCK/BT_PCM_CLK	TDM2_SCK/PCM Clock	VDDIO	I/O
27	TDM2_DI/BT_PCM_IN	TDM2_DI/PCM data Input	VDDIO	I
28	TDM2_WS/BT_PCM_SYNC	TDM2_WS/PCM Synchronization control	VDDIO	I/O
29	NC	Floating Pin, No connect to anything.		Floating
30	NC	Floating Pin, No connect to anything.		Floating
31	GND	Ground.		GND
32	TDM2_MCK	TDM2_MCK	VDDIO	I/O
33	GND	Ground.		GND
34	BT_REG_ON	Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when deasserte. This pin has an internal 50 kΩ pull-down resistor that is auto enabled and disabled upon recognizing high on this pin. It can be disabled through programming.	VDDIO	I
35	GPIO_5	GPIO configuration pin	VDDIO	I/O
36	GND	Ground.		GND
37	NC	Floating Pin, No connect to anything.		Floating
38	NC	Floating Pin, No connect to anything.		Floating
39	RFSW_CTRL_04_ANT_Diversity	Programmable RF switch control lines.	VDDIO	I/O
40	NC	Floating Pin, No connect to anything.		Floating
41	BT_UART_RTS_N	High-Speed UART RTS	VDDIO	O
42	BT_UART_TXD	High-Speed UART Data Out	VDDIO	O
43	BT_UART_RXD	High-Speed UART Data In	VDDIO	I
44	BT_UART_CTS_N	High-Speed UART CTS	VDDIO	I

45	BT_GPIO_2	Bluetooth GPIO configuration pin	VDDIO	I/O
46	BT_GPIO_3	Bluetooth GPIO configuration pin	VDDIO	I/O
47	BT_GPIO_4	Bluetooth GPIO configuration pin	VDDIO	I/O
48	GND	Ground.		GND
49	GND	Ground.		GND
50	GND	Ground.		GND
51	GND	Ground.		GND
52	TDM1_DO	TDM2 interface Data Out	VDDIO	
53	LHL_GPIO_3	Miscellaneous GPIO configuration pin	VDDIO	I/O
54	LHL_GPIO_2	Miscellaneous GPIO configuration pin	VDDIO	I/O
55	TDM1_SCK	TDM1 interface Slave Clock	VDDIO	
56	TDM1_WS	TDM1 interface WordSelec	VDDIO	
57	TDM1_MCK	TDM1 interface Master Clock	VDDIO	
58	TDM1_DI	TDM1 interface Data In	VDDIO	
59	GND	Ground.		GND
60	GND	Ground.		GND
61	GND	Ground.		GND
62	GND	Ground.		GND
63	GND	Ground.		GND

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply voltage for VBAT.	-0.5	-	+6[5]	V
VDDIO	DC supply voltage for VDDIO.	-0.5	-	+2.2	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply voltage for VBAT.	3.13[6]	3.3	3.6	V
VDDIO	DC supply voltage for VDDIO.	1.71	1.8	1.89	V

3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDDIO=1.8V					
V_{IH}	Input high voltage (V_{DDIO})	0.65 × VDDIO	-		V
V_{IL}	Input low voltage (V_{DDIO})	-	-	0.35 × VDDIO	V
V_{OH}	Output High Voltage @ 2mA	VDDIO – 0.40	-	-	V
V_{OL}	Output Low Voltage @ 2mA	-	-	0.45	V

[5] The maximum continuous voltage is 5.25 V. Voltage transients up to 6.0 V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed.

[6] AW-XM650 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.13V < VBAT < 3.5V.

3.4 Power Up Timing Sequence

The AW-XM606 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

Description of Control Signals (Power-Up/Power-Down/Reset Control Signals)

Signal	Description
WL_REG_ON	Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal AW-XM606 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. This pin has an internal 50 kΩ pull-down resistor that is enabled by default and disabled upon recognizing high on this pin.
BT_REG_ON	Used by the PMU to power up the BT section. It is also OR-gated with the WL_REG_ON input to control the internal AW-XM606 regulators. When this pin is high, the regulators are enabled and the BT section is out of reset. When this pin is low the BT section is in reset. This pin has an internal 50 kΩ pull-down resistor that is enabled by default and disabled upon recognizing high on this pin.

Control Signal Timing Diagrams

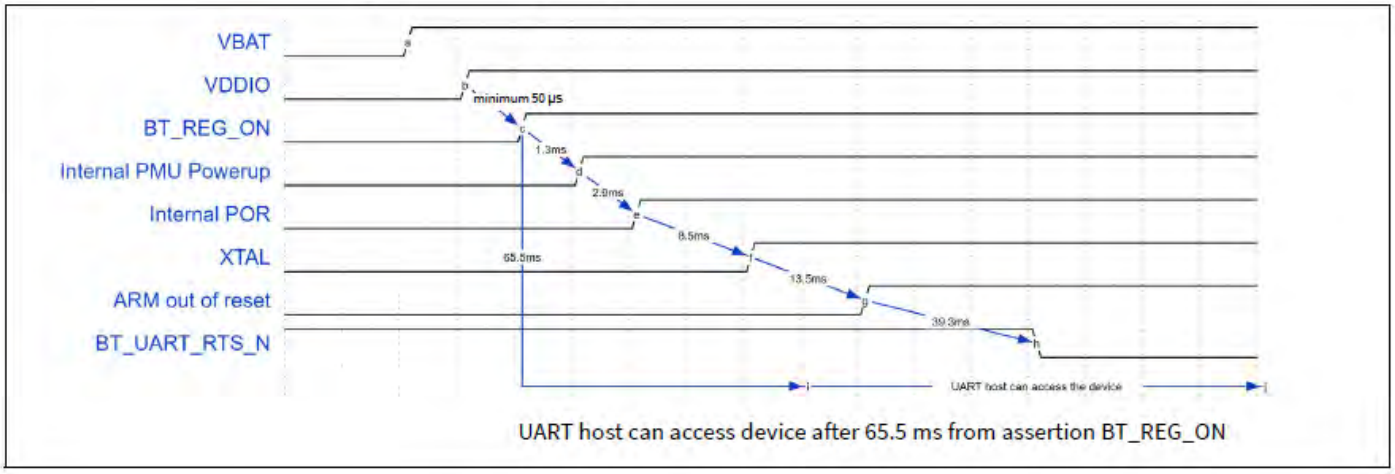


Figure 1 Bluetooth® subsystem boot-up sequence

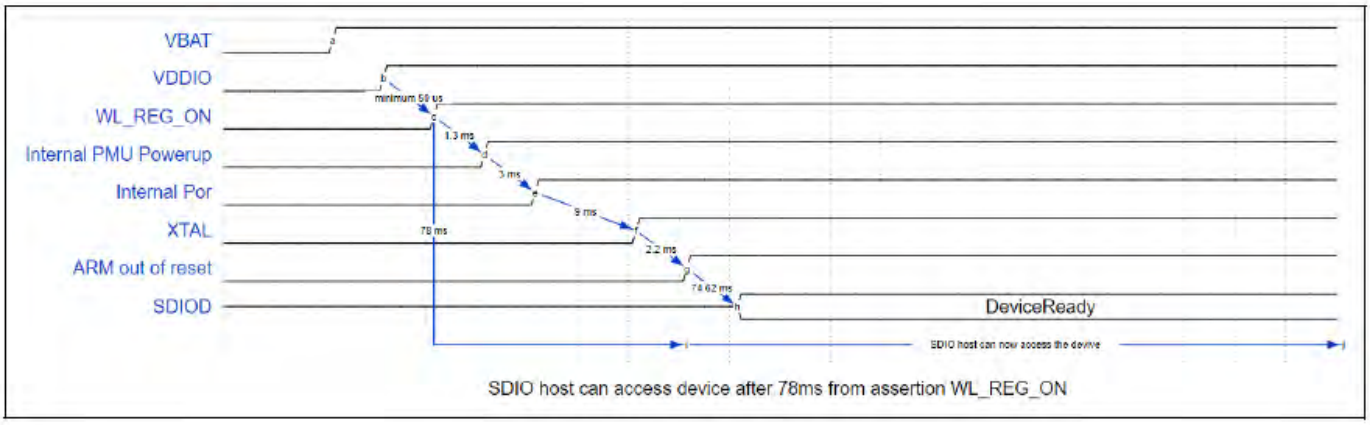


Figure 2 WLAN boot-up sequence for SDIO

3.5 SDIO Timing

3.5.1 SDIO default mode timing

SDIO default mode timing is shown by the combination of Figure 1 and Table 1.

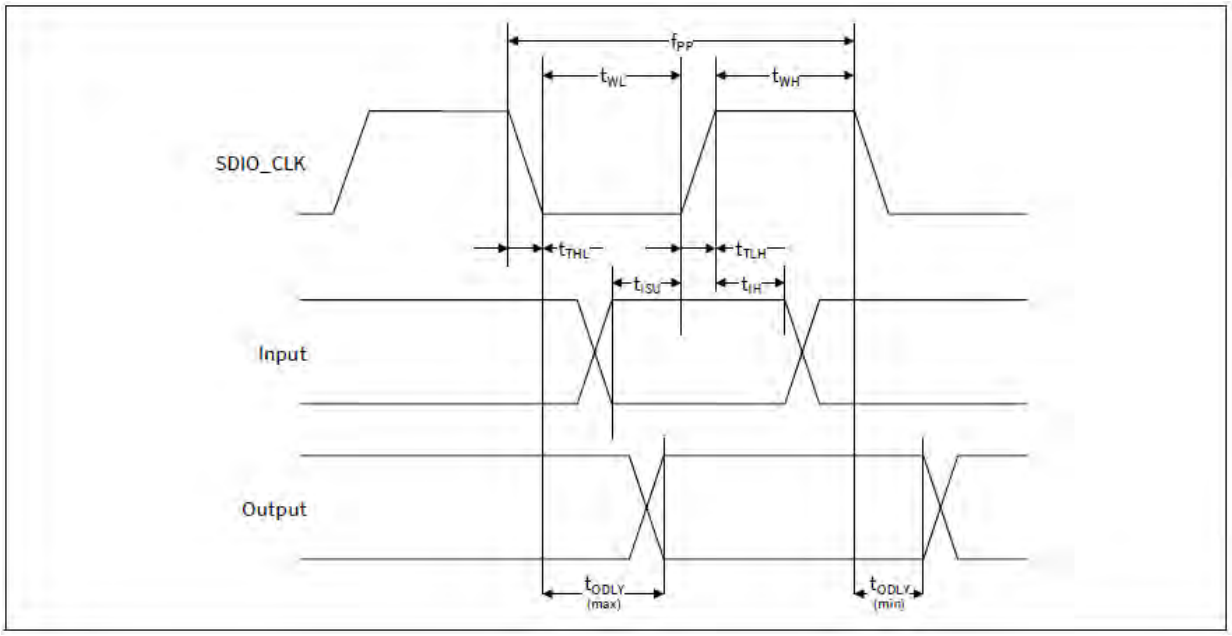


Figure 1 SDIO bus timing (Default mode)

Table 1 SDIO bus timing[7] parameters (Default mode)

Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[87])					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

87.Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

[7] Timing is based on CL ≦ 40 pF load on CMD and data.

3.5.2 SDIO high-speed mode timing

SDIO high-speed mode timing is shown by the combination of Figure 2 and Table 2.

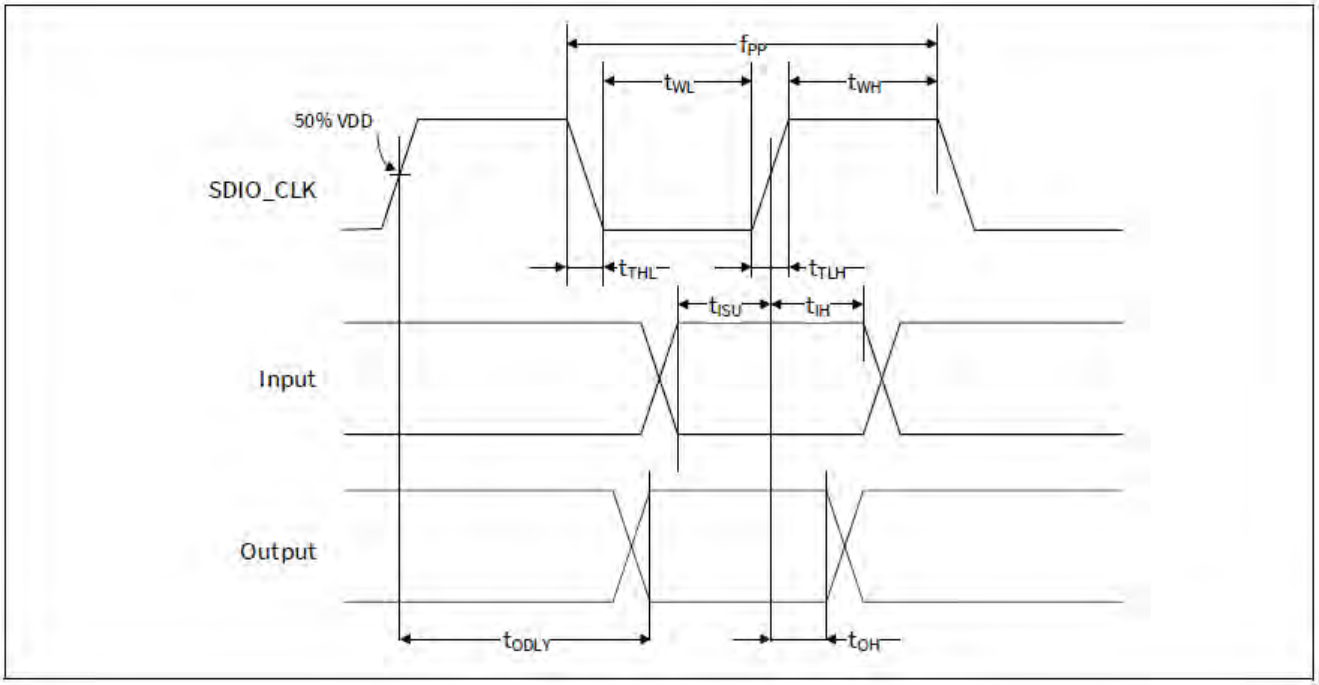


Figure 2 SDIO bus timing (high-speed mode)

Table 2 SDIO bus timing[8] parameters (Default mode)

Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[89]					
Frequency – Data Transfer mode	f_{PP}	0	–	50	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

89.Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

[8] Timing is based on CL ≦ 40 pF load on CMD and data.

3.5.2 SDIO bus timing specifications in SDR modes

3.5.2.1 Clock timing

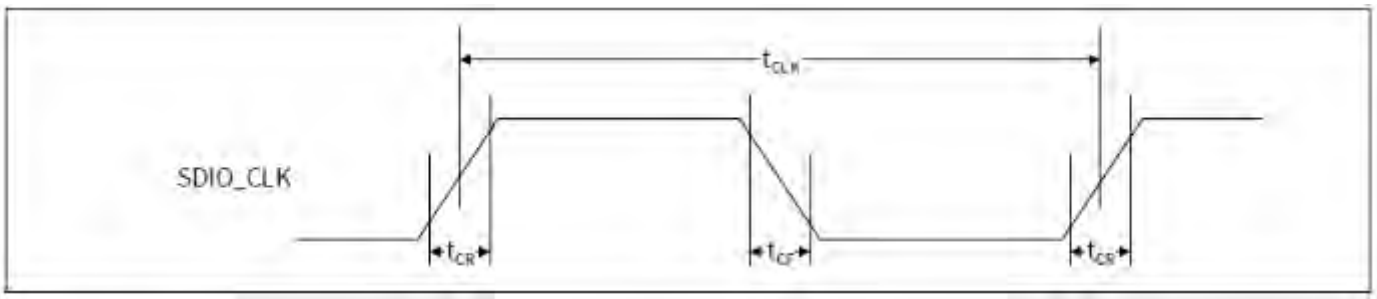


Figure 3 SDIO clock timing (SDR modes)

Table 3 SDIO bus clock timing parameters (SDR modes)

Parameter	Symbol	Min	Max	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		12.5	–	ns	SDR50 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) at 100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) at 208 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	30	70	%	–

3.5.2.2 Device input timing

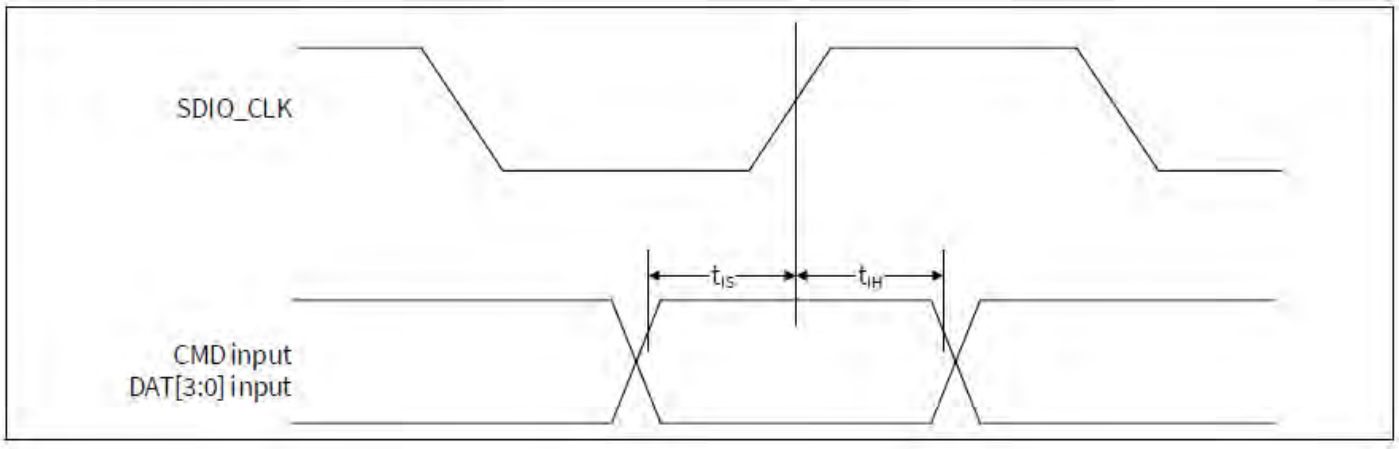


Figure 4 SDIO bus input timing (SDR modes)

Table 4 SDIO bus input timing parameters (SDR modes)

Symbol	Min	Max	Unit	Comments
SDR50 mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975 V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975 V

3.5.2.3 Device output timing

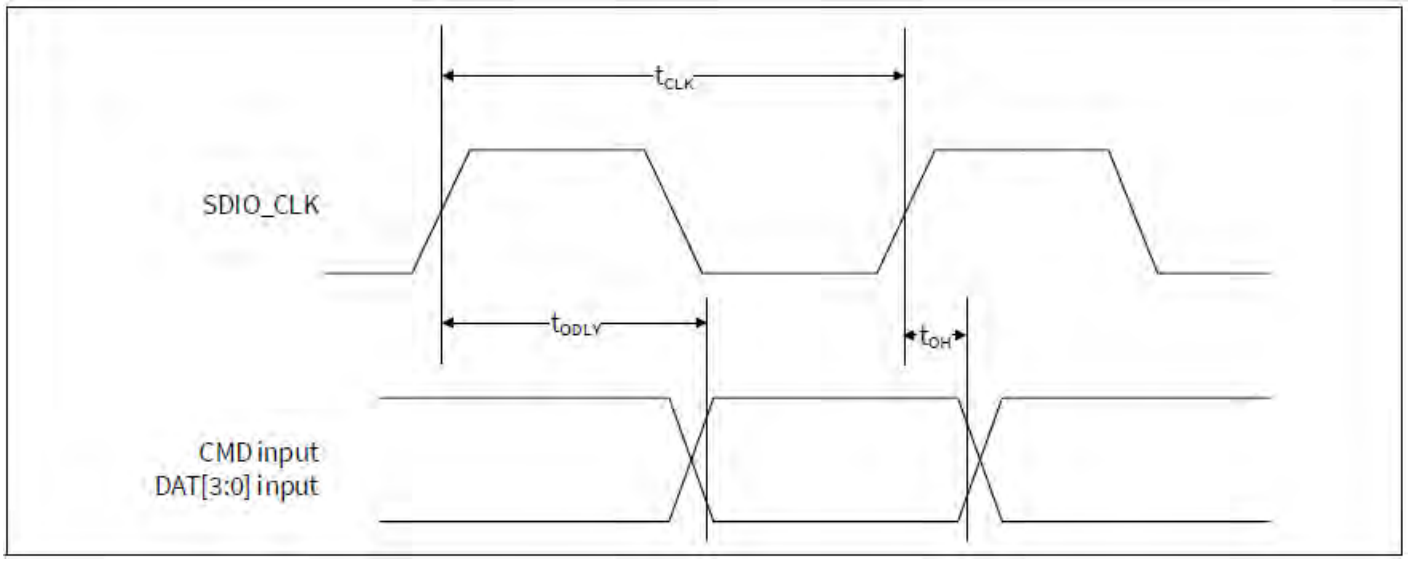


Figure 5 SDIO bus output timing (SDR modes)

Table 5 SDIO bus output timing parameters (SDR modes up to 80 MHz)

Symbol	Min	Max	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns C_L = 30 pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns C_L = 40 pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) C_L = 15 pF

3.5.2.4 SDIO bus timing specifications in DDR50 mode

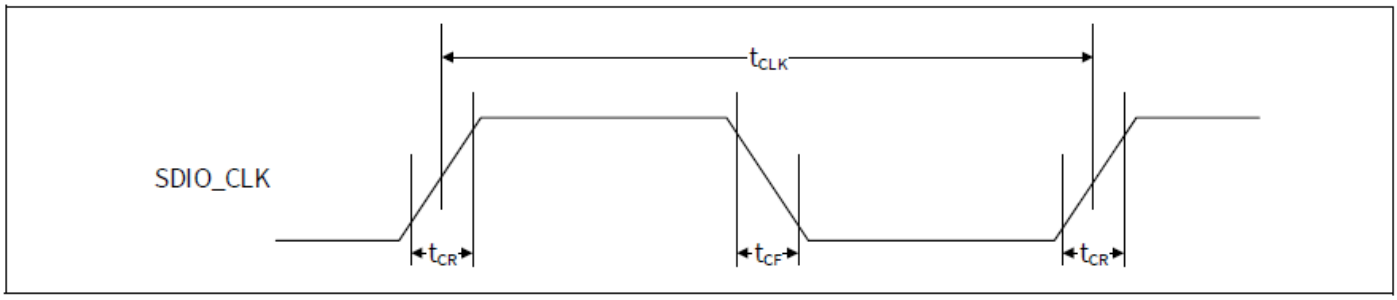


Figure 6 SDIO clock timing (DDR50 mode)

Table 6 SDIO bus clock timing parameters (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Comments
–	t_{CLK}	25	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 4.00 ns (max) at 50 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	45	55	%	–

3.5.2.5 Data timing

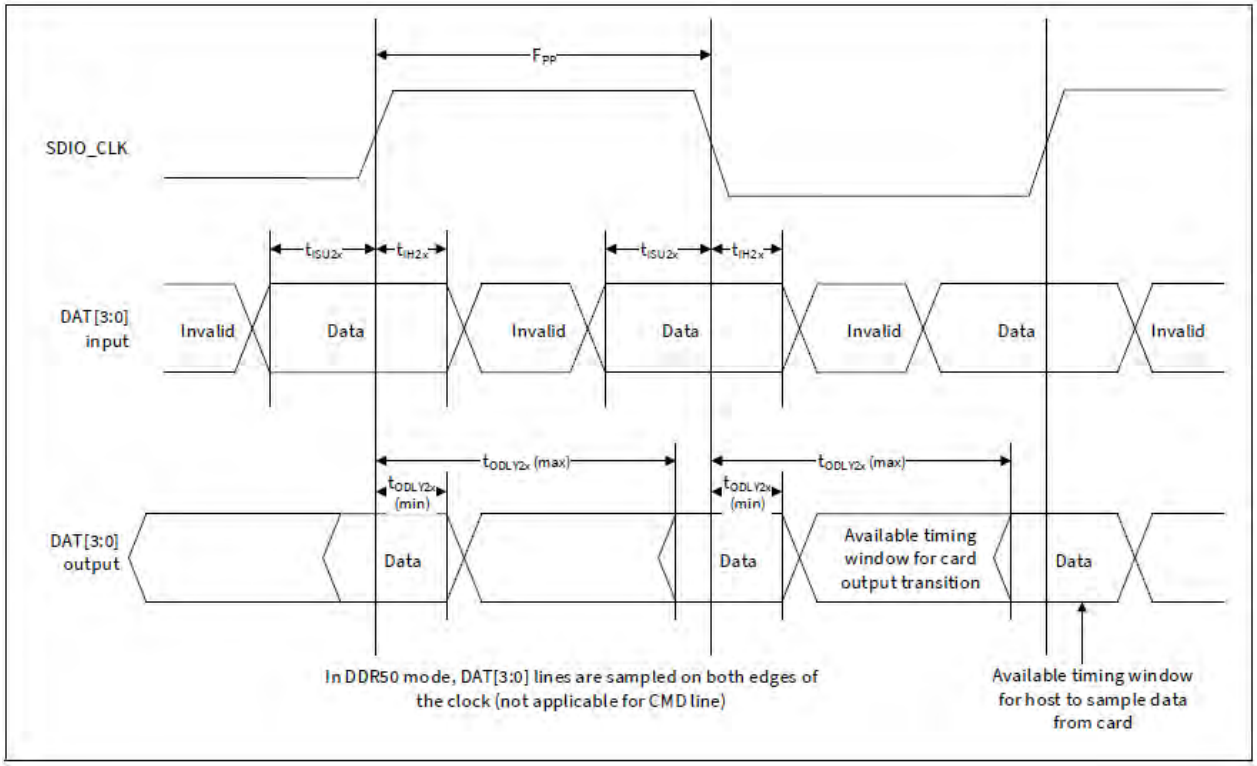


Figure 7 SDIO data timing (DDR50 mode)

Table 7 SDIO bus timing parameters (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30 pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	C_{CARD} < 25 pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)

3.6 Power Consumption[9]

3.6.1 WLAN

No.	Item			VBAT_IN=3.3 V	
				Max.	Avg.
1	Pdn *(1) (2) (5)			TBD	TBD
2	Deep Sleep *(2) (3) (5) (7) (Not associated with AP)			TBD	TBD
3	Power Save DTIM 1 (2.4GHz)*(2) (4) (7)			TBD	TBD
4	Power Save DTIM 1 (5GHz) *(2) (4) (7)			TBD	TBD
5	Power Save DTIM 1 (6GHz) *(2) (4) (6) (7)			TBD	TBD
Band (GHz)	**Mode**	**BW (MHz)**	**RF Power (dBm)**	**Transmit*(7)**	
				Max.	**Avg.**
2.4	11b@1Mbps	20	19	271	266
	11g@54Mbps	20	18	304	252
	11n@MCS7	20	17	281	233
	11ax@MCS0 NSS1	20	15	259	215
	11ax@MCS11 NSS1	20	15	235	210
5	11a@6Mbps	20	16.5	333	325
	11n@MCS7	20	15	329	302

[9] For Details, please contact Azurewave FAE

	11ac@MCS0 NSS1	20	14	305	279
	11ac@MCS8 NSS1	20	14	330	274
	11ax@MCS0 NSS1	20	13	274	270
	11ax@MCS11 NSS1	20	13	312	261
6	11ax@MCS0 NSS1	20	10	225	224
	11ax@MCS11 NSS1	20	10	261	219

Band (GHz)	Mode	BW(MHz)	Receive*(7)	
			Max.	Avg.
2.4	11b@11Mbps	20	35.2	31.8
	11g@54Mbps	20	37.1	33.1
	11n@MCS7	20	35.9	33.4
	11ax@MCS11 NSS1	20	41.7	32.8
5	11a@54Mbps	20	44.3	41.8
	11n@MCS7	20	43.7	41.7
	11ac@MCS8 NSS1	20	43.9	40.9
	11ax@MCS11 NSS1	20	45.5	42.1
6	11ax@MCS11 NSS1	20	46.5	43.2

***Current Unit: mA**

No.	Item	VDDIO=1.8 V	
		Max.	Avg.
1	Pdn *(1)(2)(5)	TBD	TBD
2	Deep Sleep *(2)(3)(5)(7) (Not associated with AP)	TBD	TBD
3	Power Save DTIM 1 (2.4GHz)*(2)(4)(7)	TBD	TBD
4	Power Save DTIM 1 (5GHz) *(2)(4)(7)	TBD	TBD
5	Power Save DTIM 1 (6GHz) *(2)(4)(6)(7)	TBD	TBD

Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit*(7)	
				Max.	Avg.
2.4	11b@11Mbps	20	19	4.77	4.65
	11ax@MCS11 NSS1	20	15	4.78	4.61
5	11a@54Mbps	20	16.5	4.77	4.58
	11ax@MCS11 NSS1	20	13	4.81	4.60
6	11ax@MCS11 NSS1	20	10	4.73	4.56

Band (GHz)	Mode	BW(MHz)	Receive*(7)	
			Max.	Avg.
2.4	11b@11Mbps	20	0.9	0.7
5	11ax@MCS11 NSS1	20	0.9	0.7
6	11ax@MCS11 NSS1	20	0.9	0.7

***Current Unit: mA**

3.6.2 Bluetooth

Mode	Packet Type	RF Power (dBm)	VBAT_IN=3.3 V	
			Max.	Avg.
Sleep*(1)	N/A	N/A	TBD	TBD
Transmit*(2) (3)	DH5/3-DH5	6.5	35.2	28.6
Receive*(2) (3)	DH5/3-DH5	N/A	23.1	19.9

***Current Unit: mA**

Mode	Packet Type	RF Power (dBm)	VDDIO=1.8 V	
			Max.	Avg.
Sleep*(1)	N/A	N/A	TBD	TBD
Transmit*(2) (3)	DH5/3-DH5	6.5	361	338
Receive*(2) (3)	DH5/3-DH5	N/A	354	333

***Current Unit: uA**

3.7 Frequency Reference

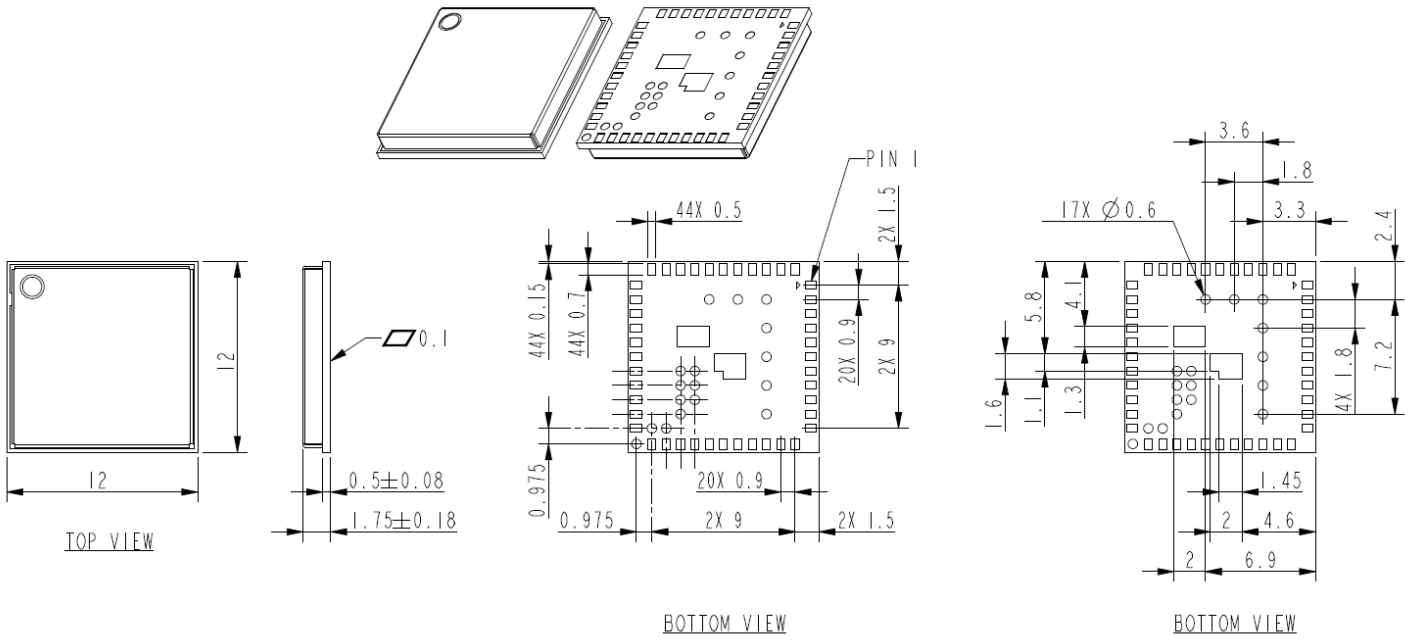
The AW-XM606 requires an external low-frequency clock for low-power mode timing. An external 32.768 kHz precision oscillator which meets the requirements listed in below table must be used.

Parameter	LPO Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	Ppm
Duty cycle	30–70	%
Input signal amplitude	200–1800 mV,	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance[10]	> 100k	Ω
	< 5	pF
Clock jitter (during initial startup)	< 10,000	Ppm

[10] When power is applied or switched off.

4. Mechanical Information

4.1 Mechanical Drawing



TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

5. Packaging Information

TBD

FCC:

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE:

This module is intended for OEM integrator. This module is only FCC authorized for the specific rule parts listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.
Additional testing and certification may be necessary when multiple modules are used.
OEM integrators that they must use the equivalent antennas or C2PC will be required.

This equipment complies with FCC mobile radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

The host manufacturer should reference KDB Publication 996369 D04 Module Integration Guide.

USERS MANUAL OF THE END PRODUCT:

In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:
The final end product must be labeled in a visible area with the following " Contains TX FCC ID: TLZ-XM606".

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

Ant list
The antenna is limited as the antenna listed.

Ant.	Brand	Model Name	Antenna Type	Connector	Gain (dBi)
1	ARISTOTLE	RFA-27-JP326MHF4C198	PIFA Antenna	I-PEX	Note1
2	ARISTOTLE	RFA-27-JP326-C198	PIFA Antenna	I-PEX	Note1

Note1:

Ant.	Gain (dBi)	
	WLAN 2.4GHz/Bluetooth	WLAN 5GHz/6GHz
1	3.5	5
2	3.5	5

This device is restricted for indoor use.
The antenna is limited as the antenna listed.

Operation of transmitters in the 5.925-7.125 GHz band is prohibited for control of or Communications with unmanned aircraft systems.

Additional testing and certification is necessary when the lowest gain in WLAN operation 6GHz of antennas which may be used in the future that is less than the lowest gain of the original certified for Contention Based Protocol (CBP).

Make sure that the antenna used for host device must be an integral antenna, per the rules governing U-NII Band 4 operation.

AW-XM606

IEEE 802.11a/b/g/n/ac/ax Wi-Fi with Bluetooth

Combo LGA Module

Layout Guide

Rev. A

(For Standard)

Revision History

Version	Revision Date	Description	Initials	Approved
01	2024/05/17	● Initial Version	QM.Tan	N.C. Chen

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1 Overview

1.1 Device supported

This document provides key guidelines and recommendations to be followed when creating AW-XM606 (12 x 12 mm LGA Module) layout. It is strongly recommended that layouts be reviewed by the AzureWave engineering team before being released for fabrication.
The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

2 GENERAL RF GUIDELINES

Follow these steps for optimal WLAN performance.

1. Control WLAN 50 ohm RF traces by doing the following:
   - Route traces on the top layer as much as possible and use a continuous reference ground plane underneath them.
   - Verify trace distance from ground flooding. At a minimum, there should be a gap equal to the width of one trace between the trace and ground flooding. Also keep RF signal lines away from metal shields. This will ensure that the shield does not detune the signals or allow for spurious signals to be coupled in.
   - Keep all trace routing inside the ground plane area by at least the width of a trace.
   - Check for RF trace stubs, particularly when bypassing a circuit.

2. Keep RF traces properly isolated by doing the following:
   - Do not route any digital or analog signal traces between the RF traces and the reference ground.
   - Keep the balls and traces associated with RF inputs away from RF outputs. If two RF traces are close each other, then make sure there is enough room between them to provide isolation with ground fill.
   - Verify that there are plenty of ground vias in the shield attachment area. Also verify that there are no non-ground vias in the shield attachment area. Avoid traces crossing into the shield area on the shield layer.

3. Consider the following RF design practices:
   - Confirm antenna ground keep-outs.
   - Verify that the RF path is short, smooth, and neat. Use curved traces or microwave corners for all turns; never use 90-degree turns. Avoid width discontinuities over pads. If trace widths differ significantly from component pad widths, then the width change should be mitered. Verify there are no stubs.
   - Do not use thermals on RF traces because of their high loss.
   - The RF traces between AW-XM606 WL_BT_ANT pin and antenna must be made using 50Ω controlled-impedance transmission line.

3 Ground Layout

Please follow general ground layout guidelines. Here are some general rules for customers' reference.

• The layer 2 of PCB should be a complete ground plane. The rule has to be obeyed strictly in the RF section while RF traces are on the top layer.

• Each ground pad of components on top layer should have via drilled to PCB layer 2 and via should be as close to pad as possible. A bulk decoupling capacitor needs two or more.

• Don't place ground plane and route signal trace below printed antenna or chip antenna to avoid destroying its electromagnetic field, and there is no organic coating on printed antenna. Check antenna chip vendor for the layout guideline and clearance.

• Move GND vias close to the pads.

4 Power Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

• A 4.7uF capacitor is used to decouple high frequency noise at digital and RF power terminals. This capacitor should be placed as close to power terminals as possible.

• In order to reduce PCB's parasitic effects, placing more via on ground plane is better.

5 Digital Interface

Please follow power and ground layout guidelines. Here are some general rules for customers' reference.

• The digital interface to the module must be routed using good engineering practices to minimize coupling to power planes and other digital signals.

• The digital interface must be isolated from RF trace.

6 RF Trace

The RF trace is the critical to route. Here are some general rules for customers' reference.

• The RF trace impedance should be 50Ω between ANT port and antenna matching network.

•The length of the RF trace should be minimized.

•To reduce the signal loss, RF trace should laid on the top of PCB and avoid any via on it.

•The CPW (coplanar waveguide) design and the microstrip line are both recommended; the customers can choose either one depending on the PCB stack of their products.

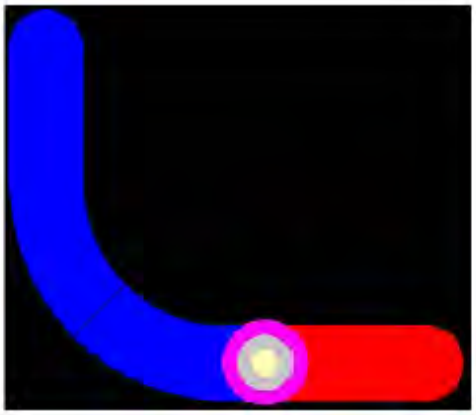
•The RF trace must be isolated with aground beneath it. Other signal traces should be isolated from the RF trace either by ground plane or ground vias to avoid coupling.

•To minimize the parasitic capacitance related to the corner of the RF trace, the right angle corner is not recommended.

If the customers have any problem in calculation of trace impedance, please contact AzureWave.

Correct RF trace

Right-angled corner



Via on RF trace

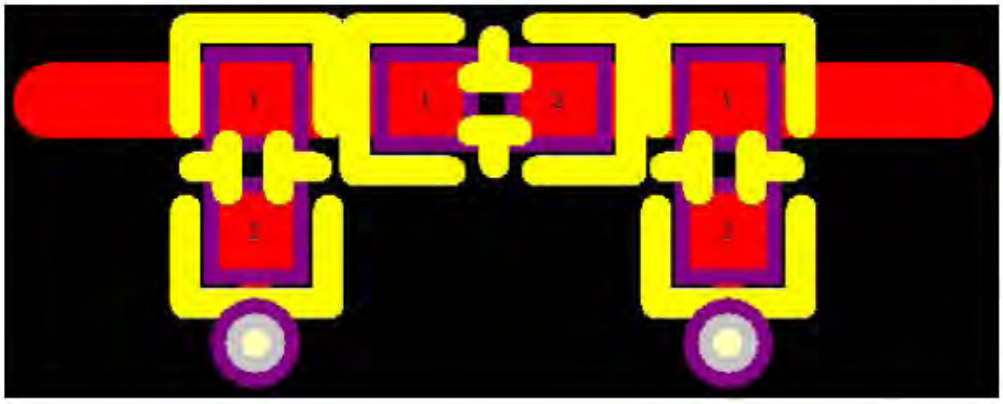
Incorrect RF trace

7 Antenna

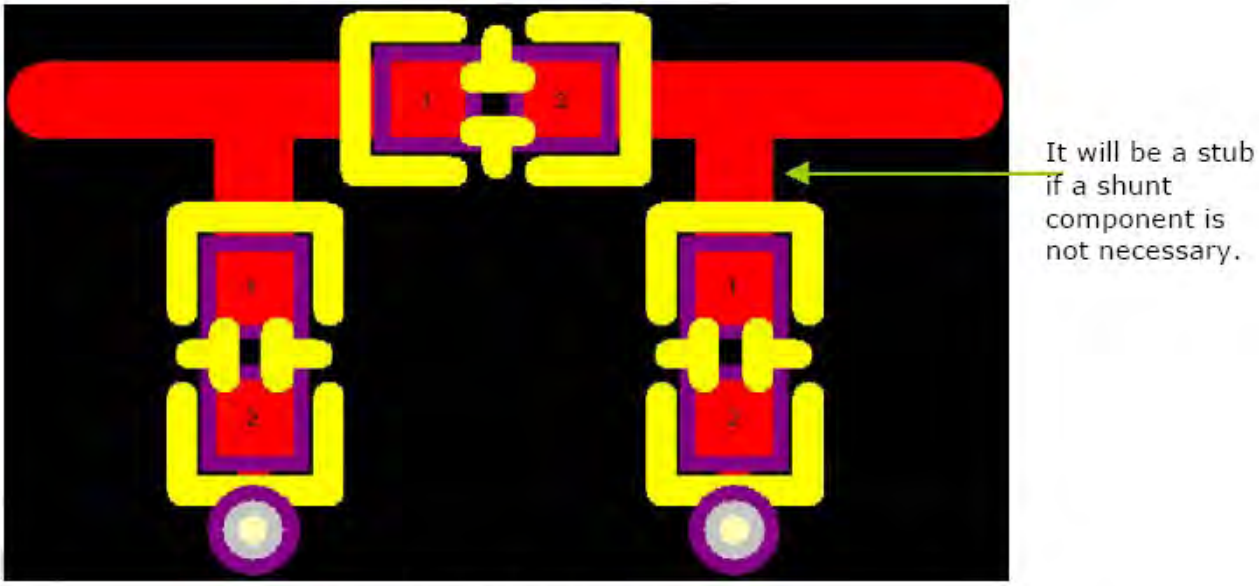
All the high-speed traces should be moved far away from the antenna. For the best radiation performance, check antenna chip vendor for the layout guideline and clearance.

8 Antenna Matching

PCB designer should reserve an antenna matching network for post tuning to ensure the antenna performance in different environments. Matching components should be close to each other. Stubs should also be avoided to reduce parasitic while no shunt component is necessary after tuning.



Correct layout for antenna matching



Incorrent layut for antenna matching

9 Shielding Case

Magnetic shielding, ferrite drum shielding, or magnetic-resin coated shielding is highly recommended to prevent EMI issues.

10 GENERAL LAYOUT GUIDELINES

Follow these guidelines to obtain good signal integrity and avoid EMI:

1. Place components and route signals using the following design practices:
   - Keep analog and digital circuits in separate areas.
   - Identify all high-bandwidth signals and their return paths. Treat all critical signals as current loops. Check each critical loop area before the board is built. A small loop area is more important than short trace lengths.
   - Orient adjacent-layer traces so that they are perpendicular to one another to reduce crosstalk.
   - Keep critical traces on internal layers, where possible, to reduce emissions and improve immunity to external noise.
     However, RF traces should be routed on outside layers to avoid the use of vias on these traces.
   - Keep all trace lengths to a practical minimum. Keep traces, especially RF traces, straight wherever possible. Where turns are necessary, use curved traces or two 45-degree turns. Never use 90-degree turns.
2. Consider the following with respect to ground and power supply planes:
   - Route all supply voltages to minimize capacitive coupling to other supplies. Capacitive coupling can occur if supply traces on adjacent layers overlap. Supplies should be separated from each other in the stack-up by a ground plane, or they should be coplanar (routed on different areas of the same layer).
   - Provide an effective ground plane. Keep ground impedance as low as possible. Provide as much ground plane as possible and avoid discontinuities. Use as many ground vias as possible to connect all ground layers together.
   - Maximize the width of power traces. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.
3. Consider these power supply decoupling practices:
   - Place decoupling capacitors near target power pins. If possible, keep them on the same side as the IC they decouple to avoid vias that add inductance. If a filter component cannot be directly connected to a given power pin with a very short and fat etch, do not connect it by a copper trace. Instead, make the connection directly to the associated planes using vias.
   - Use appropriate capacitance values for the target circuit, and consider each capacitor's self-resonant frequency.

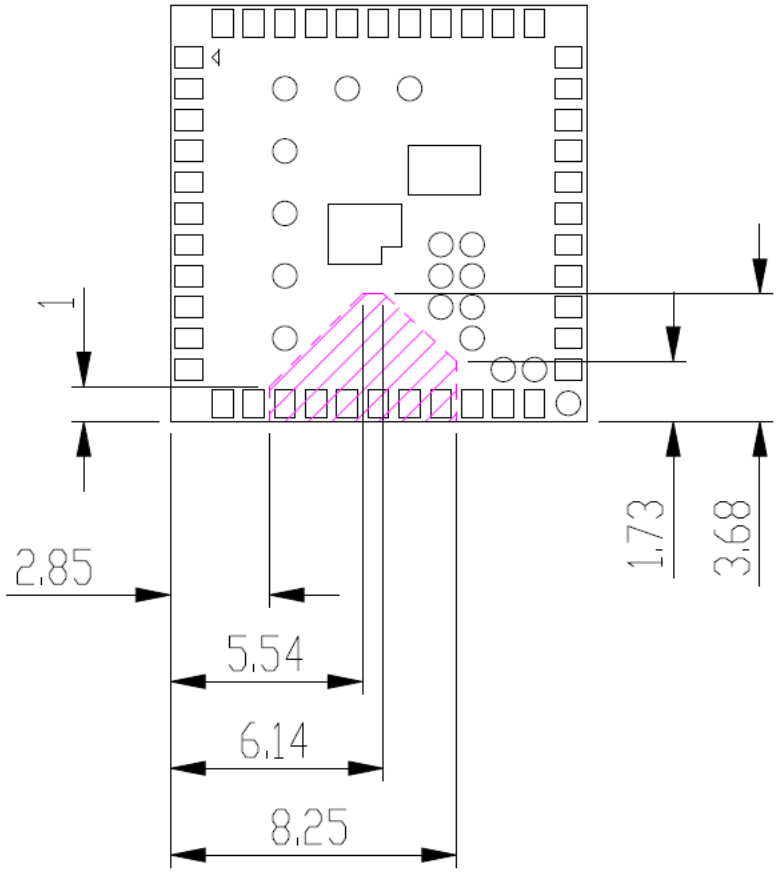
11 The other layout guide Information

• Make sure every power traces have good return path (ground path).
• Connect the input pins of unused internal regulators to ground.
• Leave the output pins of unused internal regulators floating.
• High speed interface (i.e. UART/SDIO/HSIC) shall have equal electrical length. Keep them away from noise sensitive blocks.
• Good power integrity of VDDIO will improve the signal integrity of digital interfaces.
• Good return path and well shielded signal can reduce crosstalk, EMI emission and improve signal integrity.
• RF IO is around 50 ohms, reserve Pi or T matching network to have better signal transition from port to port.
• Smooth RF trace help to reduce insertion loss. Do not use 90 degrees turn (use two 45 degrees turns or one miter bend instead).
• Well arranged ground plane near antenna and antenna itself will help to reduce near field coupling between other RF sources (e.g. GSM/CDMA … antennas).
• Discuss with AzureWave Engineer after you finish schematic and layout job.

12 AW-XM606 layout footprint recommend

12.1 AW-XM606 SDIO Restrict Area

Do not route any trace and keep GND in the restrict area.



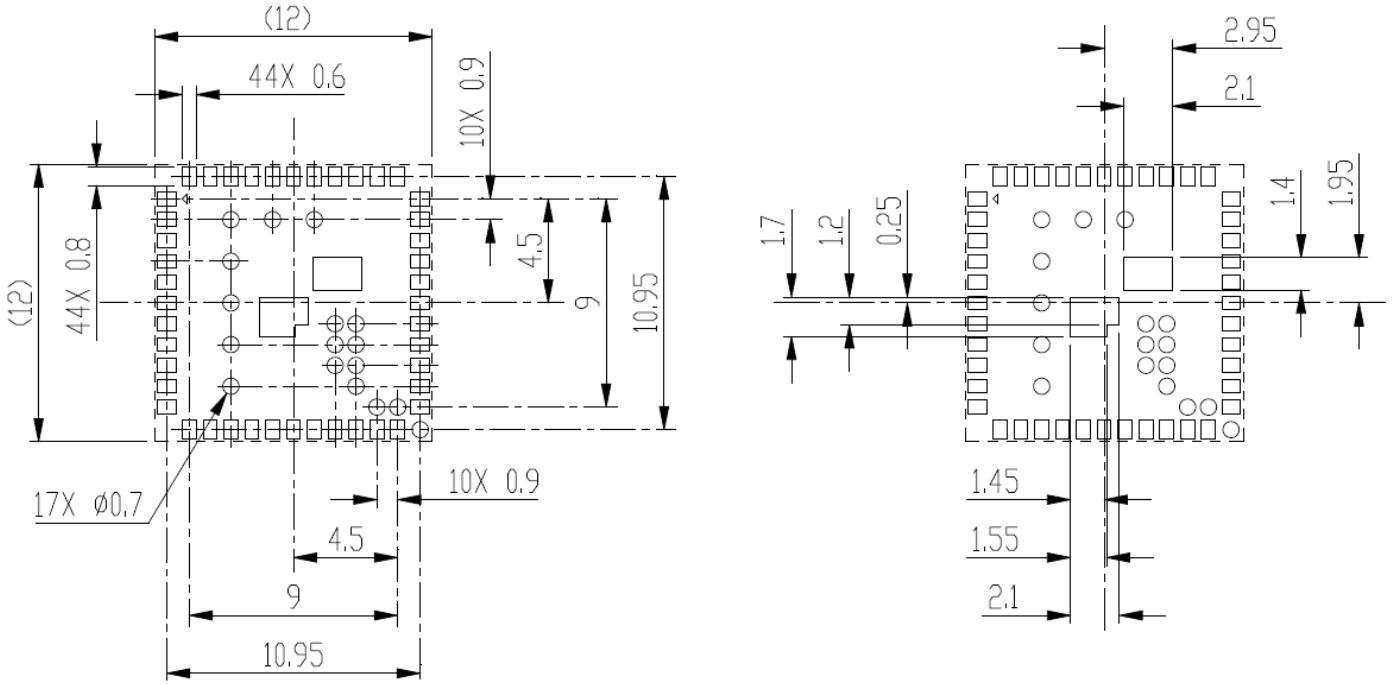
RESTRICT AREA (TOP VIEW)

12.2 AW-XM606 Solder Down stencil and Pad opening Suggestion

- Stencil thickness：0.10~0.12mm
- Function Pad opening size suggestion: Max. 1:1

PS: This opening suggestion just for customer reference, please discuss with AzureWave's Engineer before you start SMT.

Solder Printer Opening and Customer PCB Footprint suggest
Example:



RECOMMENDED PCB LAYOUT (TOP VIEW)