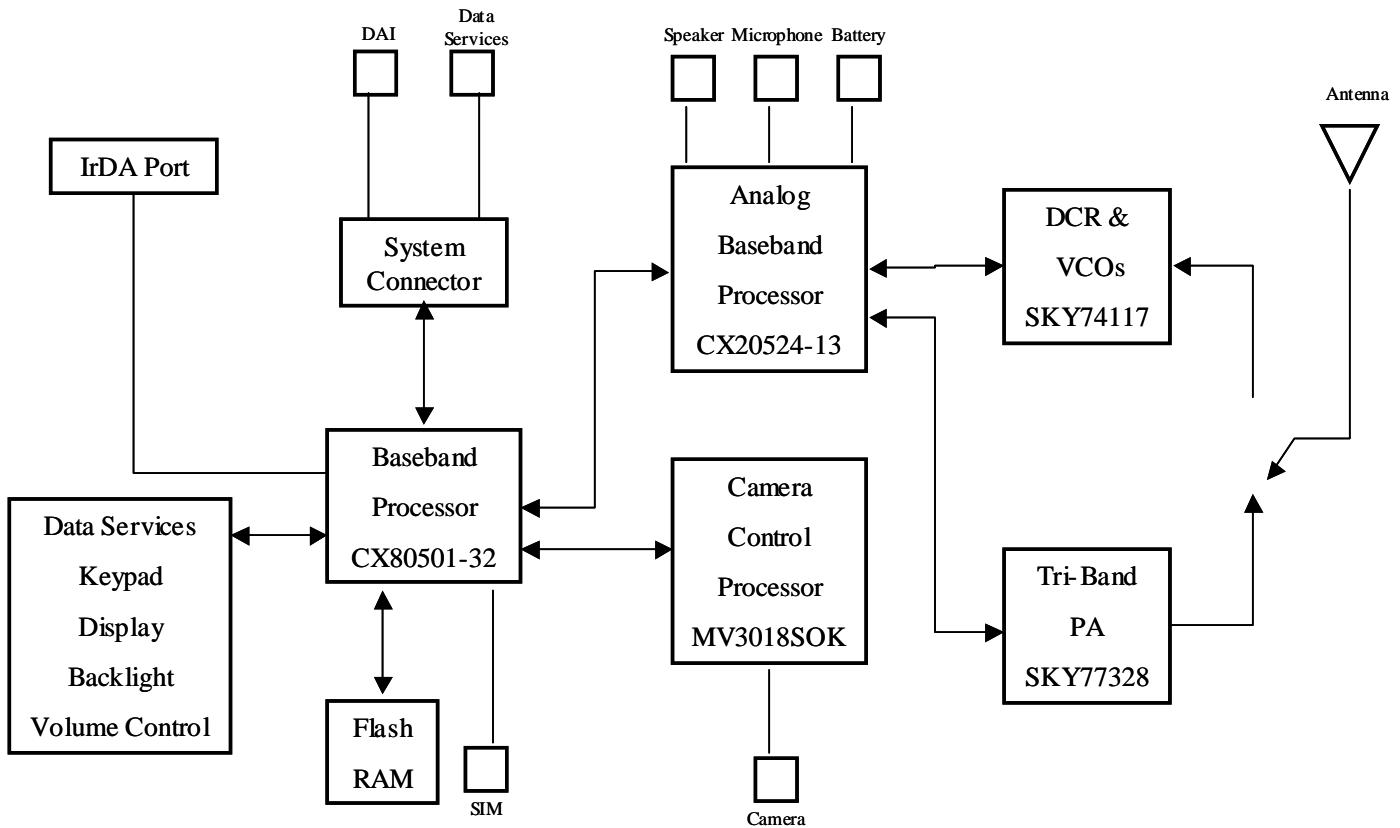


The equipment with brand name GRUNDIG and model name A155 (FCC ID: TKH-A155) is a tri-band GSM phone but only GSM850 and PCS1900 are available in the USA market. The device architecture can be described by the following block diagram:



In the following pages can be found a description of the different functional blocks of this block diagram.

PRODUCT SUMMARY

SKY74117-13: RF Transceiver for Multi-Band GSM, GPRS, and EDGE Applications

Applications

- GSM850, EGSM900, DCS1800, and PCS1900 handsets
- GPRS handsets and modules
- EDGE receive handsets and modules

Features

- Direct down-conversion transceiver eliminates the external image reject/IF filters
- Integrated LDO voltage regulators for direct connection to battery
- Four separate LNAs with single-ended inputs
- Gain selectable in 2 dB steps
- Integrated receive baseband filtering with programmable bandwidth
- Integrated low droop DCOC sequencer
- Integrated IP2 calibration
- Multiplexed and non-multiplexed I/Q input and output lines
- Integrated loop filters
- Integrated quad-band transmit VCOs
- Single integrated, fully programmable fractional-N synthesizer suitable for multi-slot EGPRS operation
- Fully integrated wideband UHF VCO
- Integrated crystal oscillator maintaining amplifier with sinusoidal output buffer
- Digital crystal oscillator center frequency control
- Automatic frequency control possible with fractional-N synthesizer
- Low power standby mode
- Separate enable lines for transmit, receive, and synthesizer
- Band selection possible with the three-wire interface
- Four, fully programmable GPOs to control any antenna switch module
- Low external component count
- Interfaces to low dynamic range receive ADC
- Meets AM suppression requirements without baseband interaction

Description

The SKY74117-13 RF transceiver is a highly integrated device for multi-band Global System for Mobile Communications (GSM), General Packet Radio Service (GPRS), and/or Enhanced Data Rate for GSM Evolution (EDGE) receive applications. The device supports GSM850, EGSM900, DCS1800, and PCS1900 applications.

The receive path implements a direct down-conversion architecture that eliminates the need for Intermediate Frequency (IF) components. The device consists of four integrated Low Noise Amplifiers (LNAs), a quadrature demodulator, selectable receiver baseband filter bandwidths, low droop DC Offset Correction (DCOC) sequencer, and integrated 2nd order Intercept Point (IP2) calibration circuitry.

Similar to its predecessors, Skyworks innovative DCR™ architecture allows for this highly integrated device to be combined with virtually any standard GSM/EGPRS baseband without requiring any special processing interfaces.

The device uses a translation loop transmit architecture. This architecture consists of an In-phase and Quadrature (I/Q) modulator and a frequency translation loop to perform frequency up-conversion with high output spectral purity. The translation loop also contains a phase-frequency detector, charge pump, mixer, programmable dividers, and high power transmit Voltage Controlled Oscillators (VCOs) with no external tank required.

The SKY74117-13 also features an integrated, fully programmable, sigma-delta fractional-N synthesizer suitable for EGPRS multi-slot operation. The reference frequency for the synthesizer is supplied by an integrated Voltage Controlled Crystal Oscillator (VCXO) circuit that enables the use of a low-cost crystal. The VCXO also provides a buffered reference frequency output to supply other devices in the system.

The SKY74117-13 is packaged in a small, 40-pin 6 x 6 mm RF Land Grid Array (RFLGA™) package. A functional block diagram is shown in Figure 1.

NEW



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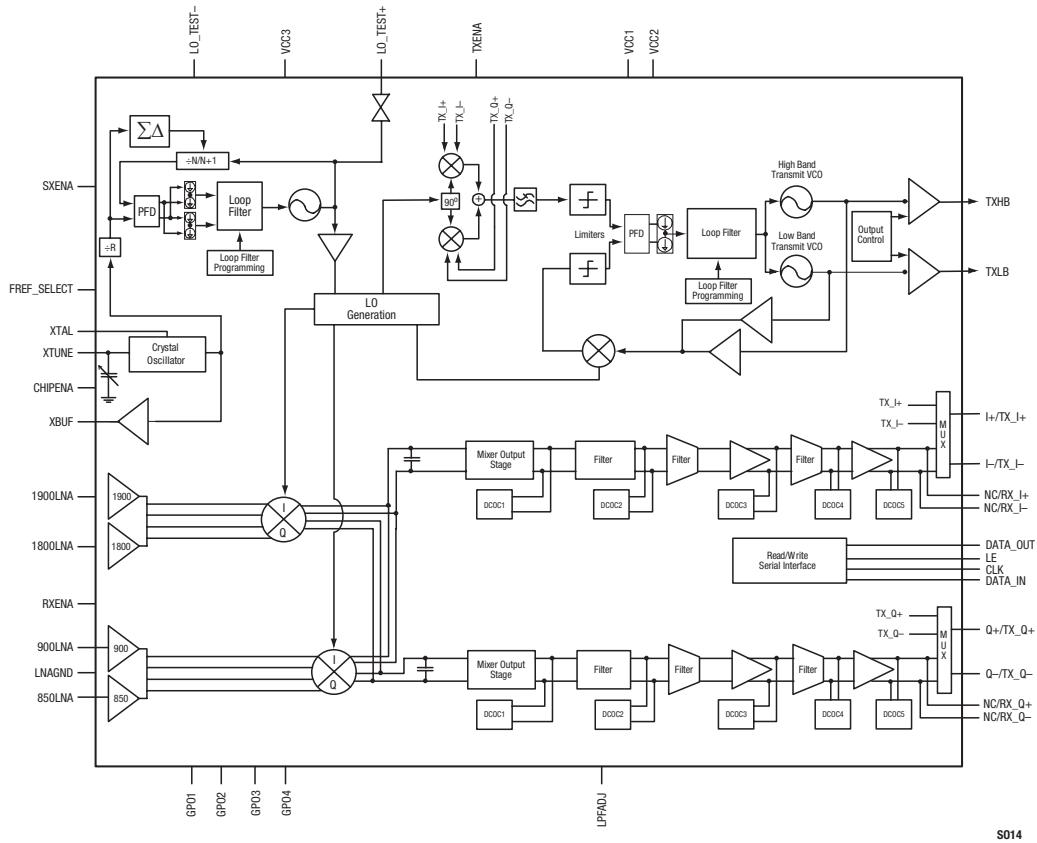


Figure 1. SKY74117-13 RF Transceiver Block Diagram

Ordering Information

Model Name	Manufacturing Part Number	Product Revision
SKY74117 RF Transceiver	SKY74117-13 (Pb-free package)	

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PRODUCT SUMMARY

GPRS RF Subsystem for Integrated Quad-Band GSM, GPRS, and EDGE Handset Applications

Applications

- GSM850, EGSM900, DCS1800, and PCS1900 handsets
- GPRS handsets and modules
- EDGE receive handsets and modules

Features

- Direct down-conversion transceiver eliminates the external image reject/IF filters
- High performance, quad-band PA with current sensing power control
- Integrated PA and switch functions
- High efficiency
- Closed loop iPAC™ or open loop operation with external PA controller
- High linearity transmit/receive switches
- Integrated LDO voltage regulators for direct connection to battery
- Gain selectable in 2 dB steps
- Integrated receive baseband filtering with programmable bandwidth
- Single integrated, fully programmable fractional-N synthesizer suitable for multi-slot EGPRS operation
- Low power standby mode
- Separate enable lines for transmit, receive, and synthesizer
- Four, fully programmable GPOs to control any antenna switch module
- Low external component count

NEW

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Description

Skyworks quad-band integrated subsystem combines a direct conversion transceiver (SKY74117) with an integrated Power Amplifier Control (iPAC™) front-end module (SKY77500). Together, these devices provide a complete, integrated solution with an extremely compact footprint (<250 mm²). The quad-band RF subsystem supports GSM850, EGSM900, DCS1800, and PCS1900 cellular data service applications.

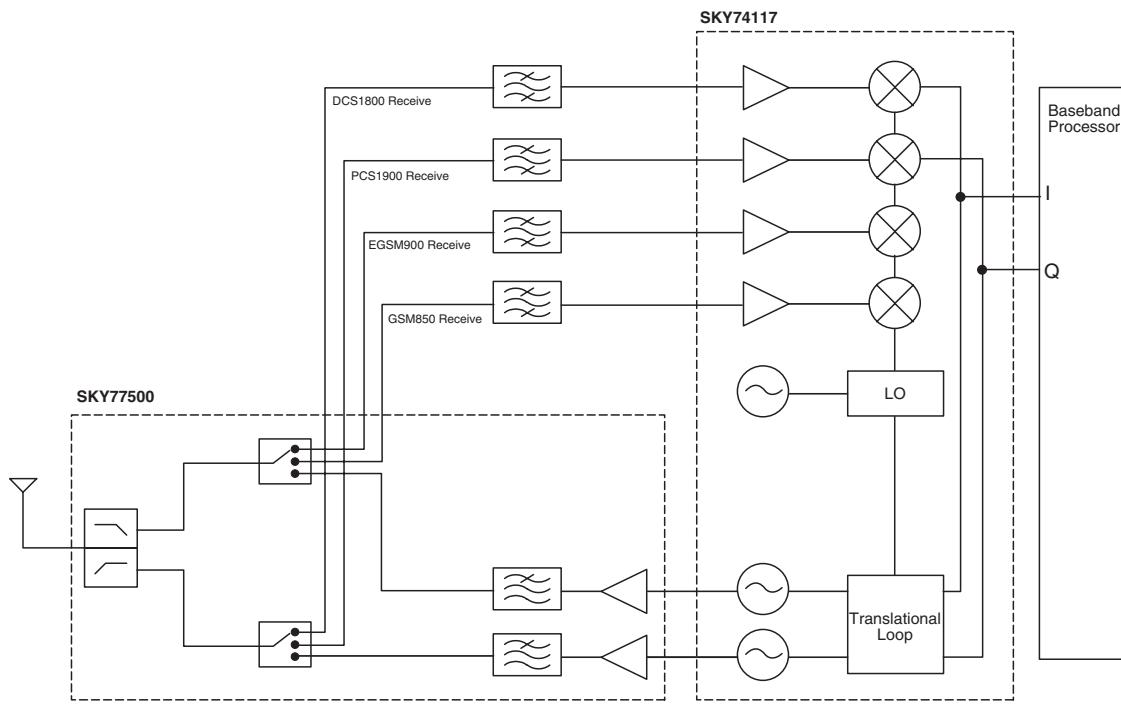
The SKY74117 is based on Skyworks industry-leading, single-chip DCR™ technology. This device consists of a direct conversion transceiver, a transmitter with an integrated Voltage Controlled Oscillator (VCO), and a fully integrated fractional-N synthesizer. The SKY74117 is packaged in a Pb-free 40-pin, 6 x 6 mm RF Land Grid Array (RFLGA™) package.

The SKY77500 incorporates separate GSM850/900 and DCS1800/PCS1900 PA blocks that share a common power supply input for current distribution. Impedance-matching circuitry for 50 Ω input/output and a PA bias control block are also incorporated. Internal decoder circuitry controls the RF switches and provides a low current external control interface. The SKY77500 is packaged in a 32-pin, 8 x 10 mm Multi-Chip Module (MCM) package.

The quad-band RF subsystem can be combined with virtually any standard GSM, GPRS, or EDGE baseband without requiring any special processing interfaces.

The subsystem uses a translation loop transmit architecture to perform frequency up-conversion with high output spectral purity. The sigma-delta, fractional-N synthesizer reference frequency is supplied by an integrated Voltage Controlled Crystal Oscillator (VCXO) circuit that enables the use of a low cost crystal. The subsystem also supports Class 12 EGPRS multi-slot operation.

A block diagram of the quad-band RF subsystem is shown in Figure 1.



S349

Figure 1. GPRS Quad-Band RF Subsystem Functional Block Diagram

Ordering Information

Model Name	Manufacturing Part Number	Product Revision
GPRS Quad-Band RF Subsystem: SKY74117 RF Transceiver SKY77500 iPACT™ PA Front-End Module	SKY74117-13 (Pb-free package) SKY77500-12	

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PRELIMINARY PRODUCT SUMMARY

SKY77328: iPAC™ PAM for Quad-Band GSM / GPRS

Applications

- Quad-band cellular handsets encompassing
 - Class 4 GSM850/900
 - Class 1 DCS1800
 - PCS1900
 - Class 12 GPRS multi-slot operation

Features

- Low input power range
 - 0 to 6 dBm
- High efficiency
 - GSM850 56%
 - GSM900 56%
 - DCS 54%
 - PCS 53%
- BiCMOS PA controller and interface IC
 - Low power control slope
 - Fast response time
 - Improved control accuracy
- Integrated closed loop power amplifier control
- Internal I_{CC} sense resistor for PAC
- Input/Output matching 50 Ω internal (with DC blocking)
- 20-pin package
- Small outline
 - 6 mm x 6 mm
- Low profile
 - 1.2 mm maximum
- Gold plated, lead-free contacts
- MSL3/250 °C

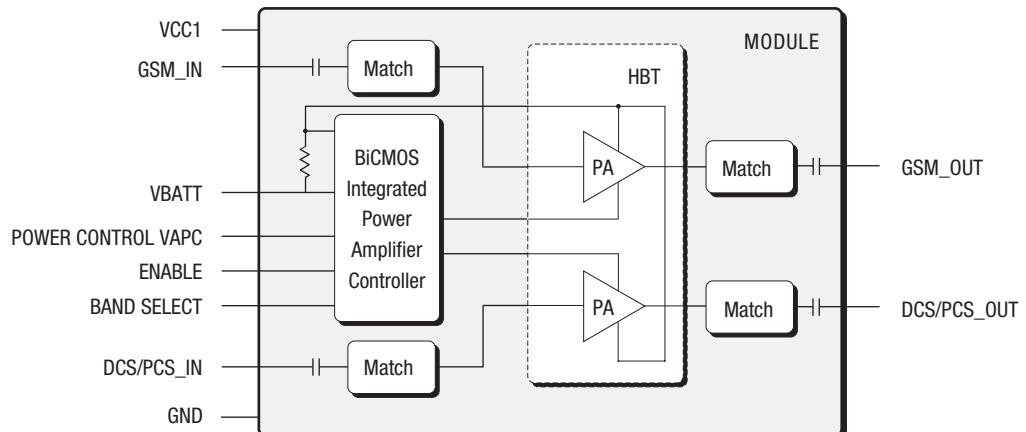
Description

The SKY77328 Power Amplifier Module (PAM) is designed in a low profile (1.2 mm), compact form factor for quad-band cellular handsets comprising GSM850/900, DCS1800, and PCS1900 operation. The PAM also supports Class 12 General Packet Radio Service (GPRS) multi-slot operation.

The module consists of separate GSM850/900 PA and DCS1800/PCS1900 PA blocks, impedance-matching circuitry for 50 Ω input and output impedances, and a Power Amplifier Control (PAC) block with an internal current-sense resistor. The custom BiCMOS integrated circuit provides the internal PAC function and interface circuitry. Fabricated onto a single Gallium Arsenide (GaAs) die, one Heterojunction Bipolar Transistor (HBT) PA block supports the GSM850/900 bands and the other supports the DCS1800 and PCS1900 bands. Both PA blocks share common power supply pins to distribute current. The GaAs die, the Silicon (Si) die, and the passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold.

RF input and output ports of the SKY77328 are internally matched to a 50 Ω load to reduce the number of external components for a quad-band design. Extremely low leakage current (2.5 μA, typical) of the dual PA module maximizes handset standby time. The SKY77328 also contains band-select switching circuitry to select GSM (logic 0) or DCS/PCS (logic 1) as determined from the Band Select (BS) signal. In Figure 1 below, the BS pin selects the PA output (DCS/PCS OUT or GSM850/900 OUT) and the Analog Power Control (VAPC) controls the level of output power.

The VBATT pin connects to an internal current-sense resistor and interfaces to an integrated power amplifier control (iPAC™) function, which is insensitive to variations in temperature, power supply, process, and input power. The ENABLE input allows initial turn-on of PAM circuitry to minimize battery drain.



103216_001

Figure 1. Functional Block Diagram

NEW

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PRODUCT SUMMARY

CX20524 Mixed Signal Device for GSM and GPRS Applications

Applications

- GSM handsets and modules (850/900/1800/1900 MHz)
- GPRS handsets and modules (850/900/1800/1900 MHz)

Features

- Supports multi-slot GPRS up to Class 12
- $\Sigma\Delta$ Analog-to-Digital Converters (ADCs) for digitization of baseband receive signal
- Receive path PGA for AGC of received signal
- GMSK Digital Modulator
- Digital-to-Analog Converters (DACs) for analog conversion of the GMSK modulator output
- Transmit power ramping and power level control
- Low noise voiceband ADC for direct interface to handset and headset microphone
- Low noise voiceband DAC for direct interface to handset and headset speaker
- Auxiliary 8-bit ADC for monitoring system signals
- 3 V/1.8 V SIM card interface
- Temperature sensor
- High speed asynchronous serial ports for interface to Skyworks Baseband Processor device
- Low speed asynchronous serial port for power management functions
- Voltage regulators for both internal (fixed voltage) and system (programmable voltage) needs
- Low power operation
- Control circuit for multi-chemistry advanced battery charger
- Power-On Reset (POR) generation
- Over current-limiting
- Power On/Off control inputs
- CX20524-12: 160-pin FPBGA 12 mm x 12 mm package
- CX20524-13: 180-pin FPBGA 10 mm x 10 mm package

Description

The CX20524 Mixed Signal Device (MSD) is a highly integrated device designed for use in multi-band Global System for Mobile communications (GSM) and General Packet Radio Service (GPRS) handsets. The MSD includes all the power management, voice-band, mixed signal, and radio control functions required in a GSM/GPRS handset and module.

In the receive path, the MSD digitizes the baseband In-Phase/Quadrature (I/Q) inputs. Digital samples are then sent to the Baseband Processor (BP) via the Rx serial interface. The receive path features a programmable gain amplifier (PGA) for Automatic Gain Control (AGC) of the receive signal.

In the transmit path, bursts of digital data are input to the MSD over the control port. A Gaussian Minimum-Shift Keying (GMSK) modulator generates modulated I and Q waveforms from the input data. The I and Q waveforms are converted into analog waveforms and output from the MSD.

The CX20524 generates an analog signal to control the handset Power Amplifier (PA) output level.

The device voiceband Codec section provides an interface to a 32 Ω handset speaker and microphone. Line In/Out signals are also available to interface with audio accessories, such as a headset or car kit.

The MSD is designed to operate directly from a single cell, 3.6 V Li Ion battery with no external regulation required. The MSD integrates all necessary Low Drop Out (LDO) voltage regulators that generate the required device and system power supplies from battery input.

An integrated SIM interface circuit allows direct interface to 3.0 V and 1.8 V SIM cards with no external components.

An integrated battery charger control circuit provides charging capabilities for multi-chemistry batteries.

The CX20524-12 is packaged in a compact, 160-pin (12 mm x 12 mm) Fine Pitch Ball Grid Array (FPBGA), shown in Figure 2.

The CX20524-13 is packaged in a compact, 180 pin 10 mm x 10 mm, 0.5 mm pitch, Fine Pitch Ball Grid Array (FPBGA), shown in Figure 3.

CX20524 Mixed Signal Device Product Summary

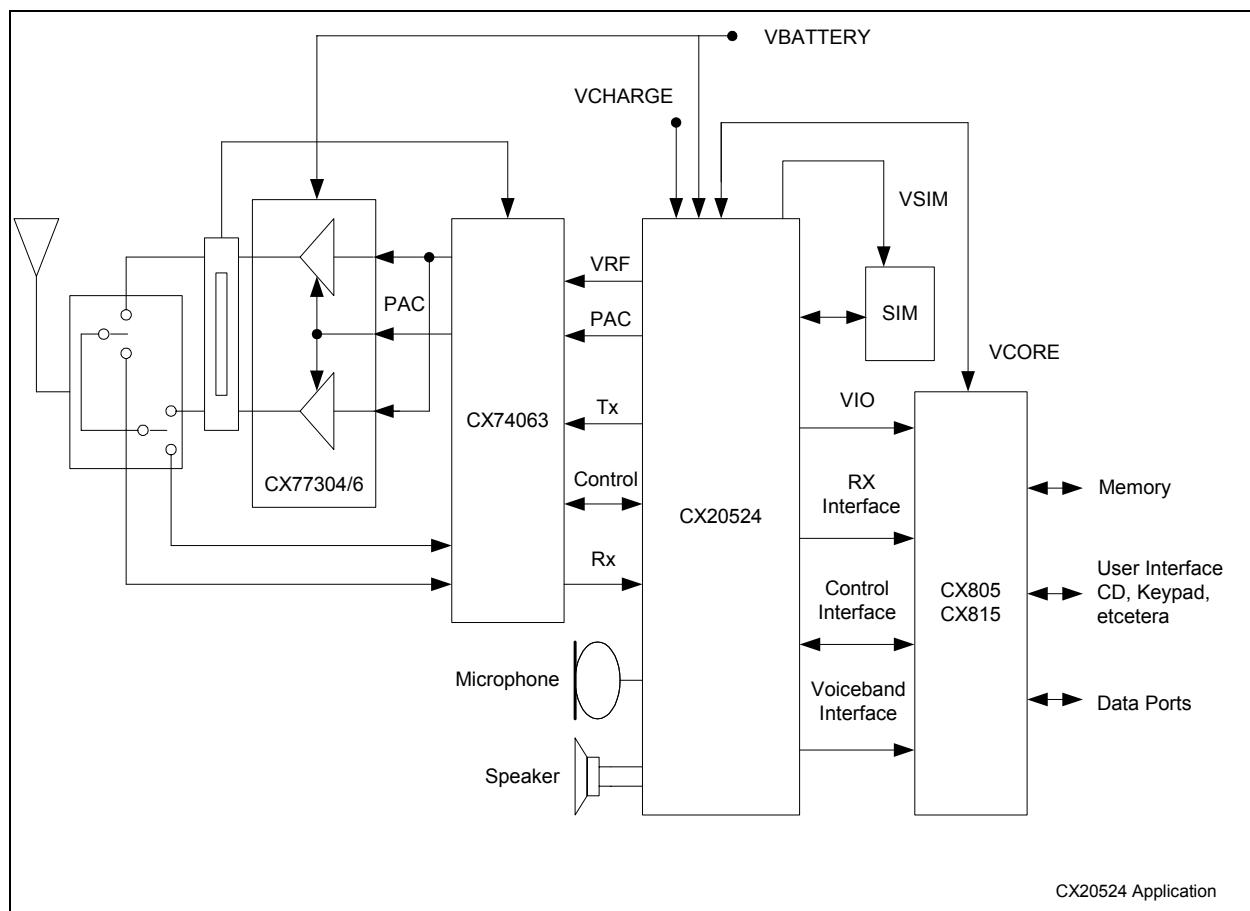


Figure 1. Typical CX20524 Application in a Handset Design

12 x 12 FFBGA - 160 Balls/ 0.80 mm Ball Pitch

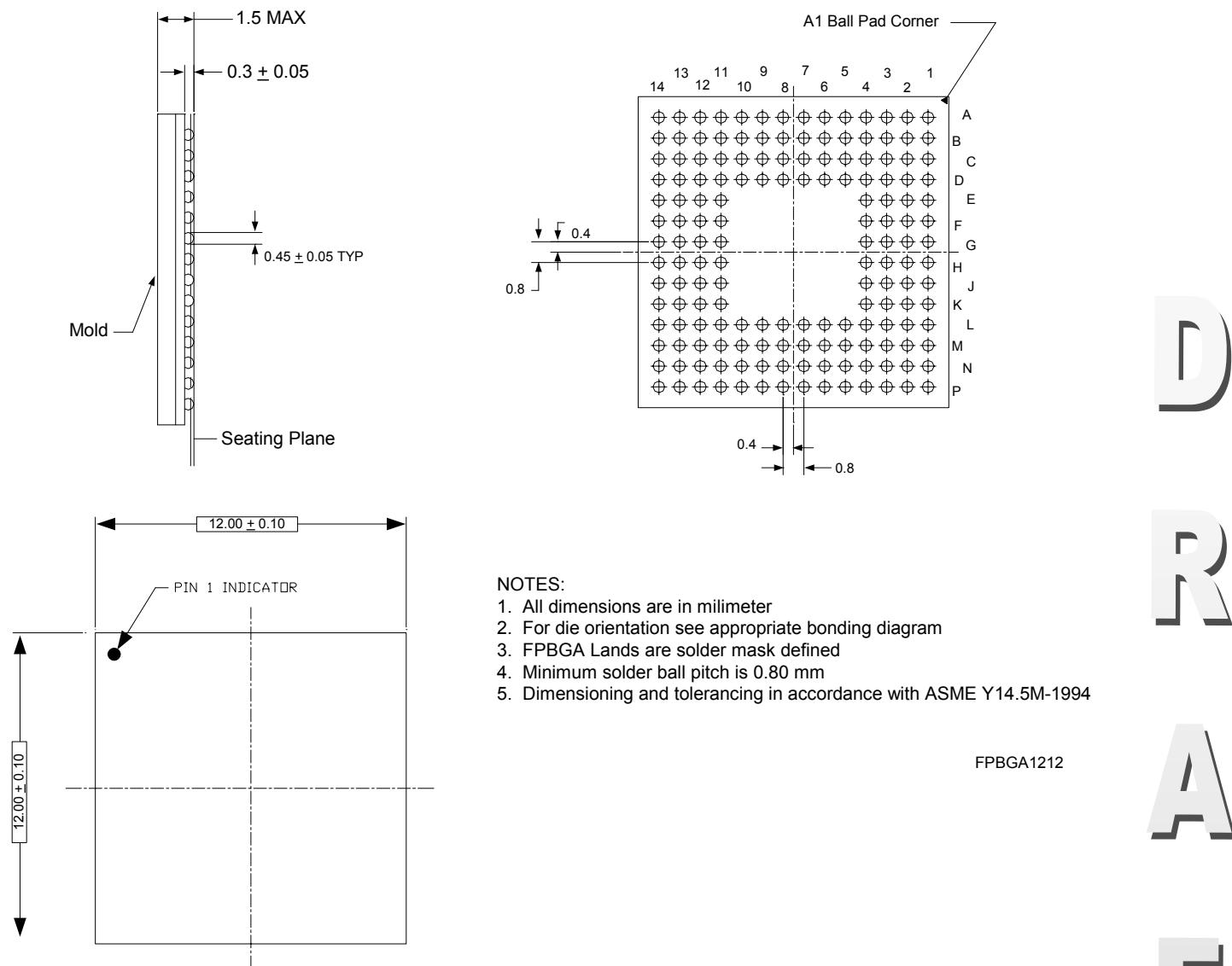
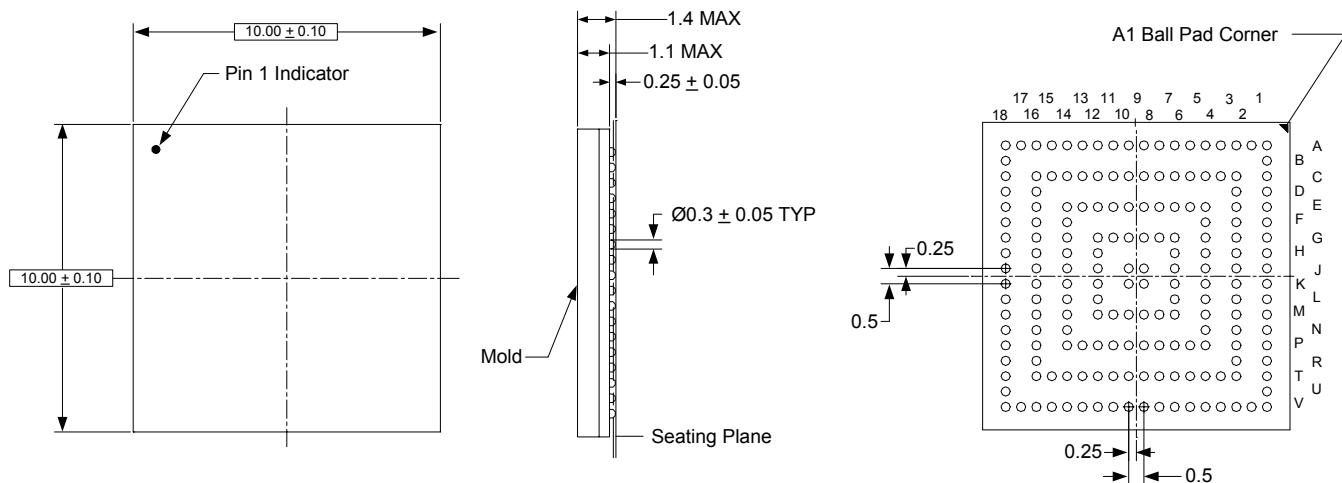


Figure 2. CX20524-12 Package Description

CX20524 Mixed Signal Device Product Summary

10 x 10 FPBGA - 180 Balls/ 0.50 mm Pitch



NOTES:

1. All dimensions are in millimeter
2. For die orientation see appropriate bonding diagram
3. FPGAs Lands are solder mask defined
4. Minimum solder pitch is 0.50 mm
5. Dimensioning and tolerancing in accordance with ASME Y14.5 M - 1994

FPBGA_1010

Figure 3. CX20524-13 Package Description

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PRODUCT SUMMARY

CX805-30 Baseband Processor for Multiband GSM and GPRS Applications

Applications

- GSM handsets and modules (850/900/1800/1900 MHz)
- GPRS handsets and modules (850/900/1800/1900 MHz)
- Bluetooth®-enabled wireless headset modules

Features

- 0.25 μ CMOS process technology
- ARM7 TDMI core
- Skyworks DSP core with all memory on-chip
- GPRS class 10 and circuit-switched data (14.4 kbps) services
- Half-rate, full-rate, and enhanced full-rate speech coders
- Voice features such as voice recognition, conversation record, and voice memo
- Hardware accelerator for GPRS encryption algorithms (GEA 1 and 2)
- Integrated Real-Time Clock (RTC)
- Interface to handset MMI peripherals such as keypad, liquid crystal display (LCD), and annunciator
- Interfaces to Skyworks IA and PMIC devices
- Interface to Subscriber Identity Module (SIM)
- Addresses up to 16 MB of external memory (flash or SRAM)
- Application Interfaces:
 - Serial/RS-232
 - Infra-red Data Adapter (IrDA)
- Low power operation. 3 V I/Os and an on-chip supplied 2.5 V core
- Eight Chip Select (CS) signals for external memory
- 16-bit data bus, 24-bit address bus

NEW

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Description

The Skyworks CX805-30 Baseband Processors (BPs) are highly integrated, dual core processors optimized for use in Global System for Mobile communications (GSM) and General Packet Radio Service (GPRS) cellular handset applications. The CX805-30 is the baseband portion of the Skyworks GSM/GPRS System Solution.

Both the Digital Signal Processor (DSP) core and the ARM7 THUMB™ Reduced Instruction Set Computing (RISC) architecture are well suited to meet the needs of low power, high performance embedded systems such as cellular phones. The BP operates over a range of 2.7 V to 3.3 V.

The baseband processing tasks are divided between the DSP and ARM7 processor cores. The DSP core executes the physical layer (layer 1) processing functions, and the ARM microcontroller core executes the Layer 2 and Layer 3 protocol software and Man-Machine Interface (MMI) functions. The two cores communicate through a dedicated block of dual port memory. Each of the functional blocks in the device can be individually powered down to ensure minimum current consumption in the idle or standby mode.

The CX805-30 family of devices is available in several package options:

- 12 x 12 mm, 0.8 mm pitch, 160-pin FPBGA
 - CX80501-31: supports up to Class 8 GPRS operation
 - CX80502-33/-35: supports up to Class 10 GPRS operation
- 10 x 10 mm, 0.5 mm pitch, 180-pin FPBGA
 - CX80501-32: supports up to Class 8 GPRS operation
 - CX80502-34/-36: supports up to Class 10 GPRS operation
 - CX80503-34: supports up to Class 10 GPRS operation and features optimized ROM code
- Lead-free 10 x 10 mm, 0.5 mm pitch, 180-pin FPBGA
 - CX80502-38: supports up to Class 10 GPRS operation
 - CX80503-38: supports up to Class 10 GPRS operation and features optimized ROM code

Figure 1 provides a block diagram of the CX805-30 device in a typical application. Package dimensions are provided in Figure 2 for the 12 x 12 devices and Figure 3 for the 10 x 10 devices.

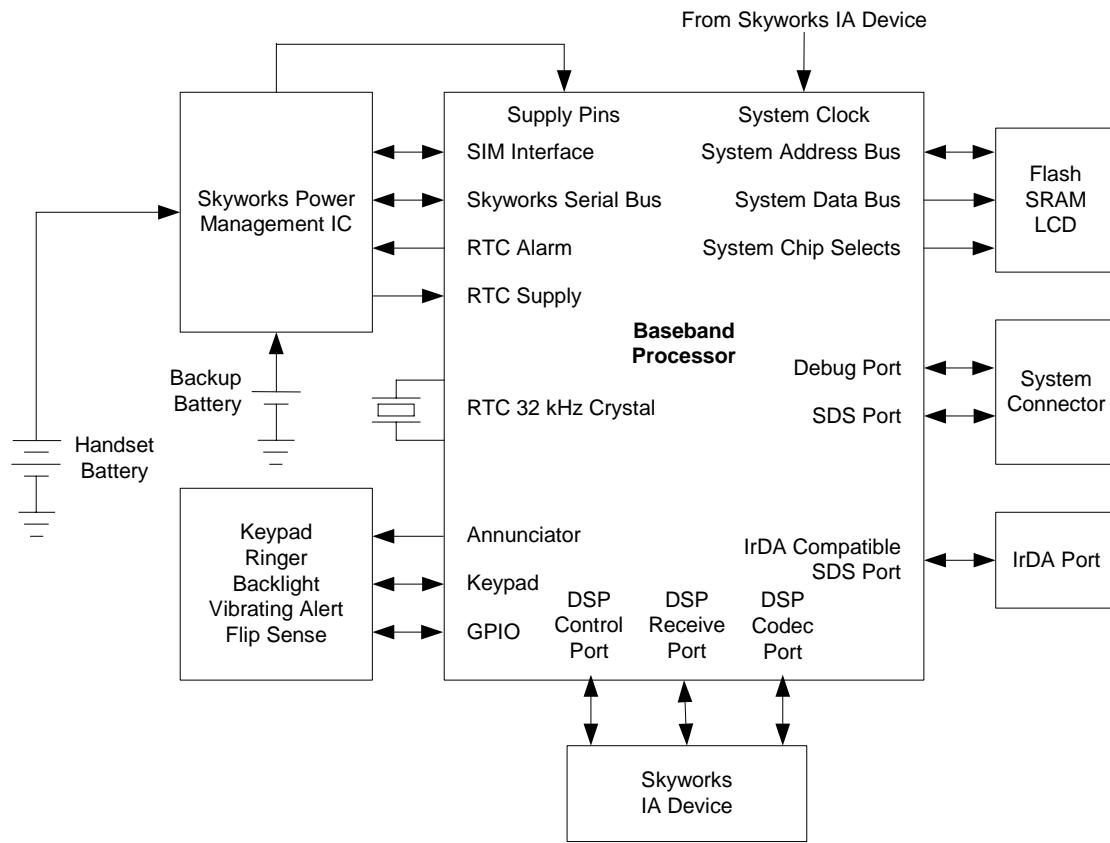
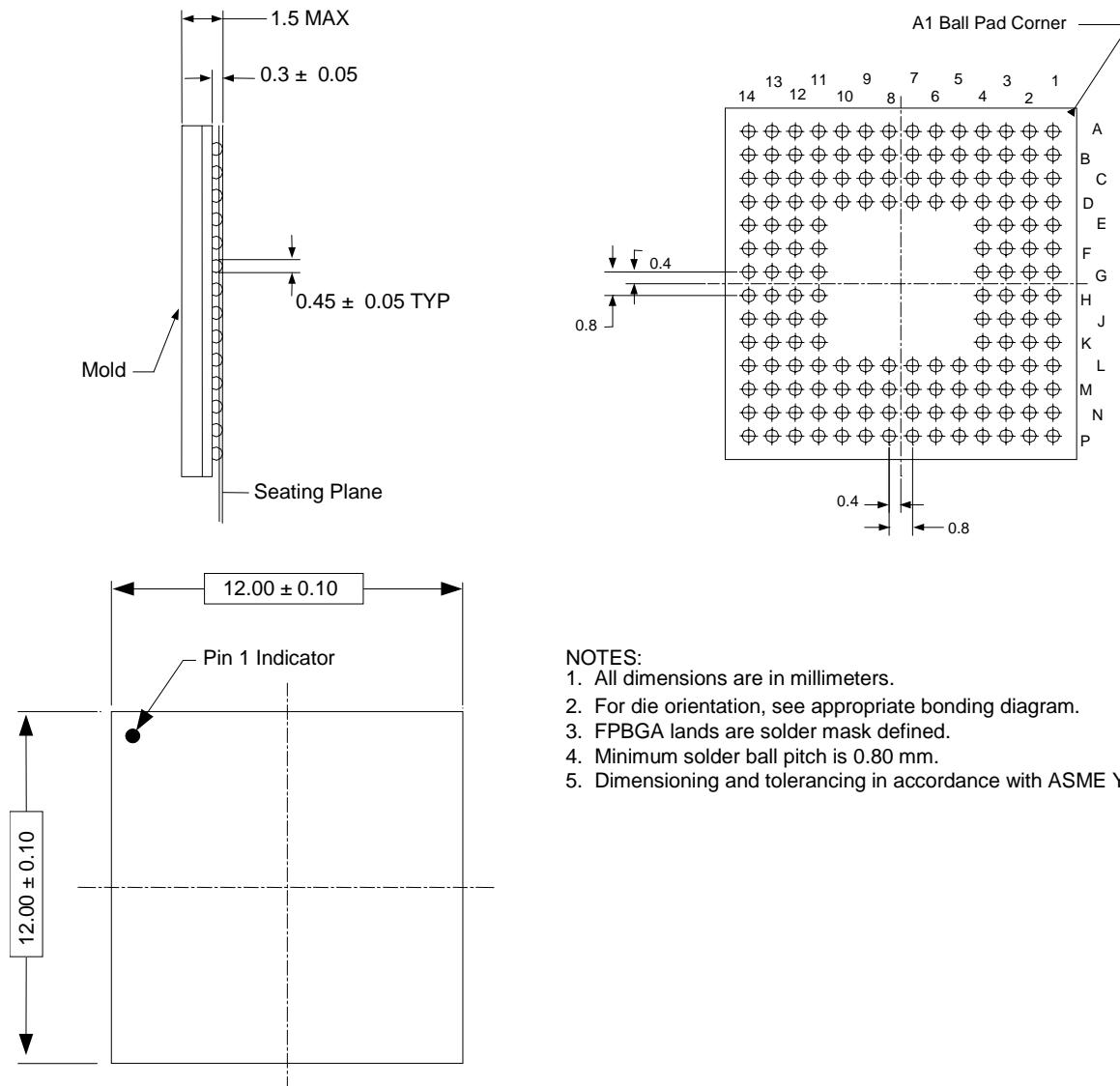


Figure 1. Block Diagram of the CX805-30 in a Typical Application

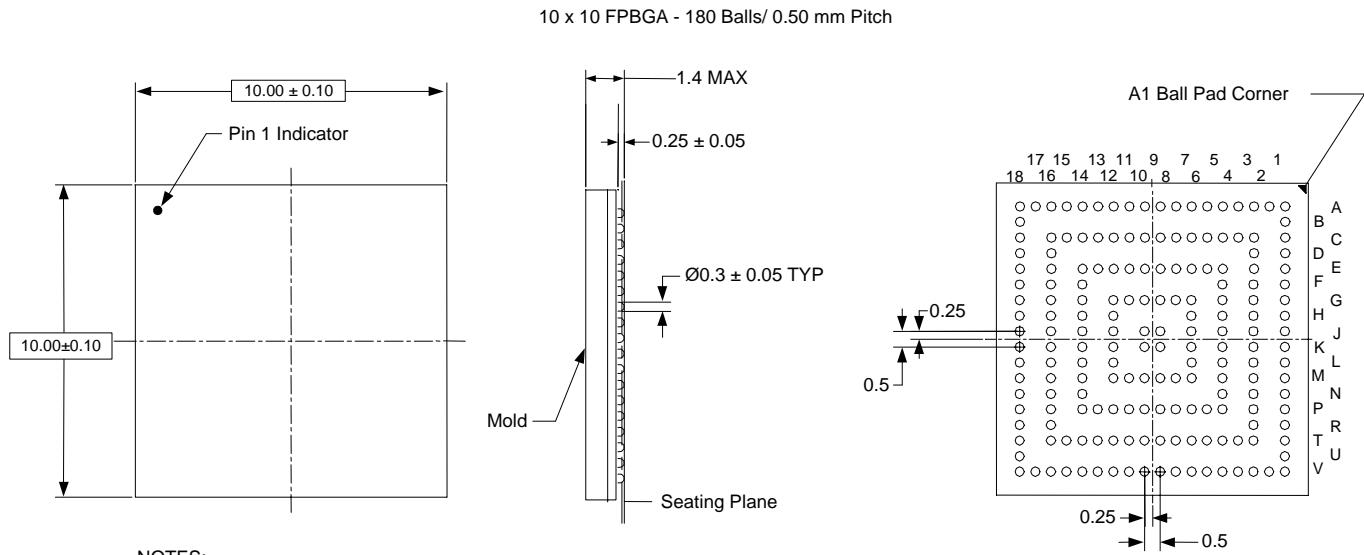
12 x 12 FPBGA - 160 Balls/ 0.80 mm Ball Pitch



NOTES:

1. All dimensions are in millimeters.
2. For die orientation, see appropriate bonding diagram.
3. FPBGA lands are solder mask defined.
4. Minimum solder ball pitch is 0.80 mm.
5. Dimensioning and tolerancing in accordance with ASME Y14.5M-1994

Figure 2. 160-pin FPBGA Package Dimensions



NOTES:

1. All dimensions are in millimeter
2. For die orientation see appropriate bonding diagram
3. FPBGA Lands are solder mask defined
4. Minimum solder pitch is 0.50 mm
5. Dimensioning and tolerancing in accordance with ASME Y14.5 M - 1994

Figure 3. 180-pin FPBGA and Lead-free 180-pin Lead-free FPBGA Package Dimensions

Ordering Information

Model Name	Part Number	Device Configuration
Baseband Processor	CX80501-31	12 x 12 mm, 160-pin, 0.8 mm pad pitch, FPBGA, GPRS Class 8
	CX80501-32	10 x 10 mm, 180-pin, 0.5 mm pad pitch, FPBGA, GPRS Class 8
	CX80502-33 ¹	12 x 12 mm, 160-pin, 0.8 mm pad pitch, FPBGA, GPRS Class 10
	CX80502-35 ¹	
	CX80502-34 ²	10 x 10 mm, 180-pin, 0.5 mm pad pitch, FPBGA, GPRS Class 10
	CX80502-36 ²	
	CX80502-38	Lead-free 10 x 10 mm, 180-pin, 0.5 mm pad pitch, FPBGA, GPRS Class 10
	CX80503-34	10 x 10 mm, 180-pin, 0.5 mm pad pitch, FPBGA, GPRS Class 10 with optimized ROM code
	CX80503-38	Lead-free 10 x 10 mm, 180-pin, 0.5 mm pad pitch, FPBGA, GPRS Class 10 with optimized ROM code
1. The CX80502-33 and CX80502-35 are interchangeable devices.		
2. The CX80502-34 and CX80502-36 are interchangeable devices.		

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MV3018

Overview

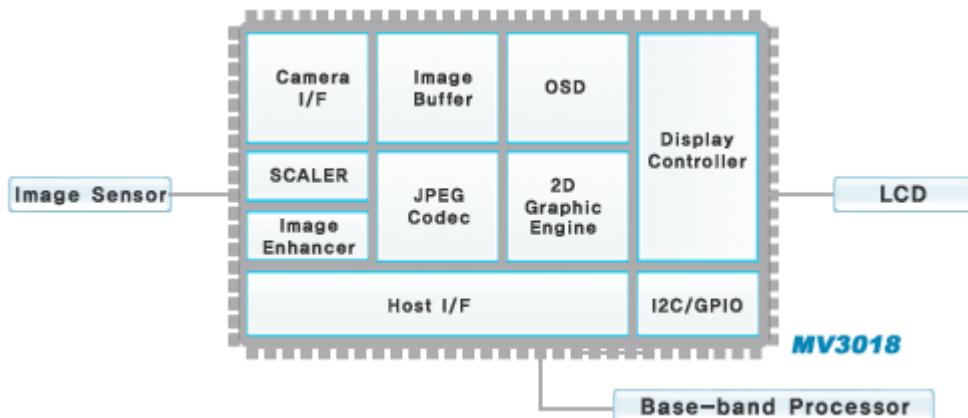


MV3018

MV3018 is a Camera Control Processor uniquely designed to provide the most optimized movement of image data throughout portable terminal devices such as mobile handsets. It processes VGA level images and delivers 30 frames per second displays through its hardware based real-time JPEG compression and decompression. MV3018 eliminates system bottlenecks by assuming the processing load for displaying images, thus freeing up the system baseband. The 16bit/18bit data bus supports interface types such as i80, TI, m68 and Agere baseband chipsets. MV3018 incorporates features such as image enhancement algorithm, digital zoom, thumbnail and EZ-OSD enabling feasibility for phone manufacturers to design products with maximized performance.

[▲ Diagram](#) [▲ Features](#)

Diagram



Features

Image Sensor>>	<ul style="list-style-type: none">* CMOS/CCD Type Image Sensor Interface* Image Size: VGA / CIF type
Image Effects>>	<ul style="list-style-type: none">* GAMMA Enhance, Edge Enhance, Smoothing filter* Gray / Negative / Sepia / Emboss / Sketch
Compression>>	<ul style="list-style-type: none">* JPEG Encoding YUV422 up to VGA* 90°, 180°, 270° Rotate & Mirror Capture Support up to VGA* Free Size JPEG Encoding Support
Decompression>>	<ul style="list-style-type: none">* JPEG Decoding (444/422/420/411) up to VGA
Data Interface>>	<ul style="list-style-type: none">* Host I/F Parallel 16bit/18bit* Strobe Function (FLASH)* 5 GPIO

Package>> * 8mmx8mm, 81CABGA 0.8mm pitch, 1.1mm thickness

Moving Picture>>

- * MJPEG Format
- * MPEG Input Format Support
- * Hardware Dedicated Method
- * Software management Method
- * Easy Controllable Encoding & Decoding Frame Rate

Display Management>>

- * Digital Real Zoom: up to 8 times
- * Superimpose (16bit/18bit color)
- * 90°, 180°, 270° Rotate Preview Support
- * Frame Rate: 30fps
- * Two Window OSD
- * 2 LCD Interface (Main, Sub) : 8bit, 12bit, 16bit, 18bit
- * QVGA Resolution(320x240)

2D Graphic Engine>>

- * BitBLT
- * Color Conversion

S/W Library>>

- * MV300 S/W Library compatibility for all CCP products
- * Many Applications and Sample codes are available
- * Easy to port and simple to use

Power Management>>

- * Single Power 2.8V
- * Wide Range I/O (1.8V ~ 3.0V)
- * Standby Current Less Than 100uA
- * Full Operation Current Less Than 30mA (under 10mA in the preview mode)
- * Separated I/O power support : SVDD(Sensor), MVDD(MCU), LVDD(LCD),
- * RVDD(Regulator)