MS Series Encoder Data Structure

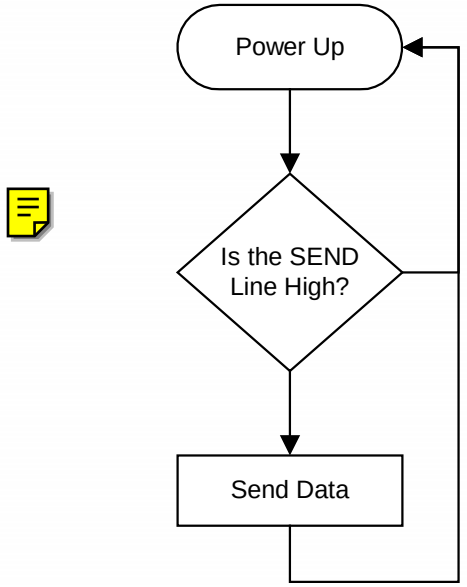
The MS Series encoder is designed to securely register button presses or switch closures over a wireless link for remote control applications. It will turn eight parallel input lines into a secure, encoded serial bit stream output.

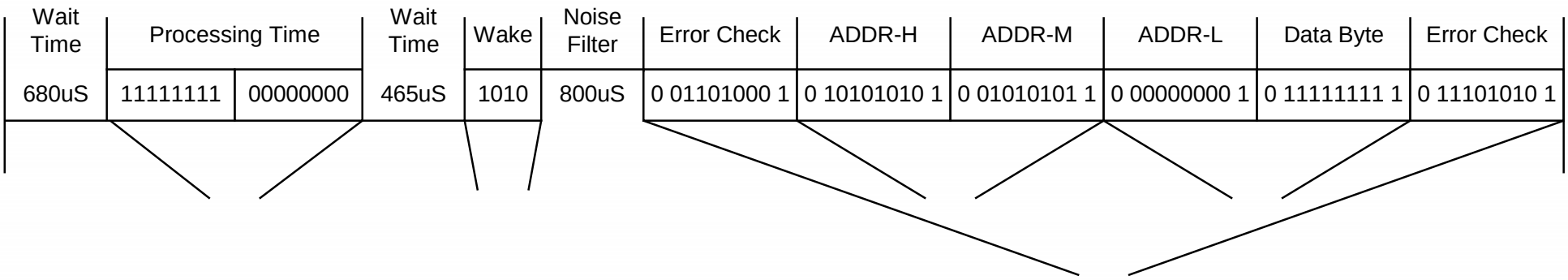
The MS Series algorithm is designed to create a data stream with a 50% duty cycle by using the same number of high bits and low bits. Two wait times reduce this duty cycle to just below 50%.

Logic State Description:
- 1 = HIGH
- 0 = LOW

Total bits, including start and stop bits = 80
- Total 1's = 40
- Total 0's = 40

Value for each bit per baud rate:
- 2400bps = 417uS or 1.18% of duty cycle
- 9600bps = 104uS or 1.01% of duty cycle
- 19200bps = 52uS or 0.85% of duty cycle
- 28800bps = 35uS or 0.74% of duty cycle





$$\text{Duty Cycle} = \frac{\text{Time High}}{\text{Total Time}} \rightarrow \frac{\text{40 bits + 800uS}}{\text{80 bits + 680uS + 465uS + 800uS}} \rightarrow \frac{\text{(40*417uS) + 800uS}}{\text{(80*417uS) + 1,945uS}} = \frac{\text{17,480uS}}{\text{35,305uS}} = 49.51\%$$

MS Series Encoder Data Structure

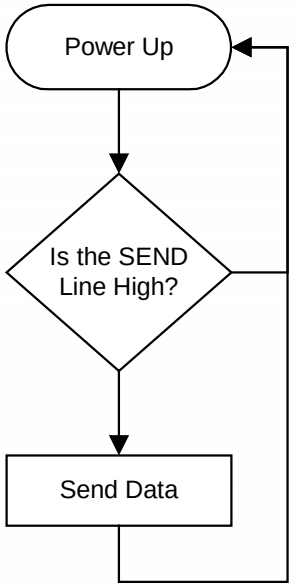
The MS Series encoder is designed to securely register button presses or switch closures over a wireless link for remote control applications. It will turn eight parallel input lines into a secure, encoded serial bit stream output.

The MS Series algorithm is designed to create a data stream with a 50% duty cycle by using the same number of high bits and low bits. Two wait times reduce this duty cycle to just below 50%.

Logic State Description:
- 1 = HIGH
- 0 = LOW

Total bits, including start and stop bits = 80
- Total 1's = 40
- Total 0's = 40

Value for each bit per baud rate:
- 2400bps = 417uS or 1.18% of duty cycle
- 9600bps = 104uS or 1.01% of duty cycle
- 19200bps = 52uS or 0.85% of duty cycle
- 28800bps = 35uS or 0.74% of duty cycle



Wait Time	Processing Time		Wait Time	Wake	Noise Filter	Error Check	ADDR-H	ADDR-M	ADDR-L	Data Byte	Error Check
680uS	11111111	00000000	465uS	1010	800uS	0 01101000 1	0 10101010 1	0 01010101 1	0 00000000 1	0 10001000 1	0 11101010 1

$$\text{Duty Cycle} = \frac{\text{Time High}}{\text{Total Time}} \rightarrow \frac{\text{40 bits + 800uS}}{\text{80 bits + 680uS + 465uS + 800uS}} \rightarrow \frac{\text{(34*417uS) + 800uS}}{\text{(80*417uS) + 1,945uS}} = \frac{\text{14,978uS}}{\text{35,305uS}} = 42.42\%$$