MaxID RM100 RFID reader Technical Description

Version	***0.1***
Date	***21 September, 2005***
Document Status	***Draft***
Document ID	***1209***

MaxID Limited, Quatro House, Lyon Way, Frimley, Surrey GU16 7ER, United Kingdom
Phone: +44 (0) 1276 80 4498, Fax: +44 (0) 1276 80 4499, URL: www.MaxIDcorp.com

Change History

Configuration Control

Project:	RFID
Title:	MaxID RM100 RFID reader Technical Description
Document ID:	1209
Created by:	Riaan van den Berg
Creation Date:	21 September 2005

Document History

Version	*Date*	*Status*	*Who*	*Saved as:*

Revision History

Version	*Date*	*Changes*
0. 1	2005/0/21	Initial release.

Management Authorisation

Version	*Date*	*Status*	*Approval Minutes Reference*

Table of Contents

1. Introduction

The RM100 from MaxID Ltd is a multi-protocol radio frequency identification (RFID) reader designed to support all electronic product code (EPC)-compliant UHF RFID tags.

The RM100 is an industrial-class OEM (Original Equipment Manufacturer) reader that provides all of the RFID control functions required to power and communicates with passive RFID tags. The RM100 was designed to integrate into handheld portable data terminals, printers, label applications, mobile computers and other OEM devices.

It is a high-performance reader that collects, writes, processes and communicates information from all classes of EPC RFID tags. The RM100 leverages advanced digital filter technology to deliver superior interference management and are optimized to read tags in both clean and noisy radio environments.

2. FCC Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.

WARNING !

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiated radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

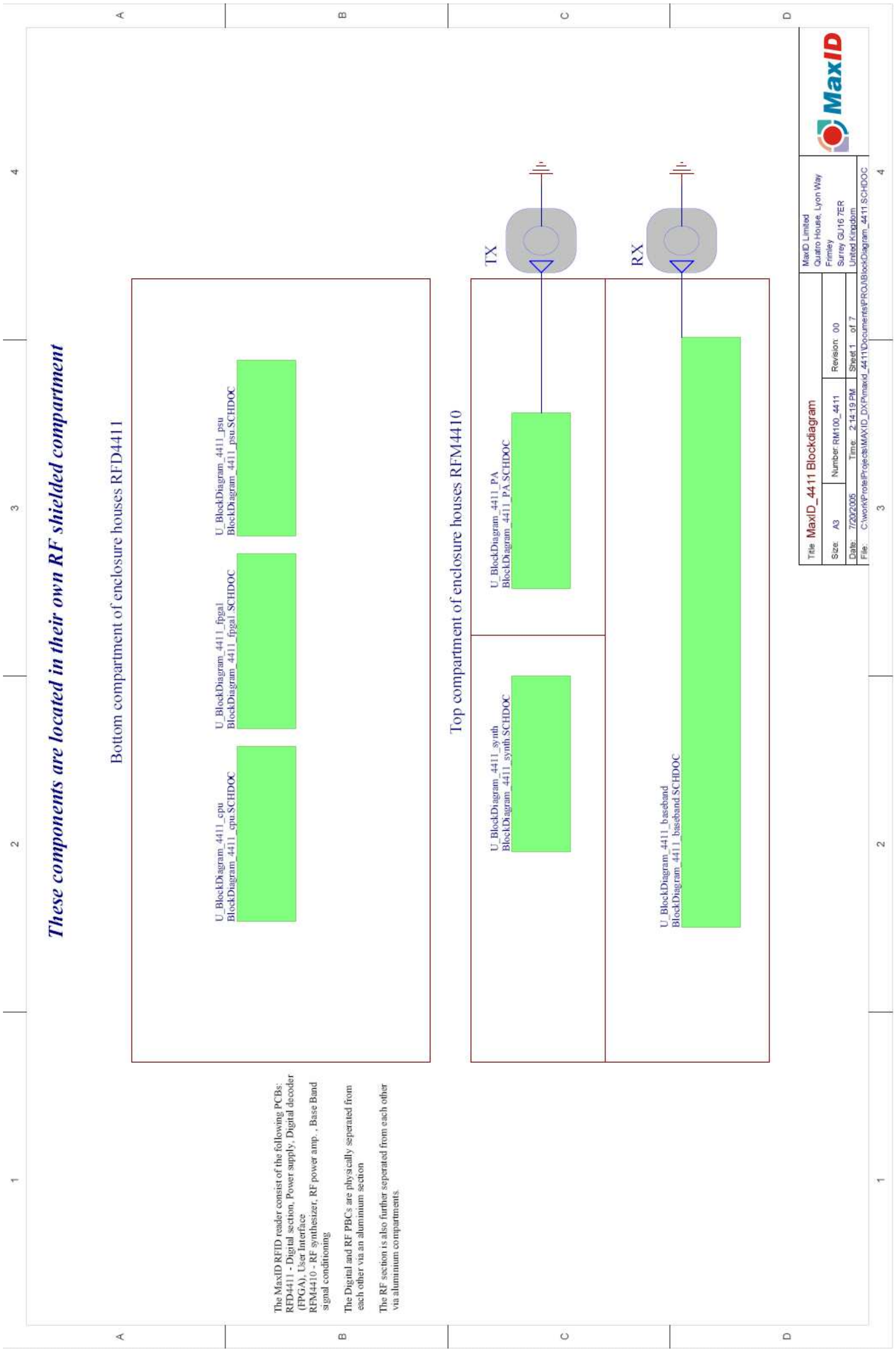
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

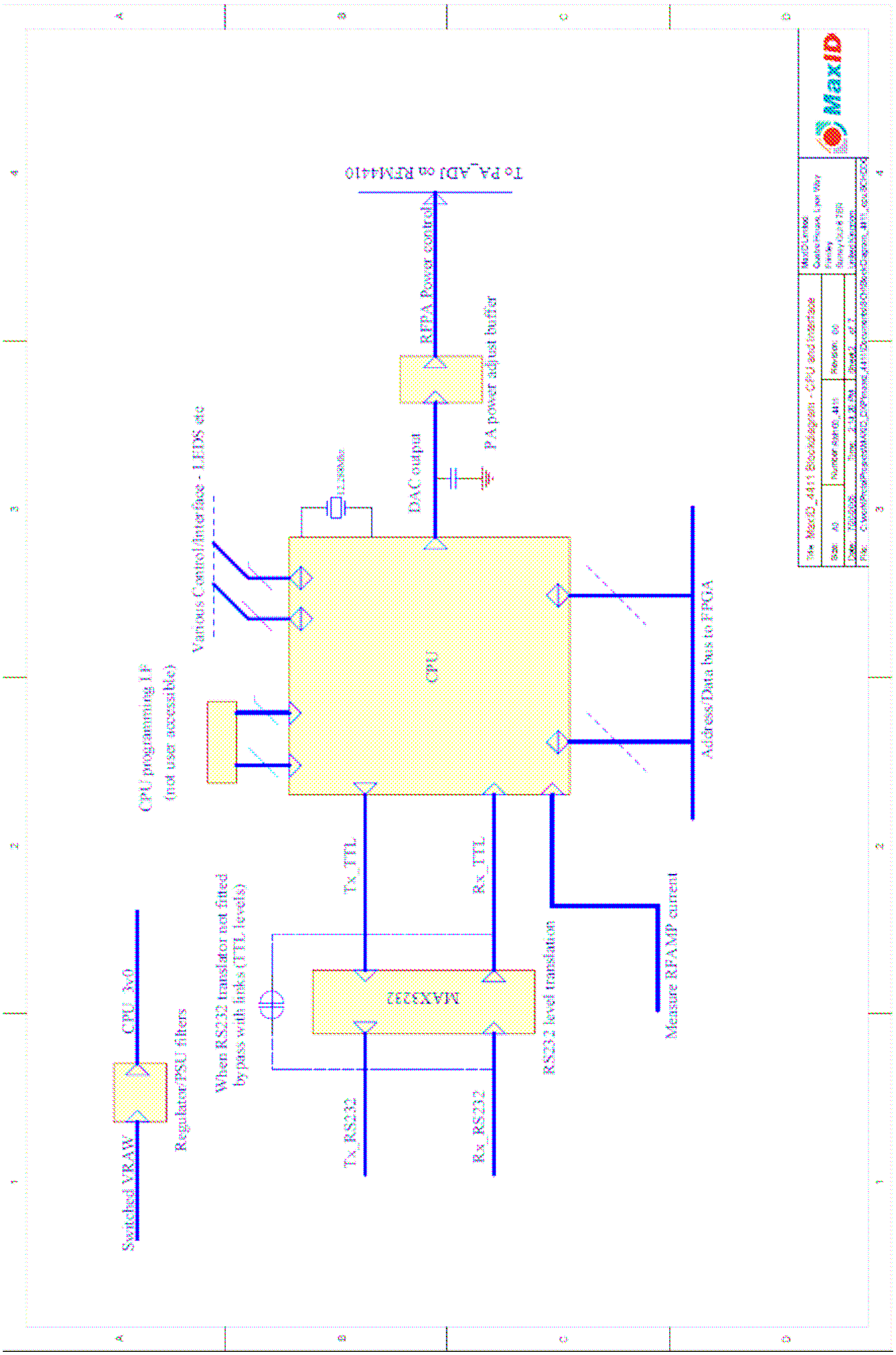
Changes or modifications not expressly approved by the party responsible for compliance could void the user‘s authority to operate the equipment.

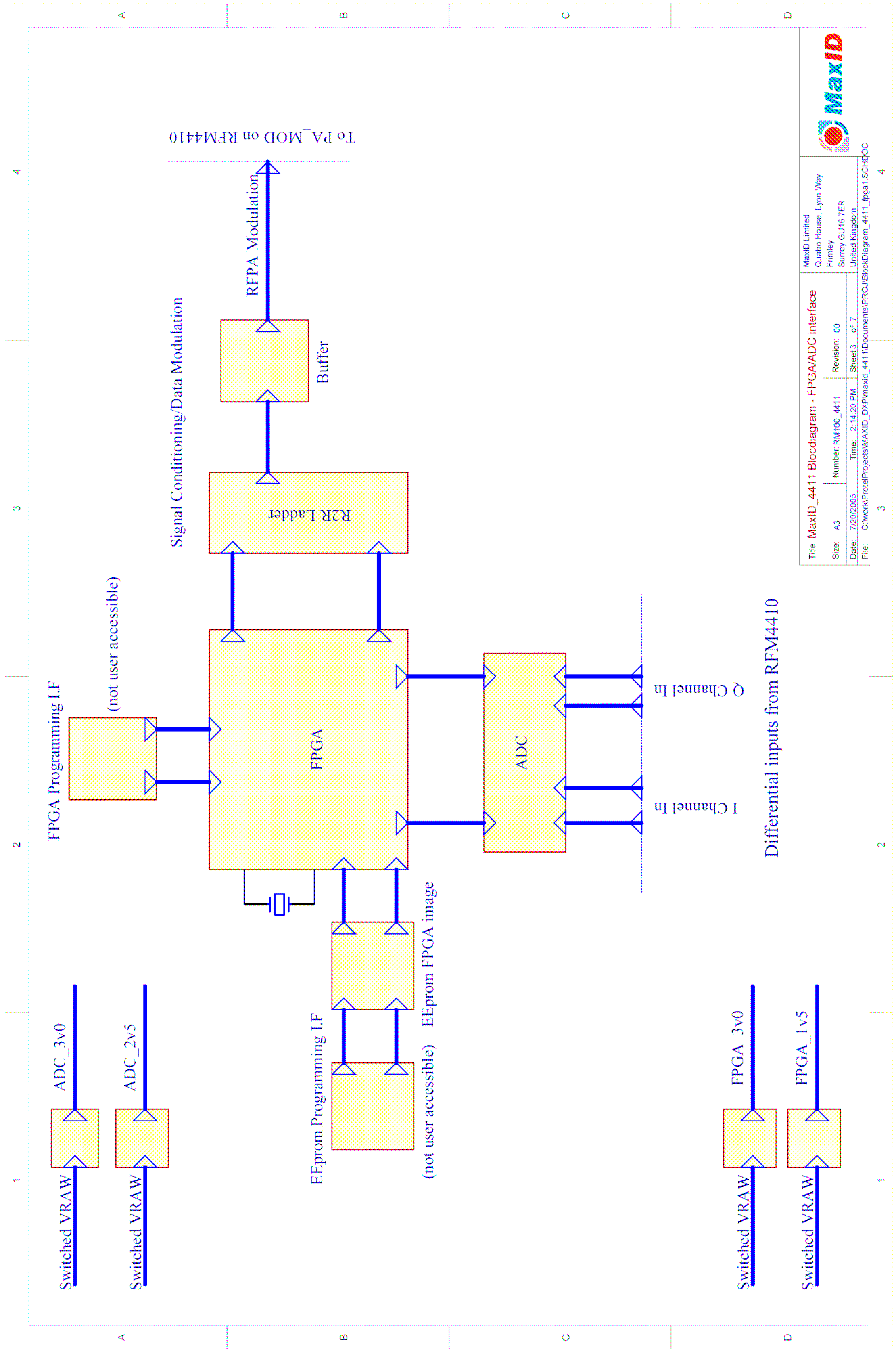
3. Limitation of Liability

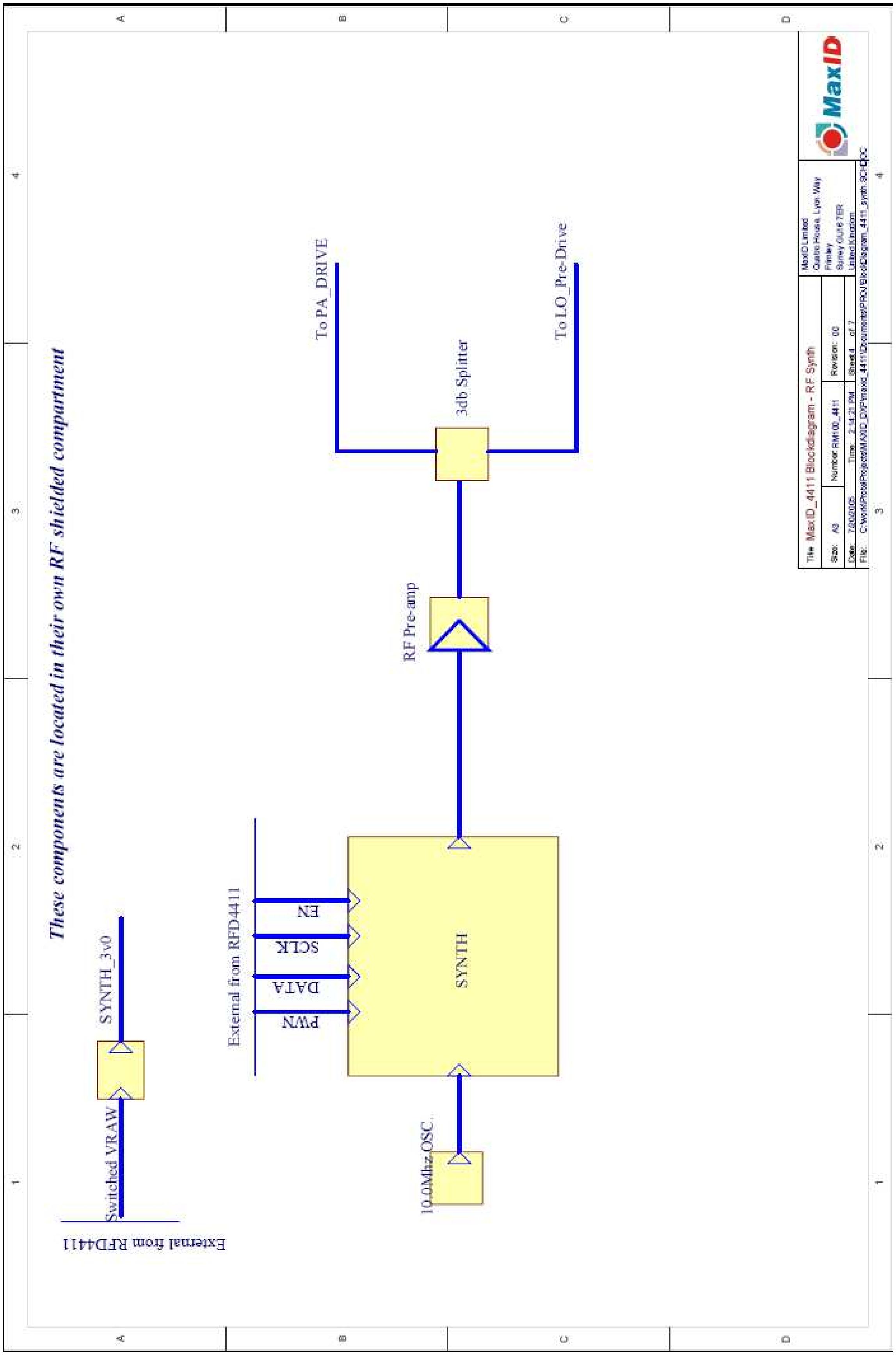
In no event shall MaxID Ltd. or anyone else involved in the creation, production or delivery of the accompanying product (including hardware and software) be liable for any damages whatsoever (including, without limitation, consequential damages including loss of business profits, business interruption or loss of business information) arising out of the use of or the results of use of or inability to use such product, even if MaxID Ltd. has been advised of the possibility of such damages. Some jurisdictions do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you.

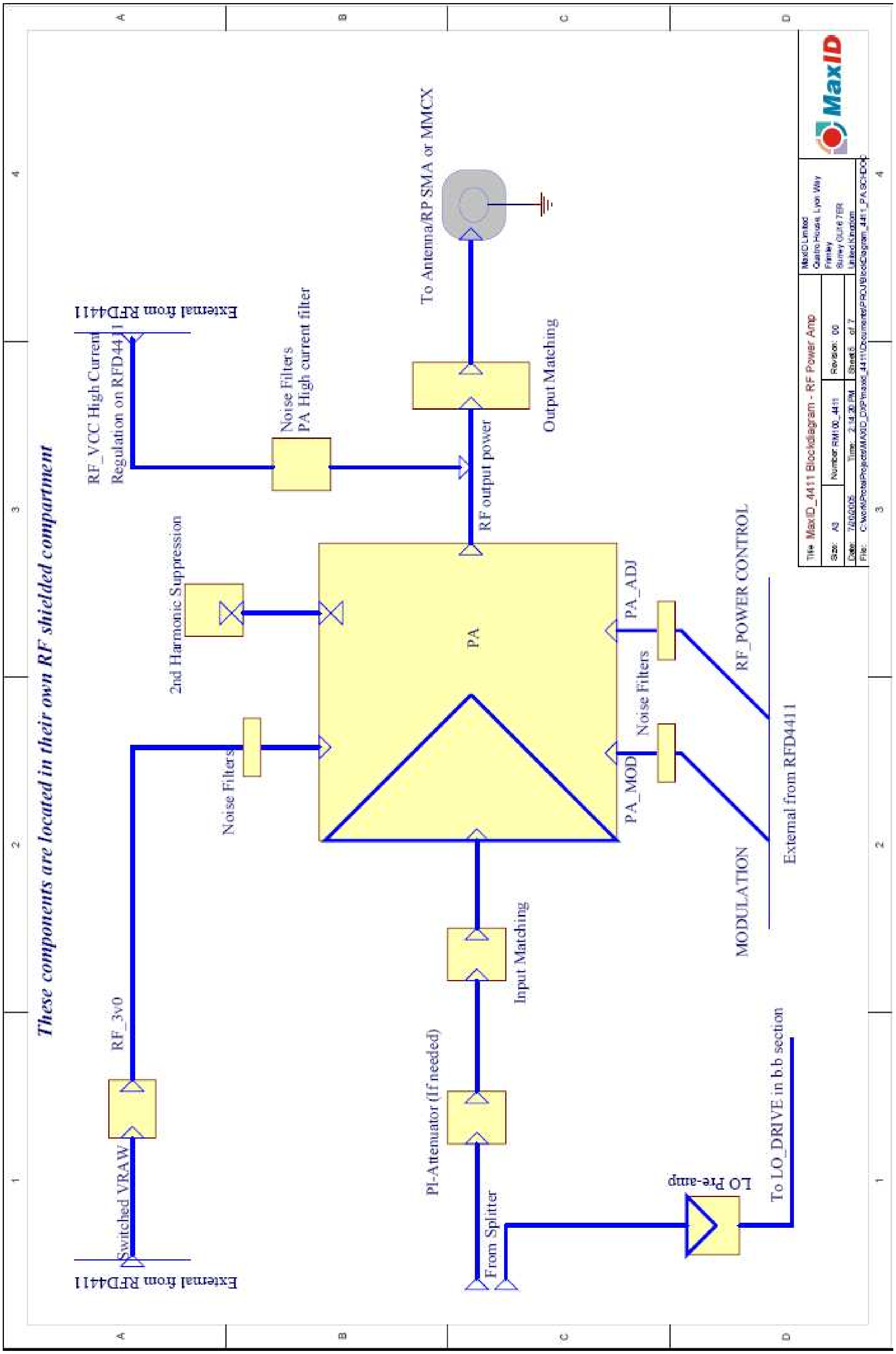
4. Functional Block diagram

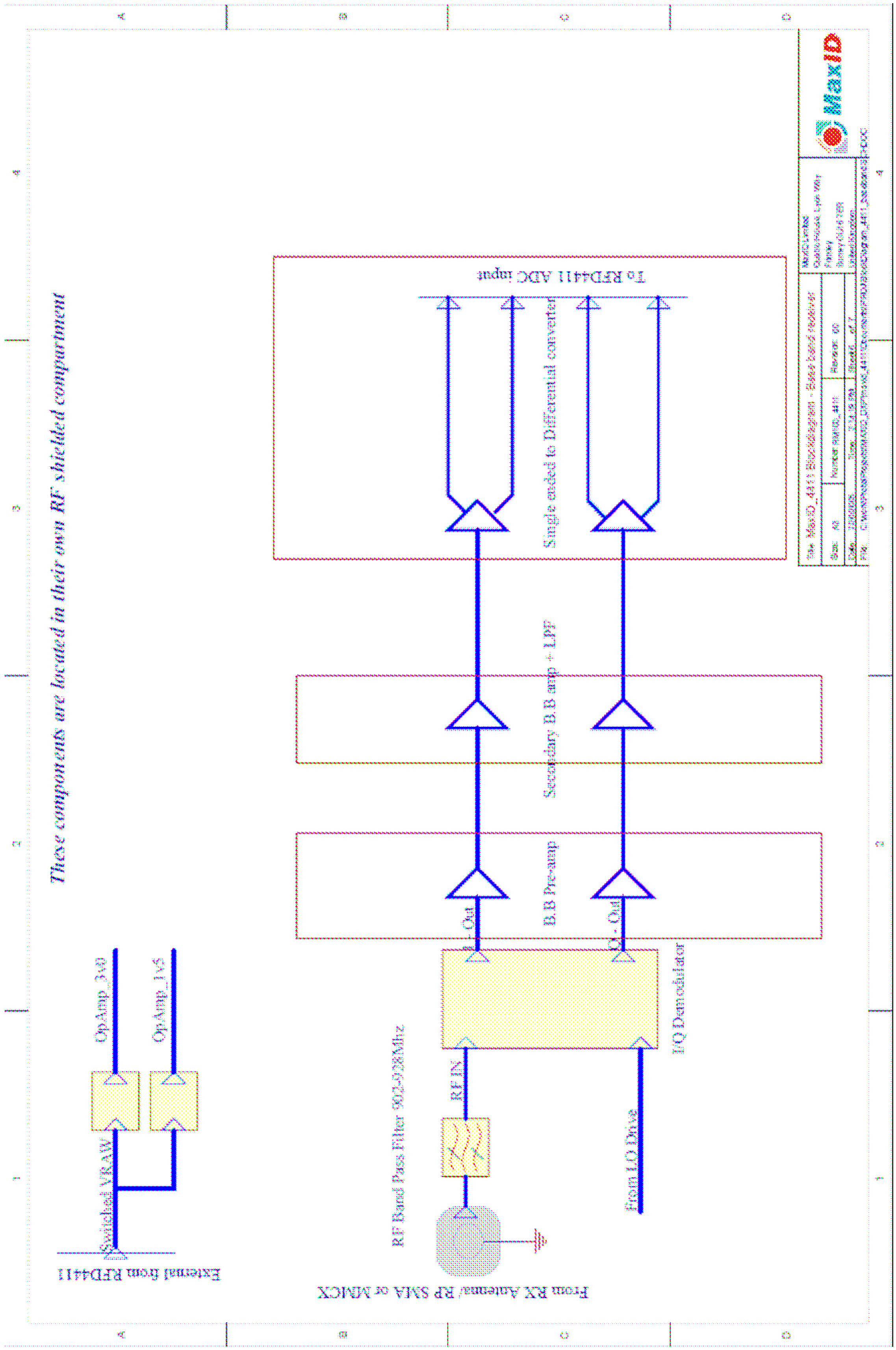


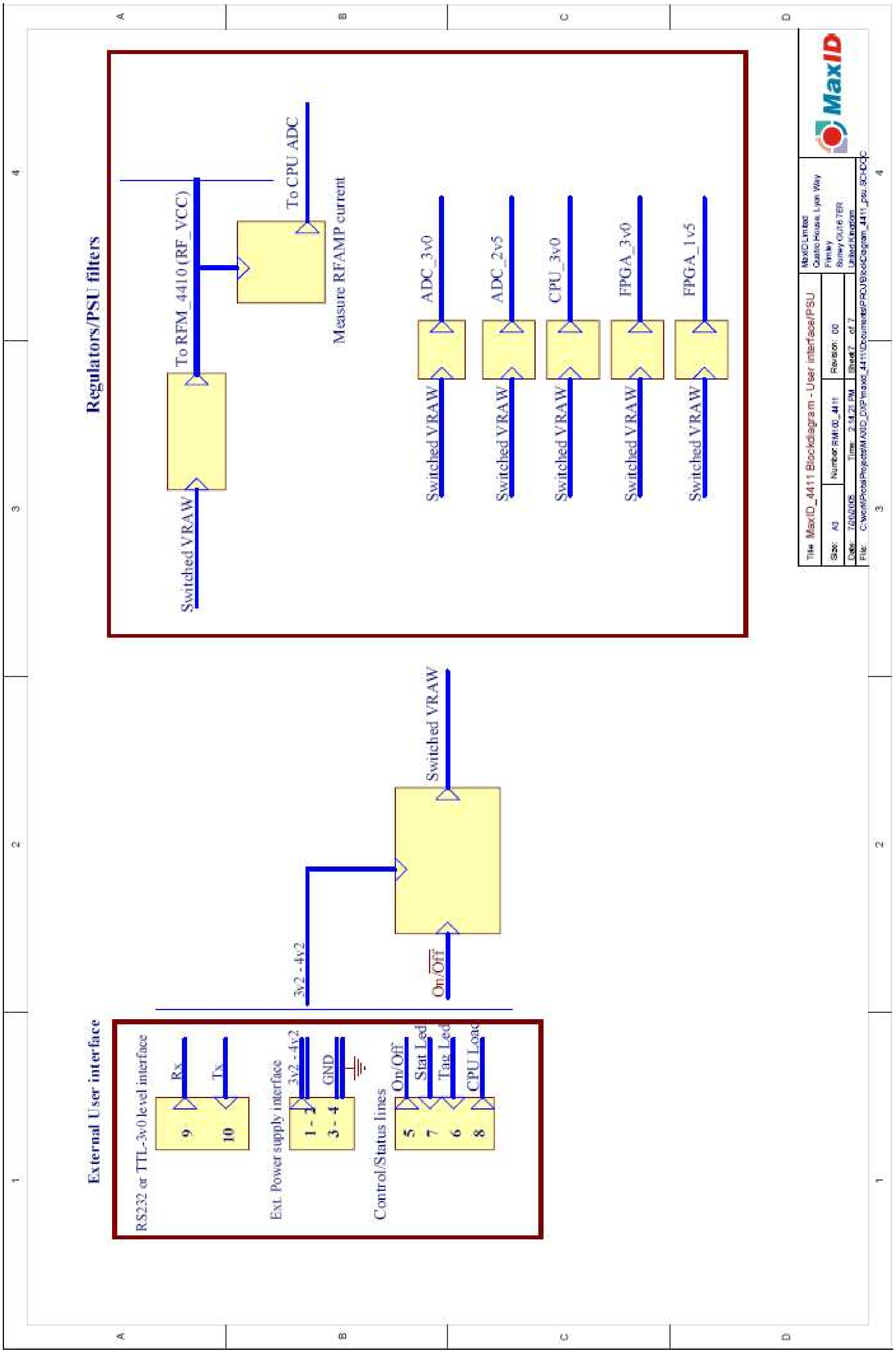

To PA_ADJ on RFM4410
RFPA Power control
PA power adjust buffer
DAC output
Various Control/interface - LEDS etc
CPU programming I/F
(not user accessible)
CPU
Address/Data bus to FPGA
Tx_TTL
Rx_TTL
Measure RFAMP current
MAX3232
RS232 level translation
When RS232 translator not fitted
by pass with links (TTL levels)
Tx_RS232
Rx_RS232
Switched VRAW
CPU 3v0
Regulator/PSU filters
MaxID


To PA_MOD on RFM4410
RFPA Modulation
Signal Conditioning/Data Modulation
Buffer
R2R Ladder
FPGA Programming I.F
(not user accessible)
FPGA
ADC
Q Channel In
I Channel In
Differential inputs from RFM4410
EEprom Programming I.F
(not user accessible)
EEprom FPGA image
ADC_3v0
ADC_2v5
FPGA_3v0
FPGA_1v5
Switched VRAW
Switched VRAW
Switched VRAW
Switched VRAW
Title MaxID_4411 Blocdiagram - FPGA/ADC interface
MaxID Limited
Quattro House, Lyon Way
Frimley
Surrey GU16 7ER
United Kingdom
Size: A3
Number: RM100_4411
Revision: 00
Date: 7/20/2005
Time: 2:14:20 PM
Sheet3 of 7
MaxID


These components are located in their own RF shielded compartment
To PA_DRIVE
To LO_Pre-Drive
3db Splitter
RF Pre-amp
SYNTH
EN
SCLK
DATA
PWN
External from RFD4411
SYNTH_3v0
Switched VRAW
10.0Mhz OSC.
External from RFD4411
MaxID
Title MaxID_4411 Blockdiagram - RF Synth
Size: A3
Number RM100_4411
Revision: 00
MaxID Limited
Surrey
United Kingdom


These components are located in their own RF shielded compartment
External from RFD4411
Switched VRAW
RF_3v0
Noise Filters
RF_VCC High Current
Regulation on RFD4411
External from RFD4411
Noise Filters
PA High current filter
2nd Harmonic Suppression
PA
PA_ADJ
PA_MOD
Noise Filters
RF output power
Output Matching
To Antenna/RP SMA or MMCX
Input Matching
PI-Attenuator (If needed)
From Splitter
LO Pre-amp
To LO_DRIVE in b.b section
MODULATION
RF_POWER CONTROL
External from RFD4411
Title MaxID_4411 Blockdiagram - RF Power Amp
MaxID Limited
Quatro House, Lyon Way
Frimley
Surrey GU16 7ER
United Kingdom


These components are located in their own RF shielded compartment
To RFD4411 ADC input
Single ended to Differential converter
Secondary B.B amp + LPF
B.B Pre-amp
I - Out
Q - Out
I/Q Demodulator
RF IN
From LO Drive
RF Band Pass Filter 902-928MHz
From RX Antenna/ RF SMA or MMCX
External from RFD4411
Switched VRAW
OpAmp_3v0
OpAmp_1v5



Regulators/PSU filters
Switched VRAW
To RFM_4410 (RF_VCC)
To CPU ADC
Measure RFAMP current
ADC_3v0
ADC_2v5
CPU_3v0
FPGA_3v0
FPGA_1v5
External User interface
RS232 or TTL-3v0 level interface
Rx
Tx
9
10
Ext. Power supply interface
3v2 - 4v2
GND
1 - 2
3 - 4
Control/Status lines
On/Off
Stat Led
Tag Led
5
7
6
8
3v2 - 4v2
On/Off
MaxID

5. Block diagram Description

The RM100 RFID reader module consist of 2 PC boards:

1) Digital board and
2) RF board

These two boards connect to each other via 3 very low profile connectors.

One connector control the RF synthesiser, a second connector provide RF transmit power control as well as modulation index adjustments control, while a third connector is used to interconnect the received I & Q signals the ADC converter on the Digital board.

5.1 Digital Board – RFD4411

The Digital board can be divided into 3 sections namely:

1) Power supply unit (PSU)
2) Micro Controller Unit (MCU)
3) Digital Signal processing (DSP)

5.1.1 Power supply unit

The RM100 module was designed to operate from a single Lithium-Ion battery. Although the nominal voltage of a Lithium-Ion cell is 3.6v or 3.7V, most Lithium-Ion batteries is still capable of supplying power even when these cells reach 3.3Volts

To ensure stability in the system, low drop voltage regulators were use. Different regulators in different sections were used to ensure best regulation and decoupling possible.

Power to the final Power Amp (PA) on the RF board is regulated by a 3VDC, 1.5A Low Drop Out (LDO) linear voltage regulator. See net name RF_VCC. The CPU is getting power from a separate 3VDC regulator and although the FPGA also require 3VDC, the FPGA also uses a dedicated 3VD regulator. See net names VCC_CPU_3V0 and VCC_FPGA_3V0 respectively. The FPGA also uses a 1.5V reference voltage.

The Analogue to digital converter (ADC) is using a 3VDC and 2.5VD regulated voltage. These voltages are also dedicated to the ADC. See net names VCC_ADC_3V0 and VCC_ADC_2V5.

5.1.2 Micro controller

The Micro controller is a 32-bit architecture, designed for high-speed applications. The main purposes of the MCU is as follows:

1) Control RF operating frequencies by program a synthesiser on the RF board

2) Control RF power and modulation depth on the RF board
3) Control mode in which the RF board must interrogate different passive tags
4) Decode received information from the tags after the FPGA performed all the necessary signal processing functions
5) Handle interface protocol to external computer or data terminal via RS-232
6) Perform basic interface functions to operators by driving different LED's

The MCU control all the frequency management on the RF board. The MCU program the RF synthesiser with the desired hopping frequency and it also determine which channel to hop to. In the 902-928Mhz bands, 50 channels are used with 500KHz channel spacing.

The RF board is totally digitally controllable from the digital board. The MCU has a build in DAC (digital to analogue converter) and this is used to control the RF power output on the final Power Amplifier (PA). The modulation index on the transmitter is also totally digitally controllable by the MCU. The MCU pass the digital modulated data to the FPGA and FPGA uses a R2R ladder to convert the digital information into a analogue format, which is then fed to the PA on the RF board.

The RM100 is a multi functional RFID reader and can be used to read any type of current available passive tags. Each type of tag uses different data rates and modulation index and it is up to the MCU to ensure that the correct mode is used to interrogate tags.

The MCU connects to the FPGA using a parallel interface to ensure fast data transfer between them. The MCU pass digital modulated data to the FPGA. The FPGA perform the necessary sloping the ensure that the transmit mask is minimized while still perform high data rates to the tag. Once data is received from the FPGA, the FPGA will then pass the received tag data to the MUC via the same parallel interface or bus interface.

The RM100 is using an AT command like protocol to communicate with a data terminal. This is only a 3 wire RS-232 interface and all the necessary operations may be controlled via this RS-232 link.

The MCU control 2 LED's that can be mounted on a faceplate or a front panel. The first LED is used to indicate the presents of a transmit carrier and/or modulated data. This LED will represent the activity of the transmitter section of the RF board. The second LED is used to indicate tag read activity. This LED will be active as long as tag data is received.

5.1.3 Digital Signal Processing

The Digital signal processing consists of an ADC and FPGA. The ADC is 12-BIT 20MSPS dual channel converter, which is used to convert the received in phase (I) and Quadrate phase (Q) signals to digital signals. The FPGA act like a state machine and perform more digital filtering and phase lock loops (PLL) to decode the received tag data correctly.

As mentioned before, the FPGA is also responsible for the modulated data by using a simple 8-bit R2R ladder and buffer.

5.2 RF board - RFM4411

The RF board can be divided into two sections namely:

1) Synthesiser
2) Power amplifier
3) Receiver
4) Base band filter

5.2.1 Synthesizer

The synthesizer is using a Jauch Crystal with a temperature stability of 10ppm over the temperature range -10ºC to +70ºC. This means that with a frequency of 915MHz, the carrier may drift ±10KHz

The RF output frequency is set by programming the R and N-Divider registers. The PLL has R and N registers so that each can be programmed independently. Programming either the R- or N-Divider register automatically selects the associated output.

The reference frequency at the VCO is divided by R and this signal is input to the PLL's phase detector. The other input to the phase detector is the PLL's VCO output frequency divided by N. The PLL acts to make these frequencies equal. Both the receiver and transmitter share a local oscillator drive to ensure that all signals are in phase with each other. The synthesiser is programmed by the CPU to hop between 902 and 928 MHz. The Synthesizer incorporates a phase lock loop as well as a local oscillator, with an output of –5dBm. This local oscillator frequency is then amplified by 15dB and then fed to an in-phase splitter. The splitter provides a +7dBm drive to the receiver board as well as to the transmitter main amplifier.

5.2.2 Power amplifier (PA)

The amplifier has 2 functions:

1) Amplify the RF signal to +30.5dBm
2) Act as an AM modulator by switching between two power levels.

The PA has 2 bias inputs, One is used to adjust output power levels and the other is used to change the AM modulation index

Lastly the PA output is fed via a harmonic low pass filter to the antenna connector.

5.2.3 Receiver

On the receiver circuit, the RF input is fed via a 902-928 band pass filter to the direct IQ demodulator. The demodulator uses the local oscillator to directly convert the received signals to base band signals. The IQ demodulator is also known as a homodyne or zero IF receiver.

5.2.4 Base band

The demodulator outputs Q and I base band signals. These signals are then fed to a 500 KHz 12dB per octave low pass filter and 2-stage amplifier. These signals are then passed to the differential Analogue to Digital converter described previously.

6. RF Channel Management

As mentioned previously, the RM100 is using 50 hopping channels, each with 500KHz channel spacing. These 50 channels are randomly generated every 20 seconds and placed into a list. Each channel is then active for 10 milliseconds before hopping to another channel. The MCU run through this list and make sure that within a 20 second, each channel doesn't occupy the spectrum for more than the allowable 400milliseconds.

See the 50 channel frequencies below

Channel #	Frequency MHz		Channel #	Frequency MHz
1	902.75		26	915.25
2	903.25		27	915.75
3	903.75		28	916.25
4	904.25		29	916.75
5	904.75		30	917.25
6	905.25		31	917.75
7	905.75		32	918.25
8	906.25		33	918.75
9	906.75		34	919.25
10	907.25		35	919.75
11	907.75		36	920.25
12	908.25		37	920.75
13	908.75		38	921.25
14	909.25		39	921.75
15	909.75		40	922.25
16	910.25		41	922.75
17	910.75		42	923.25
18	911.25		43	923.75
19	911.75		44	924.25
20	912.25		45	924.75
21	912.75		46	925.25
22	913.25		47	925.75
23	913.75		48	926.25
24	914.25		49	926.75
25	914.75		50	927.25

7. Internal frequencies

Two types of frequency components are present inside the RM100.

1) Crystal frequencies
2) Mixing

The FPGA is using a 16.384MHz Crystal oscillator and this frequency is multiplied by a factor of 5 by the PLL to 81.92Mhz, which is the clock speed of the FPGA

The MCU is using an 18.432Mhz Crystal. No other frequencies are generated inside the Digital board.

The RF synthesiser is using a 10MHz crystal to generate all the RF frequencies in the above table. See PLL/VCO description under section 6.2.1

On the RF board, the VCO generates the operating frequency of the transmitter directly. No intermediate frequencies are present. The same is with the receiver. The same VCO frequency is split to the receiver. As mentioned before, the receiver is a homodyne type receiver.

Care was taken to ensure the suppression of harmonic frequencies. The 2^{nd} and 3rd harmonic, generated by the VCO was present on the antenna ports. Two harmonic low pass filters were included to reduce these harmonic emissions to the desired level.

8. Specification

8.1 Performance

Frequency band	902-928MHz
Frequency stability	<10 ppm
RF Type	Frequency hopping spread spectrum
Channels	50
Occupied freq. Bandwidth	<250kHz
Transmitter power output	1W (30dBm) max. At antenna port
Hopping rate	>10mS
Modulation Type	Amplitude Modulation
Modulation Index	10 to 90% adjustable
Data rate to Tag	160kbps
Receiver RF input	0dBm max
Receiver sensitivity	<-60dBm
Serial port data rate	38400 bps
Serial port interface	RS232 (3 wire, no flow control)
Operating voltage	3.3Vdc to 4.2Vdc (Lithium-Ion battery)
Operating current	1.2A on read, 240mA on Idle
RF approval	FCC part 15.247

8.2 Physical

Height	17mm (max)
Length	103mm (max)
Width	69mm (max)
Weight	100 grams
Antenna ports	Reverse polarized SMA
Host interface	10 way male pin header (5 x 2)
Mounting	4 x 3mm mounting holes

8.3 Environment

Operating Temperature	-10ºC to +40ºC
Storage Temperature	-20ºC to +70ºC
Humidity	95% (non-condensing)
Shock	20Gs, 11ms, half sine pulse
ESD	+8KV(indirect), +4KV(direct)

■