INTEGRATED RADIO TRANSCEIVER

The BCM2042 has an integrated radio transceiver that has been optimized for use in 2.4-GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4-GHz unlicensed ISM band. It is fully compliant with Bluetooth Radio Specification v1.2 and meets or exceeds the requirements to provide the highest communication link quality of service.

TRANSMITTER PATH

The BCM2042 features a fully integrated zero IF transmitter. The baseband transmit data is digitally GFSK modulated in the modem block and up-converted to the 2.4-GHz ISM band in the transmitter path, which contains signal filters, an I/Q up-converter, an output power amplifier (PA), and RF filters.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Power Amplifier

The fully integrated PA provides a maximum output signal level of +4 dBm using a highly linearized, temperature compensated design. This gives the user greater flexibility in the type of front end matching and filtering to use with the BCM2042. Due to the linear nature of the PA combined with some integrated filtering, no external filters are required for meeting Bluetooth and regulatory harmonic and spurious requirements.

RECEIVER PATH

The receiver path uses a low IF scheme to down-convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high order on-chip channel filtering to ensure reliable operation in the noisy 2.4-GHz ISM band. The front end topology with built-in out-of-band attenuation enables the BCM2042 to be used in most applications with no off chip filtering.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the BCM2042 provides an Receiver Signal Strength Indicator (RSSI) signal to the baseband so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/sec) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The BCM2042 uses an internal RF and IF loop filter, which only requires one external capacitor.

Calibration

The BCM2042 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration, which accounts for process and temperature variations, optimizes the performance of all major circuit blocks within the radio. The gain and phase of all relevant filter blocks, amplifier blocks, and matching circuits are calibrated. Calibration occurs in the background during normal operation and during LO frequency hop setting times.

Internal Regulator

To reduce the external BOM, the BCM2042 has an integrated 1.5V Low Dropout (LDO) regulator to provide power to the digital and RF circuits. This regulator operates from a 1.7V to 3.6V input supply with less than 50 mV of maximum dropout voltage at full load.

A ferrite bead may be needed between the digital and RF supply pins to isolate noise coupling and suppress the noise into the RF circuits. For optimal performance, it is best to include a low-pass filter between the digital and RF supply pins; a pi filter circuit with two shunt caps and one 0603 ferrite bead will suffice. Figure 2 illustrates a sample LDO filter.

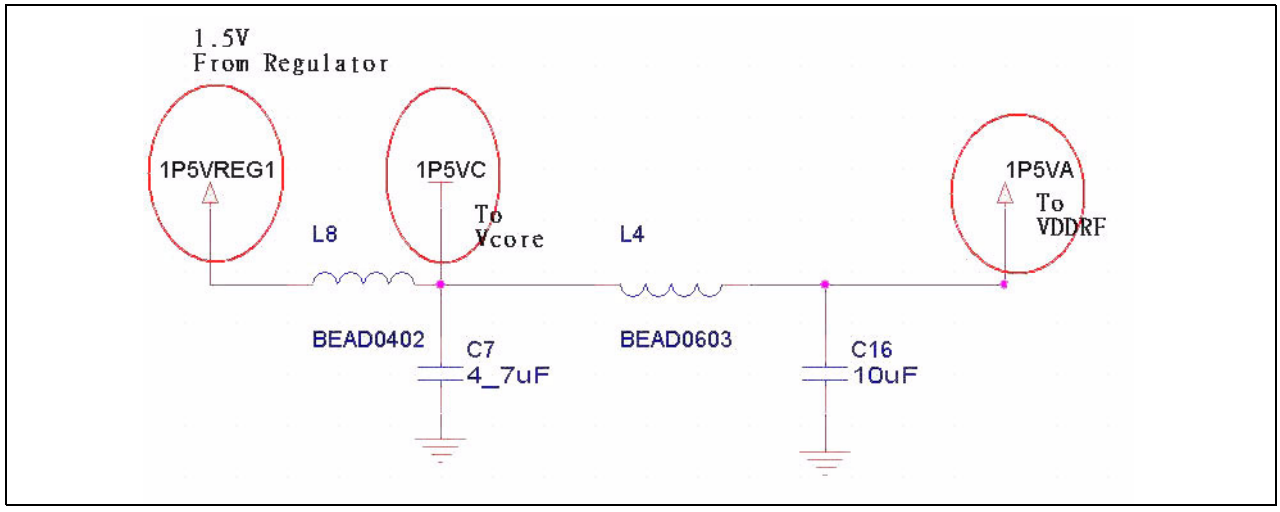

Figure 2: LDO Filter

MICROPROCESSOR UNIT

The Microprocessor Unit (µPU) runs software from the Link Control (LC) layer, up to the Host Controller Interface (HCI). The microprocessor is an enhanced performance 8051 microcontroller. The µPU also consists of one UART port, 2 KB of internal register RAM, 24 KB of internal SRAM, 112 KB of application ROM, and 16K of boot-ROM.

An external EEROM up to 32 KB in size may be connected to customize the operation of the BCM2042 for a particular application. The EEPROM may also contain patch-code to modify application behavior, or to fix any bugs which may exist in the ROM code.

The 8051 core is object code compatible with the industry standard 8051 microcontroller.

EXTERNAL MEMORY INTERFACE (120-PIN PACKAGE ONLY)

The memory interface (available only on the 120-pin package) allows 8051 microcontroller accesses to two types of 8-bit wide external memory: Flash memory and SRAM. The interface can access 128 KB (1 Mbit) of external Flash memory, 128 KB of external SRAM with no bank switching required, or access 256 KB (2 Mbit) of Flash without access to SRAM.

When using external Flash, 32 KB of the Flash may be used to contain configuration and patch-code, eliminating the need for an external EEPROM. When using a 256 KB (2 Mbit) or larger Flash, over-the-air firmware updates can be supported.

BLUETOOTH BASEBAND CORE

The Bluetooth Baseband Core (BBC) implements all of the time critical functions required for high performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules Asynchronous Connectionless Link TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Receive Functions: Symbol timing recovery, data de-framing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data de-whitening.
- Transmit Functions: Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening.

FREQUENCY HOPPING GENERATOR

The frequency hopping sequence generator selects the correct hopping channel number depending on the Link Controller state, Bluetooth clock, and the device address.

ENCRYPTION

The encryption key and the encryption engine are implemented using dedicated hardware to reduce software complexity and provide minimal intervention from the processor.

LINK CONTROL LAYER

The Link Control Layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the Link Control Unit (LCU). This layer consists of the Command Controller that takes commands from the software, and other controllers that are activated or configured by the Command Controller to perform the Link Control tasks. Each task performs a different state in the Bluetooth Link Controller. STANDBY and CONNECTION are the two major states. In addition, there are seven substates:

- PAGE
- PAGE SCAN
- INQUIRY
- INQUIRY SCAN
- PARK
- SNIFF
- HOLD

ADAPTIVE FREQUENCY HOPPING

The BCM2042 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency hop map.

FAST CONNECTION

The BCM2042 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 1.2 page and inquiry procedures and are designed to be forward compatible to Bluetooth version 1.2 extension fast connection mode.

BROADCOM SERIAL COMMUNICATIONS INTERFACE

The BCM2042 provides a 2-pin master Broadcom Serial Communications (BSC) interface which can be used to retrieve configuration information from an external EEPROM, or to communicate with peripherals such as track-ball or touch-pad modules, and motion tracking ICs used in mice. The BSC interface is compatible with I^2C slave devices. The BSC does not support multi-master capability or flexible wait-state insertion by either master or slave devices.

Listed below are the transfer clock rates supported by the BSC:

- 100 KHz
- 400 KHz
- 800 KHz[1]
- 1 MHz[2]

Listed below are the transfers supported by the BSC:

- Read (up to 8 bytes can be read)
- Write (up to 8 bytes can be written)
- Read-then-Write (up to 8 bytes can be read and up to 8 bytes can be written)
- Write-then-Read (up to 8 bytes can be written and up to 8 bytes can be read)

Transfers are performed under hardware control, requiring minimal setup and supervision by firmware.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins which are tolerant to inputs as high as 3.6V. Pull-up resistors external to the BCM2042 are required on both SCL and SDA for proper operation.

CLOCK FREQUENCIES

The BCM2042 is set with crystal frequency of 24 MHz. This default frequency may be modified by an external EEPROM or Flash. On boot-up the clock frequency is read from the EEPROM or Flash, and used to initiate device operation.

EXTERNAL CLOCK CONNECTION

The external clock signal may be connected to the XTAL IN pin on the BCM2042. If the external clock signal is connected to the XTAL IN pin, it is recommended that a 1000 pF DC blocking capacitor is used in series with the XTAL IN pin. Figure 3 illustrates the proper external clock connection. The amplitude of the external clock signal should be greater than 700mV p-p, but should not exceed VDD_RF.

Note: Any external clock used with the BCM2042 must be accurate to ± 20 ppm.

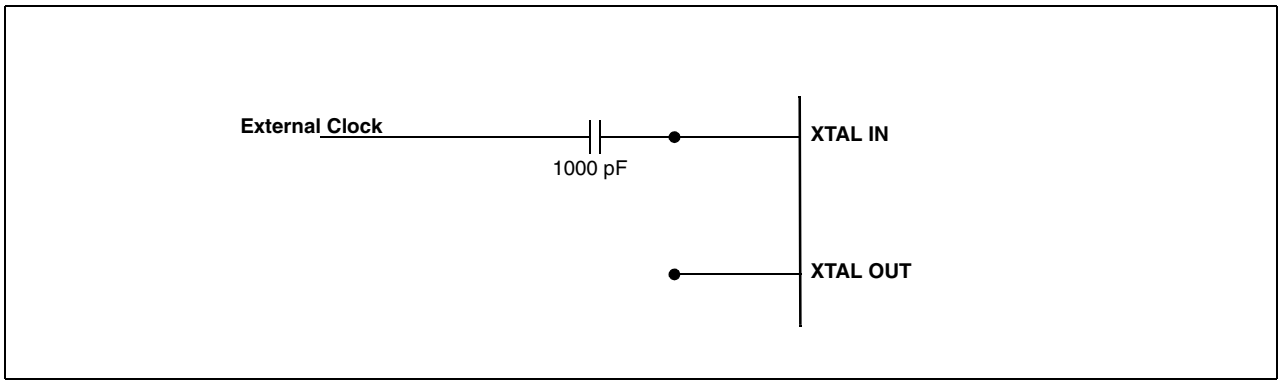

Figure 3: Recommended External Clock Connection

1. Not a standard I^2C-compatible speed.
2. Compatibility with high-speed I^2C-compatible devices is not guaranteed.

CRYSTAL OSCILLATOR

The crystal oscillator requires a crystal with an accuracy of ±20 ppm as defined by the Bluetooth specification. The crystal requires two external tuning capacitors. Refer to Figure 4 for the recommended configuration for crystals that present a 12 pF load. Refer to Figure 5 for the recommended configuration for crystals that present a 10 pF load. Refer to Table 1 for the recommended Crystal Oscillator specification.

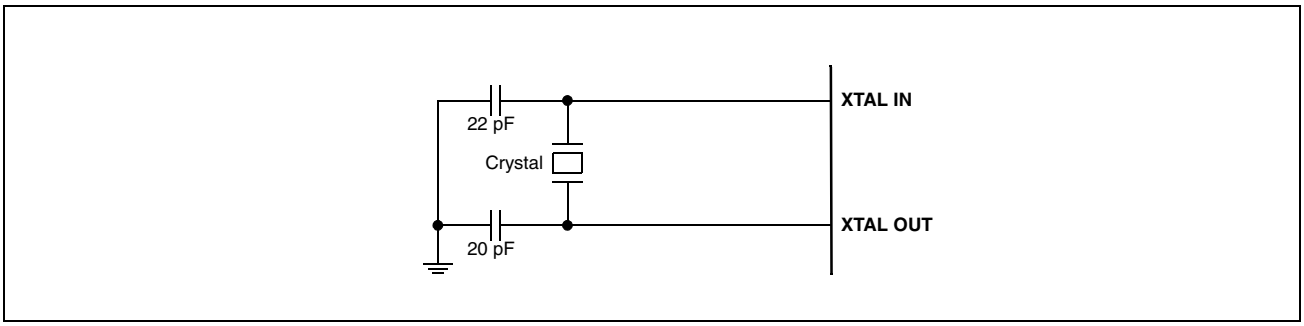

Figure 4: Recommended Oscillator Configuration – 12 pF Load Crystal

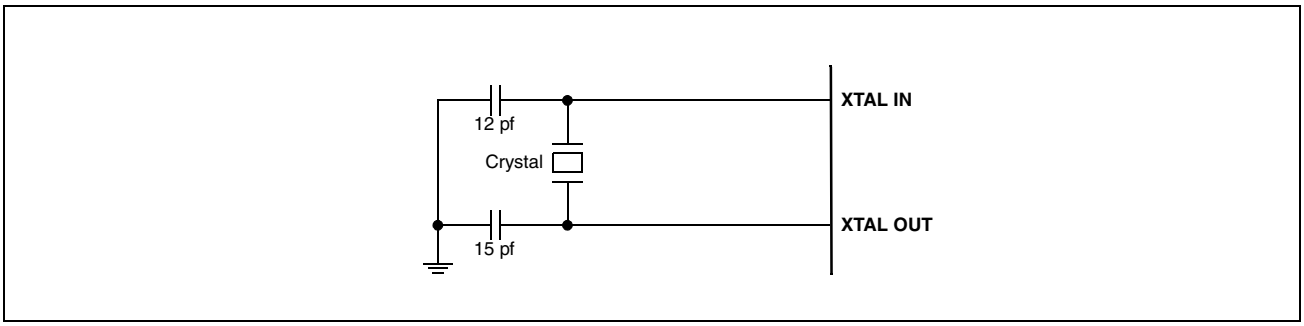

Figure 5: Recommended Oscillator Configuration – 10 pF Load Crystal

Table 1: Recommended Crystal Oscillator Specification

Parameter	***Value***
Tolerance	(+25^{o}C) 10 ppm
Temperature stability	10 ppm
Operating temperature range	–20^{o}C to +60^{o}C
ESR	100Ω
Drive level	10 uW (100 uW max.)
Storage temperature	–40^{o}C to +85^{o}C

GPIO PORT

The BCM2042 has a total of 36 General Purpose I/Os (GPIOs) in 88-pin, 100-pin, and 120-pin packages. All I/O are 3.3V tolerant, CMOS, push-pull, programmable pull-ups/pull-downs, programmable Schmitt trigger, programmable slew rate, and programmable drive strength. The GPIOs are grouped into five different ports.

The following describes the functions of each port.

PORT 0

P0[7:0] consists of eight pins. Each pin is bidirectional, and has 2 mA push-pull capability. All pins can be programmed to wake on change. Each pin can be individually configured as key-scan row input KSI[7:0]. The P0[7:2] can be configured as mouse quadrature inputs.

P0[1:0] can be programmed as input channels for the BCM2042 on-chip Analog-to-Digital Converter (ADC).

PORT 1

P1[7:0] consists of eight pins. Each pin is bidirectional, and has 2 mA push-pull capability. Each pin can be individually configured as key-scan column output (KSO).

P1[7:0] can be programmed as input channels for the BCM2042 on-chip ADC.

PORT 2

P2[7:0] consists of eight pins. Each pin is bidirectional, and has 2 mA push-pull capability. Each pin can be individually configured as KSO.

P2[5:4] are pulled down at reset, and can be reprogrammed by firmware post initialization.

P2[6:7] are pulled up at reset, and can be reprogrammed by firmware post initialization.

P2[7:0] can be programmed as input channels for the BCM2042 on-chip ADC.

PORT 3

P3[5:0] consists of six pins.

P3[1:0] each pin is open-drain bidirectional, and provides 2 mA push-pull capability. Each pin can be individually configured as KSO. Each pin will default to output LOW at reset if TMC=1, and can be reprogrammed by firmware post-initialization.

P3[3:2] can also be individually configured as key-scan column output.

P3[5:2] each pin is bidirectional, and provides 16 mA push-pull capability. Each pin can be configured as optics control for mouse quadrature signals. Each pin can also be configured as PWM control output signals.

P3[4:5] are pulled up at reset, and can be reprogrammed by firmware post initialization.

P3[4] for Class I applications, this GPIO can be programmed to control the external power amplifier ramping time.

P3[5:4] can be programmed as input channels for the BCM2042 on-chip ADC.

PORT 4

P4[5:0] each pin is bidirectional with 2 mA drive capability. Each pin can be configured as alternate mouse quadrature input. They can also be configured as quadrature input pair (e.g., scroll wheel or volume knob on keyboard).

P4[0] can be use for external regulator control if TMC=1: high for enable, low for disable at reset, and can be reprogrammed by firmware post initialization

P4[0] for Class I applications, this pin is programmed to enable/disable external power amplifier and T/R switch for receive mode.

P4[1] this pin is pulled down at reset. For Class I applications, it is programmed to control the external T/R switch for transmit mode.

P4[4] is pulled up at reset.

P4[5] is pulled down at reset.

P4[5:0] can be programmed as input channels for the BCM2042 on-chip ADC.

KEYBOARD SCANNER

The Keyboard Scanner is designed to autonomously sample keys and store them into buffer registers without the need for the host microcontroller to intervene.

The scanner has the following features:

- Ability to turn off its clock if no keys pressed
- Sequential scanning of up to 160 keys in an 8 x 20 matrix
- Programmable number of columns from 1 to 20
- Programmable number of rows from 1 to 8
- 16-byte key-code buffer (can be augmented by firmware)
- 128-KHz clock—allows scanning of full 152-key matrix in about 1.2 ms
- N-key roll-over with selective 2-key lockout if ghost is detected
- Keys are buffered until host microcontroller has a chance to read it, or until overflow occurs
- Hardware debouncing and noise/glitch filtering
- Low power consumption. Single-digit μA-level sleep current