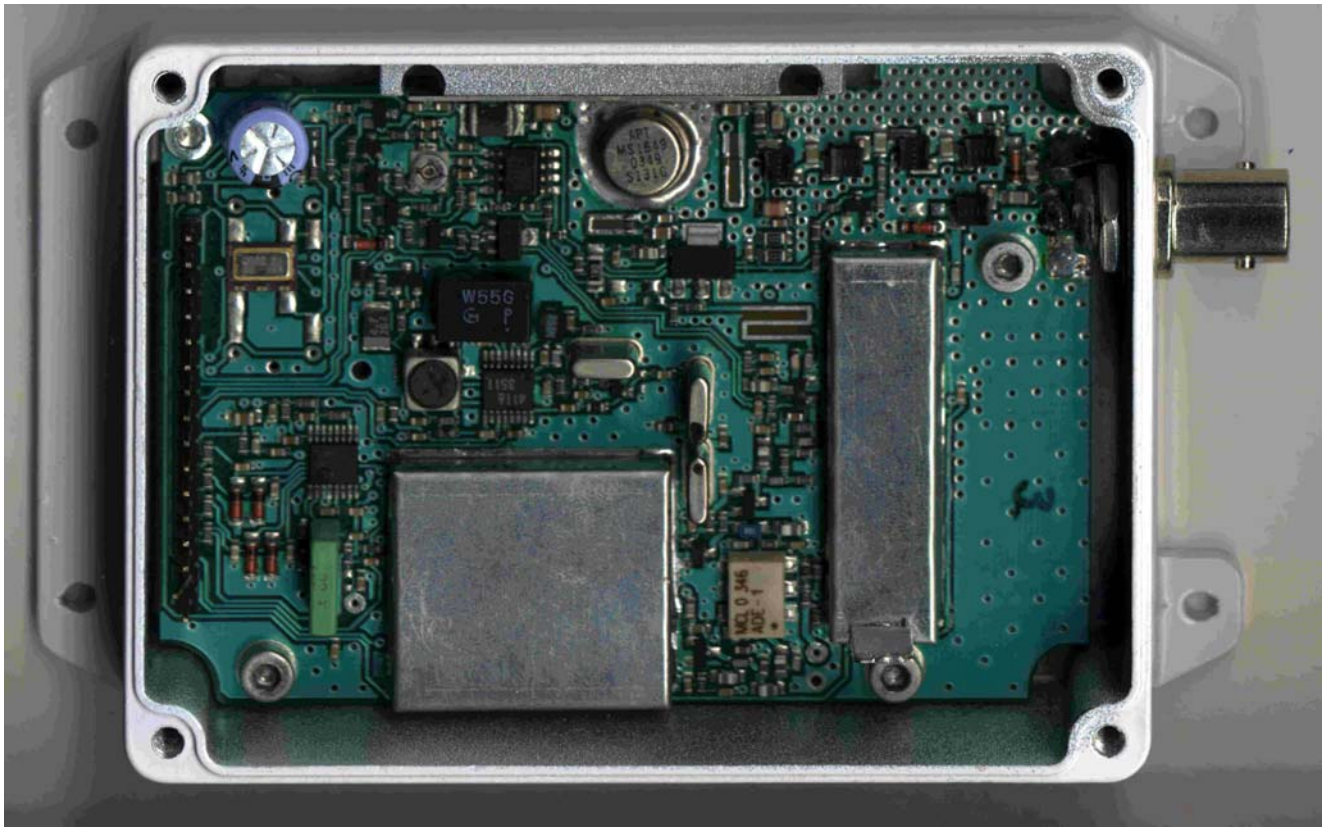
THEORY OF OPERATION



CIRCUITS on the RF- PCB

TRANSMITTER CIRCUITS:

- **BUFFER Amplifier**

VCO output level is approx. +1dBm and amplified to +23dBm by the buffer amplifier. The buffer consists of Q9,10 as a cascade and of Q11,17 between a resistive divider / R6,7,8 / for the required isolation and gain.

- **POWER AMPLIFIER**

The Power Amlifier is Q18. The amplifier amplifies the TX signal from +23 dBm to 2W **matched to 50 Ohms using a microstrip L and C105,110 network, thereby reducing the**

harmonics by -30 dB.

- **HARMONIC FILTER**

Chebyshev low pass filter. Unwanted harmonics are reduced by -70 dBc.

- **ANTENNA SWITCH**

When transmitting, the diodes D8 and D9 are forward biased to enable to make an RF path to the antenna. D9 is shorted to ground to block the RF signal to the front-end. In receive, the diodes, D8 and D9, are reverse biased to pass the signal from the antenna through L29 and C62 to the front-end without signal loss .

APC CIRCUIT

The APC (Automatic Power Control) circuit provides a stable power output.
Detector D10 rectifies the forward signals, and produces a d. c. level which is directly proportional to the RF output power level. The detected voltage is applied to pin 6 of amplifier IC4B. P1 sets d. c. voltage to the other input (pin 5) as a reference. This reference voltage is controlled by the MCU too (across Q5,R41). / High or Low power /
IC4B determines the RF power level by producing a difference signal. The difference signal is passed to Q16, Q22 to produce a constant power output by controlling the voltage supply rail to amplifier Q17. The required power output is set by adjusting P1. The output of IC4A adjusts Q11 basis bias, and set the required drive level characteristic in compliance with the transient behaviour of the transmitter.

PLL SYNTHESIZER :

- **12.8 MHz TCO**

The applied temperature compensated crystal oscillator offer excellent temperature characteristics with low power consumption and fast warmup. Compensation is ±2.5ppm or less from -30c to +60c.

- **PLL IC DUAL MODULES PRESCALER**

Input frequency of 12.8 MHz to IC1 LMX2316 pin 8 is divided to 6.25 kHz or 5 kHz by the reference counter, and then supplied to the comparator. RF signal input from VCO is divided to 32/33 at the prescaler in IC1, divided by A and N counter in IC1 to determine frequency steps, and then supplied to the comparator. PLL comparison frequency is 6.25/5kHz so that minimum programmable frequency step is 5/6.25 kHz.

The A and N counter is programmed to obtain the desired frequency by serial data in the MCU. In the comparator, the phase difference between reference and VCO signal is compared. The Charge Pump Output of IC1 connected to a loop filter for driving the input of the VCO.
Combined with a high quality reference oscillator and loop filter, the LMX2316 provide the feedback tuning voltage for a voltage controlled oscillator to generate a low phase noise local oscillator signal.

- **REFERENCE FREQUENCY LPF**

The Loop Filter contains R66,69,33, C97 and C100. LPF settling time is 12mS with 1 kHz frequency. This also reduces the residual side-band noise for the best signal-to-noise ratio.

- **VCO**

The VCO's operating frequency range can be switched by the D2 and D3 switching diodes according to the transmit or receive mode.
It is controlled by the MCU. The VCO is configured as a colpits Oscillator(Q6) . It's connected to the buffer, which a cascade amplifier /Q7,8/. The varicap diode D5 is a low-resistance element and produces a change in frequency with a change in reverse bias voltage (1-4,5V). L15 is a resonant coil, which changes the control voltage by the tuning core. The VCO is modulated by the audio signal through D6 modulation diode. By connecting to the VCO's tuning voltage, the circuit of R93,34,C139 compensates for the non-linearity of the VCO due to modulation diode, and maintains a constant modulation regardless of frequency.

RECEIVER

FRONT-END

The receive signal is routed backward through the low pass filter, then onward to the input of the Receiver Front End. It consists of a bandpass filter (C1 through C14, L 1 through L3) which is coupled to the base of Q1 which serves as an RF amplifier. Diode D1 serves as a protection from static RF overload from nearby transmitters. The output of Q1 is then coupled to a second bandpass filter consisting of C16 through C23 and L4 through L7. The output of Front End is then coupled to the double balanced mixer IC3.

FIRST MIXER

The double balanced mixer generates the 45 MHz intermediate frequency output from RF and local frequency. The 45MHz IF output is matched with the input of the 4-pole monolithic filter by L13, C124 and C101. The crystal filter provides a bandwidth of ±7.5 kHz at the operating frequency for a high degree of spurious and inter-modulation protection. The IF filter provides additional attenuation for the image frequency of the second mixer. The output impedance of the filter is matched with the base of the post amplifier Q12 by C115.

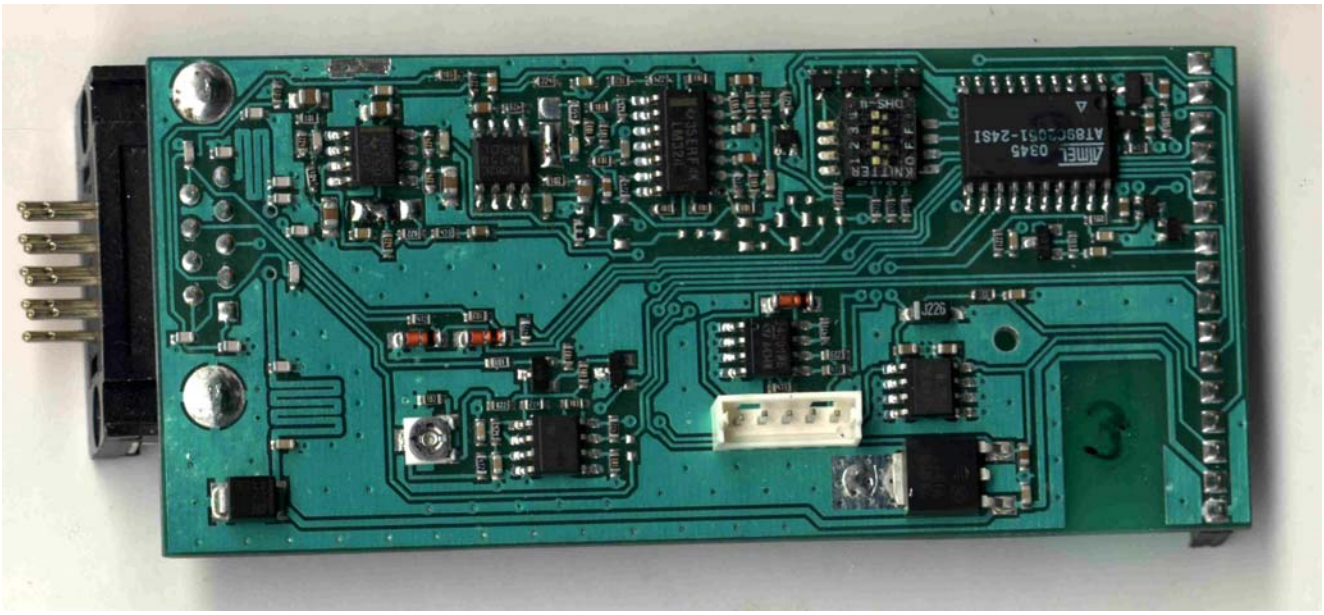
SECOND OSCILLATOR MIXER LIMITER AND FM DETECTOR

The output of the post filter amplifier, Q12, is coupled via C47 to the input of IC2 (BA4116). IC2 is a monolithic single conversion FM IF system, containing a mixer, the second local oscillator, limiter and quadrature detector. Crystal X2 / 44.545 MHz / is used to provide resultant 455kHz signal from the output of the second mixer. The mixer output is then routed to X1 (CFW455G). These ceramic filters provide the adjacent channel selectivity of 12,5 kHz bandwidth.

RSSI (RECEIVER SIGNAL STRENGTH INDICATOR)

The RSSI signal is output from IC2 on pin 12. As the receiver signals the output, DC voltage is varied as much as receiver signal strength.

CIRCUITS ON THE CONTROL-PCB



EEPROM

RX / TX channel and as well as other data from the programmer are stored in the EEPROM. The stored data is retained without power supply. This is a non-volatile and re-programmable memory. IC6 is an EEPROM with 4096 (8 x 128) capacity and data is written and read serially.

CHANNEL SELECTOR

One of 16 channels may be selected using the Dip Switch (IC9) and serial commands. The hardware selector, IC9 encodes the channel number, selected into 4-bit binary code. The binary code plus one equals the channel number. The binary code is decoded by the MCU, which enables the appropriate RX or TX frequency and associated data to be selected from the EEPROM. The external serial channel stepping command comes from Pin 9 of the DB-9 / J1/ connector and enhances the actual channel number by one.

MCU

The MCU(IC4) is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set.
The AT89C2051 is a low-voltage, high-performance CMOS 8-bit microcomputer with 2K bytes of Flash programmable and erasable read only memory (PEROM).
The IC5 (MCP130-450I/TT) reset circuit gives a standard reset impulse, which provides for the safe starting of the MCU. The IC4 gets its clock signal from the TCXO (X6) (which is on the RF-PCB), after the Q10 amplifies the signal to a level that is sufficent for the MCU.

TX-SIGNAL CIRCUIT

The audio signal from Pin 1 of DB-9 connector (J1) goes through IC406-C. The signal is amplified by IC10A and after it, there is a pre-emphasis circuit.(C12,R5) Then its amplitude is limited by IC1A. After that, this signal is filtered by an 6'th order low pass filter (IC1 B,C,D) in order to reduce the required transmission bandwidth. The output of the LPF is then fed to the RF board for TX modulation.

- **RX-SIGNAL CIRCUIT**

The Rx signal comes from the RF board, which is connected with pin 9 of JP1.
The audio signal is de-emphasized by resistor R38 and C30. After that, its level is amplified by IC2A. The amplified signal goes to pin 2 of J1 (DB-9).

RSSI (RECEIVER SIGNAL STRENGTH INDICATOR)

The RSSI signal is buffered by Q7,Q8 and goes to pin 8 of J1 (DB-9).

BUSY DETECT

The RSSI signal is compared by IC3A with d.c. level of P2. The BUSY DETECT signal appears on the IC3B output. This signal gets to the MCU /BUSY_IN/ and to the pin 6 of J1 (DB9). The BUSY DETECT level can be set by P2. The level is originally set so that the BUSY DETECT output changes at 20dB SINAD on the receiver output.