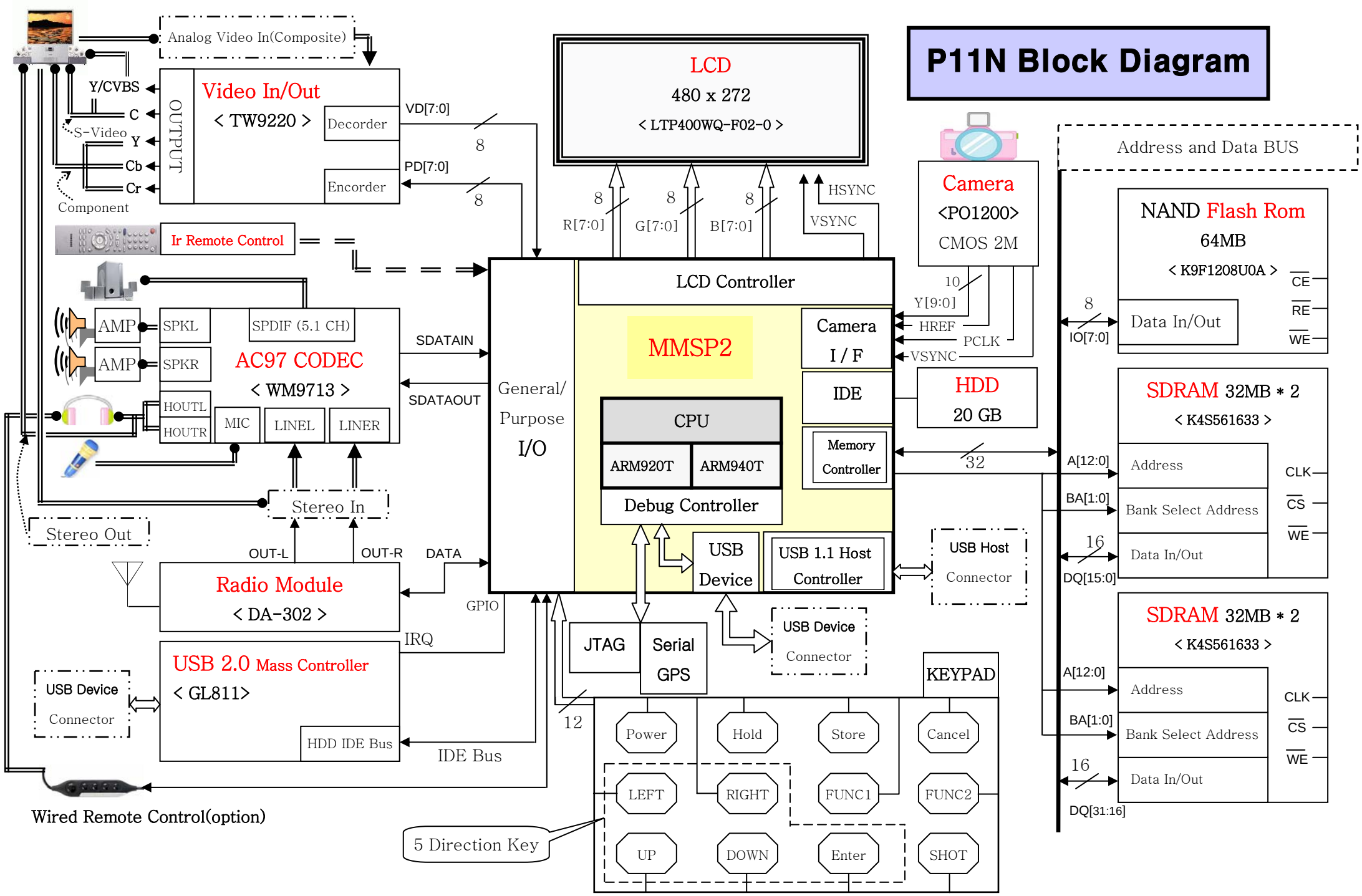
APPENDIX D

: BLOCK DIAGRAM


P11N Block Diagram
Analog Video In(Composite)
Y/CVBS
C
S-Video
Y
Cb
Cr
Component
OUTPUT
Video In/Out
< TW9220 >
Decorder
Encorder
VD[7:0]
PD[7:0]
8
8
LCD
480 x 272
< LTP400WQ-F02-0 >
8
R[7:0]
8
G[7:0]
8
B[7:0]
HSYNC
VSYNC
Camera
<PO1200>
CMOS 2M
10
Y[9:0]
HREF
PCLK
VSYNC
Address and Data BUS
NAND Flash Rom
64MB
< K9F1208U0A >
CE
RE
WE
8
IO[7:0]
Data In/Out
Ir Remote Control
AMP
AMP
SPKL
SPKR
SPDIF (5.1 CH)
AC97 CODEC
< WM9713 >
HOUTL
HOUTR
MIC
LINEL
LINER
SDATAIN
SDATAOUT
General/
Purpose
I/O
LCD Controller
MMSP2
Camera
I / F
IDE
HDD
20 GB
CPU
ARM920T
ARM940T
Debug Controller
Memory
Controller
32
SDRAM 32MB * 2
< K4S561633 >
A[12:0]
BA[1:0]
16
DQ[15:0]
Address
Bank Select Address
Data In/Out
CLK
CS
WE
Stereo In
Stereo Out
OUT-L
OUT-R
DATA
USB
Device
USB 1.1 Host
Controller
USB Host
Connector
Radio Module
< DA-302 >
GPIO
IRQ
USB 2.0 Mass Controller
< GL811>
HDD IDE Bus
IDE Bus
USB Device
Connector
JTAG
Serial
GPS
USB Device
Connector
12
KEYPAD
Power
Hold
Store
Cancel
LEFT
RIGHT
FUNC1
FUNC2
UP
DOWN
Enter
SHOT
5 Direction Key
Wired Remote Control(option)
SDRAM 32MB * 2
< K4S561633 >
A[12:0]
BA[1:0]
16
DQ[31:16]
Address
Bank Select Address
Data In/Out
CLK
CS
WE