BPP-UP100
Circuit Description

REVISED HISTORY

DATE	ISSUE	CONTENTS OF CHANGES	S/W VERSION
Semtember / 2004	ISSUE 0.1	Initial Release	

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* This manual provides the information necessary to install, program, operate and maintain the UP-100.

SECTION 1. PERFORMANCE

1.1 H/W Feature

Item	Feature	Comment
Phone size	Size : 105(L)x40(W)x15.8(T)	
Standard Battery	Li-ion, 720mAh Size: 4.5(T)x32(W)x53(L) mm Weight: 16g	
AVG TCVR Current	GSM850: 230mA, PCS: 180mA	
Standby Current	< 4.0mA	
Talk time	< 4 hours (GSM TX Level 7)	
Standby time	200 hours (Paging Period:2, RSSI: -85dBm)	
Charging time	2.5 hours	
RX Sensitivity	GSM850 : -107dBm, PCS : -106dBm	
TX output power	GSM850: 32.5dBm (Level 5) PCS1900: 29.5dBm (Level 0)	
GPRS compatibility	Class 10	
SIM card type	1.8V/3V Small	
Display	120 × 64 dots LCD	
Status Indicator	Soft icons Key Pad 0 ~ 9, #, *, Navigation Key, Menu Key, Send Key, END/PWR Key	
ANT	Internal	
EAR Phone Jack	3 pole earphone jack	
PC Synchronization	Yes	
Speech coding	EFR/FR	
Data and Fax	Yes	
Vibrator	Yes	
Buzzer	Yes	
Voice Recoding	No	
C-Mike	Yes	
Receiver	Yes	
Travel Adapter	Yes	
Options	No	

1.2 Technical Specification

<table>
<tr><td>Item</td><td>Description</td><td>Specification</td></tr>
<tr><td>1</td><td>Frequency Band</td><td>GSM 850 TX : 824 – 849 MHz
GSM 850 RX : 869 – 894 MHz
PCS 1900 TX : 1850 – 1910 MHz
PCS 1900 RX : 1930 – 1990 MHz</td></tr>
<tr><td>2</td><td>Phase Error</td><td>RMS < 5 degrees
Peak < 20 degrees</td></tr>
<tr><td>3</td><td>Frequency Error</td><td>< 0.1ppm</td></tr>
<tr><td>4</td><td>Power Level</td><td>
GSM850
<table>
<tr><td>Level</td><td>Power</td><td>Toler.</td><td>Level</td><td>Power</td><td>Toler.</td></tr>
<tr><td>5</td><td>33 dBm</td><td>±2dB</td><td>13</td><td>17 dBm</td><td>±3dB</td></tr>
<tr><td>6</td><td>31 dBm</td><td>±3dB</td><td>14</td><td>15 dBm</td><td>±3dB</td></tr>
<tr><td>7</td><td>29 dBm</td><td>±3dB</td><td>15</td><td>13 dBm</td><td>±3dB</td></tr>
<tr><td>8</td><td>27 dBm</td><td>±3dB</td><td>16</td><td>11 dBm</td><td>±5dB</td></tr>
<tr><td>9</td><td>25 dBm</td><td>±3dB</td><td>17</td><td>9 dBm</td><td>±5dB</td></tr>
<tr><td>10</td><td>23 dBm</td><td>±3dB</td><td>18</td><td>7 dBm</td><td>±5dB</td></tr>
<tr><td>11</td><td>21 dBm</td><td>±3dB</td><td>19</td><td>5 dBm</td><td>±5dB</td></tr>
<tr><td>12</td><td>19 dBm</td><td>±3dB</td><td></td><td></td><td></td></tr>
</table>
PCS
<table>
<tr><td>Level</td><td>Power</td><td>Toler.</td><td>Level</td><td>Power</td><td>Toler.</td></tr>
<tr><td>0</td><td>30 dBm</td><td>±2dB</td><td>8</td><td>14 dBm</td><td>±3dB</td></tr>
<tr><td>1</td><td>28 dBm</td><td>±3dB</td><td>9</td><td>12 dBm</td><td>±4dB</td></tr>
<tr><td>2</td><td>26 dBm</td><td>±3dB</td><td>10</td><td>10 dBm</td><td>±4dB</td></tr>
<tr><td>3</td><td>24 dBm</td><td>±3dB</td><td>11</td><td>8 dBm</td><td>±4dB</td></tr>
<tr><td>4</td><td>22 dBm</td><td>±3dB</td><td>12</td><td>6 dBm</td><td>±4dB</td></tr>
<tr><td>5</td><td>20 dBm</td><td>±3dB</td><td>13</td><td>4 dBm</td><td>±4dB</td></tr>
<tr><td>6</td><td>18 dBm</td><td>±3dB</td><td>14</td><td>2 dBm</td><td>±5dB</td></tr>
<tr><td>7</td><td>16 dBm</td><td>±3dB</td><td>15</td><td>0 dBm</td><td>±5dB</td></tr>
</table>
</td></tr>
</table>

5	Output RF Spectrum (due to modulation)	GSM850	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600 ~ 1,200	-60
		1,200 ~ 1,800	-60
		1,800 ~ 3,000	-63
		3,000 ~ 6,000	-65
		6,000	-71
		PCS	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600 ~ 1,200	-60
		1,200 ~ 1,800	-60
		1,800 ~ 3,000	-65
		3,000 ~ 6,000	-65
		6,000	-73
6	Output RF Spectrum (due to switching transient)	GSM850	
		Offset from Carrier (kHz)	Max. (dBm)
		400	-19
		600	-21
		1,200	-21
		1,800	-24
		PCS	
		Offset from Carrier (kHz)	Max. (dBm)
		400	-22
		600	-24
		1,200	-24
		1,800	-27

<table>
<tr><td>7</td><td>Spurious Emissions</td><td colspan="3">Conduction, Emission Status
Conduction, Emission Status</td></tr>
<tr><td>8</td><td>Bit Error Ratio</td><td colspan="3">GSM850
BER (Class II) < 2.439% @-102dBm
PCS
BER (Class II) < 2.439% @-100dBm</td></tr>
<tr><td>9</td><td>Rx Level Report accuracy</td><td colspan="3">± 3 dB</td></tr>
<tr><td>10</td><td>SLR</td><td colspan="3">8 ± 3 dB</td></tr>
<tr><td rowspan="10">11</td><td rowspan="10">Sending Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>/</td></tr>
<tr><td>200</td><td>0</td><td>/</td></tr>
<tr><td>300</td><td>0</td><td>-12</td></tr>
<tr><td>1,000</td><td>0</td><td>-6</td></tr>
<tr><td>2,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,400</td><td>4</td><td>-9</td></tr>
<tr><td>4,000</td><td>0</td><td>/</td></tr>
<tr><td>12</td><td>RLR</td><td colspan="3">2 ± 3 dB</td></tr>
<tr><td rowspan="12">13</td><td rowspan="12">Receiving Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>/</td></tr>
<tr><td>200</td><td>0</td><td>/</td></tr>
<tr><td>300</td><td>2</td><td>-7</td></tr>
<tr><td>500</td><td>*</td><td>-5</td></tr>
<tr><td>1,000</td><td>0</td><td>-5</td></tr>
<tr><td>3,000</td><td>2</td><td>-5</td></tr>
<tr><td>3,400</td><td>2</td><td>-10</td></tr>
<tr><td>4,000</td><td>2</td><td></td></tr>
<tr><td colspan="3">* Mean that Adopt a straight line in between 300 Hz and 1,000 Hz to be Max. level in the range.</td></tr>
<tr><td>14</td><td>STMR</td><td colspan="3">13 ± 5 dB</td></tr>
<tr><td>15</td><td>Stability Margin</td><td colspan="3">> 6 dB</td></tr>
<tr><td rowspan="8">16</td><td rowspan="8">Distortion</td><td colspan="2">dB to ARL (dB)</td><td>Level Ratio (dB)</td></tr>
<tr><td colspan="2">-35</td><td>17.5</td></tr>
<tr><td colspan="2">-30</td><td>22.5</td></tr>
<tr><td colspan="2">-20</td><td>30.7</td></tr>
<tr><td colspan="2">-10</td><td>33.3</td></tr>
<tr><td colspan="2">0</td><td>33.7</td></tr>
<tr><td colspan="2">7</td><td>31.7</td></tr>
<tr><td colspan="2">10</td><td>25.5</td></tr>
<tr><td>17</td><td>Side tone Distortion</td><td colspan="3">Three stage distortion < 10%</td></tr>
<tr><td>18</td><td><Change> System frequency (26 MHz) tolerance</td><td colspan="3">≤ 2.5 ppm</td></tr>
</table>

<table>
<tr><td>19</td><td><Change>32.768KHz tolerance</td><td colspan="2">≤ 30ppm</td></tr>
<tr><td>20</td><td>Power consumption</td><td colspan="2">Full power
< 250mA (GSM850) ; < 200mA (PCS)
Standby
- Normal Mode ≤ 4.0mA(Mix. power)
- Using Test mode on DSP Sleep function ≤ 6mA</td></tr>
<tr><td>21</td><td>Talk Time</td><td colspan="2">GSM850/Level 7 (Battery Capacity 720mA):1800 Min
GSM850/Level 12(Battery Capacity720:250 Min</td></tr>
<tr><td>22</td><td>Standby Time</td><td colspan="2">Under conditions, at least 200 hours:
1. Brand new and full 740mAh battery
2. Full charge, no receive/send and keep GSM in idle mode.
3. Broadcast set off.
4. Signal strength display set at 3 level above.
5. Backlight of phone set off.</td></tr>
<tr><td>23</td><td>Ringer Volume</td><td colspan="2">At least 80 dB under below conditions:
1. Ringer set as ringer.
2. Test distance set as 50 cm</td></tr>
<tr><td>24</td><td>Charge Voltage</td><td colspan="2">Fast Charge : < 500 mA
Slow Charge: < 60 mA</td></tr>
<tr><td rowspan="7">25</td><td rowspan="7">Antenna Display</td><td>Antenna Bar Number</td><td>Power</td></tr>
<tr><td>5</td><td>-85 dBm ~</td></tr>
<tr><td>4</td><td>-90 dBm ~ –86 dBm</td></tr>
<tr><td>3</td><td>-95 dBm ~ –91 dBm</td></tr>
<tr><td>2</td><td>-100 dBm ~ –96 dBm</td></tr>
<tr><td>1</td><td>-105 dBm ~ –101 dBm</td></tr>
<tr><td>0</td><td>~ –105 dBm</td></tr>
<tr><td rowspan="6">26</td><td rowspan="6">Battery Indicator</td><td>Batter Bar Number</td><td>Voltage</td></tr>
<tr><td>0</td><td>~ 3.62 V</td></tr>
<tr><td>1</td><td>3.62 ~ 3.71 V</td></tr>
<tr><td>2</td><td>3.72 ~ 3.78 V</td></tr>
<tr><td>3</td><td>3.79 ~3.92V</td></tr>
<tr><td>4</td><td>3.93~4.2V</td></tr>
<tr><td rowspan="2">27</td><td rowspan="2">Low Voltage Warning</td><td colspan="2">3.35~3.60 V (Call)</td></tr>
<tr><td colspan="2">3.35~3.50V (Standby)</td></tr>
<tr><td>28</td><td>Forced shut down Voltage</td><td colspan="2">3.35 ± 0.03 V</td></tr>
<tr><td>29</td><td>Battery Type</td><td colspan="2">1 Li-ion Battery
Standard Voltage = 3.8 V
Battery full charge voltage = 4.2 V
Capacity: 720mAh</td></tr>
<tr><td>30</td><td>Travel Charger</td><td colspan="2">Switching-mode charger
Input: 100 ~ 240 V, 50/60Hz
Out put: 5.2V, 600mA</td></tr>
</table>

SECTION 2. TECHNICAL BRIEF

2.1 General Description

The RF parts consist of a transmitter part, a receiver part, a frequency synthesizer part and a VCTCXO part.

The TexasInstuments transceiver is composed of one RF chipset TRF6151C which is a quadruple-band GSM/GPRS wireless communications. This device integrates a receiver based on direct conversion architecture, a transmitter based on modulation-loop architecture, frequency synthesizing including a 26-MHzVCXO, a main N-integer synthesizer, two main VCOs, a programmable main-loop filter, two TX VCOs, a TX loop filter, voltage regulators to supply on-chip and off-chip RF functions, and a power-amplifier controller.

2.2 Receiver Part

A. RF Front End

RF front end consists of FEMU101), dual band LNAs integrated in transceiver

The Received RF signals(GSM 869MHz ~ 894MHz, PCS 1930MHz ~ 1990MHz) are fed into the antenna or mobile switch. An antenna matching circuit is between the antenna and the mobile switch. The Antenna Switch is used for control the Rx and Tx paths. And, the input signals VC1 and VC2 of a U101, 1 are directly connected to baseband controller to switch either Tx or Rx path on. Ant S/W module(U101) is an antenna switch module for dual band phone.

The logic and current is given below **Table 1.**

Table 1 The Logic and Current

	VC1	VC2	Current
GSM TX	2.4 ~ 2.8 V	.0 V	8.0 mA max
PCS TX	0 V	2.4 ~ 2.8 V	8.0 mA max
GSM/PCS RX	0 V	0 V	< 0.1 mA

B. Transceiver

Receive section:

-- A GSM850 LNA (LNAGSM) with switchable gain

-- A PCS1900 LNA (LNAPCS) with switchable gain

-- Demodulators for GSM850 (MIXGSM), PCS1900 (MIXPCS) bands with programmable gain

-- Two baseband amplifiers with digitally-programmable gain

-- Two fully-integrated baseband channel filters

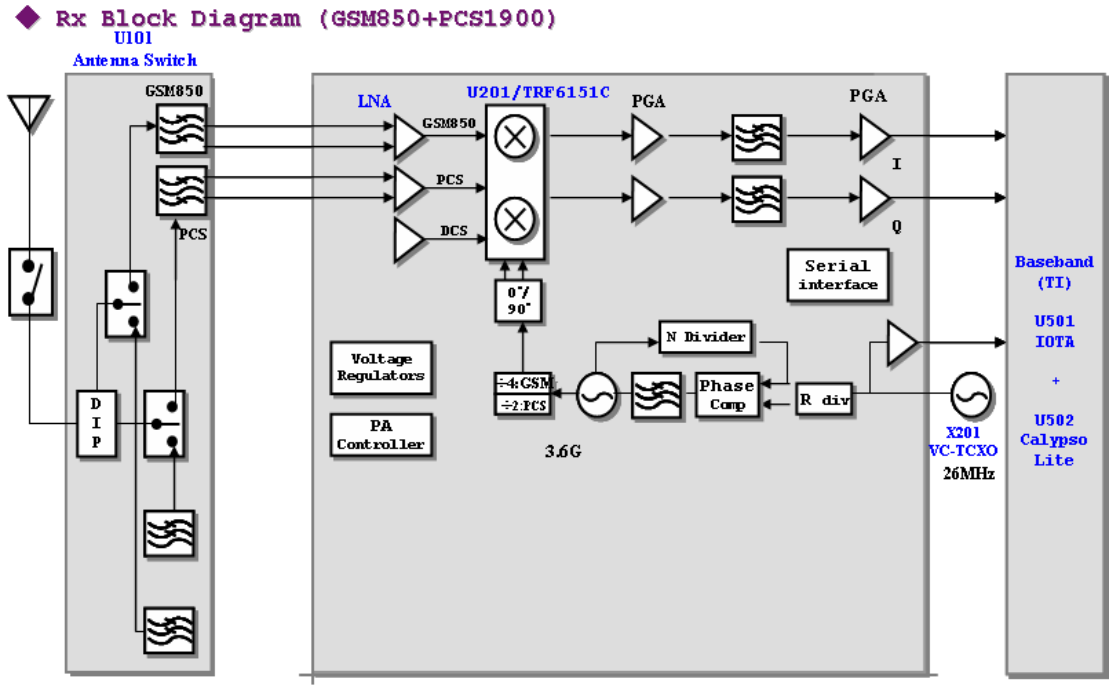
-- Two dc-offset compensation systems

-- A divider by 4 for LO generation in GSM850 in order to minimize dc offset generated by self- mixing and the LO reradiation

-- A divider by 2 for LO generation in PCS1900 in order to minimize dc offset generated by self-mixing and LO reradiation.

Figure 1 Receiver Part Block Diagram

◆ RF Block Diagram (GSM850+PCS1900)



2.3 Synthesizer Part

-- A 26-MHz VCXO with external

-- A 26-MHz buffer to drive the DBBs

-- Two main VCOs fully integrated

-- A main N-integer synthesizer

-- A programmable main loop filter

-- Three voltage regulators to supply

-- A digital serial interface

2.4 Transmitter Part

A. Transceiver

Transmit section:

-- An offset PLL with post-IQ modulator and post-offset mixer filters fully integrated on the chip

-- Two TX VCOs fully integrated on the chip

-- A TX loop filter fully integrated on the chip

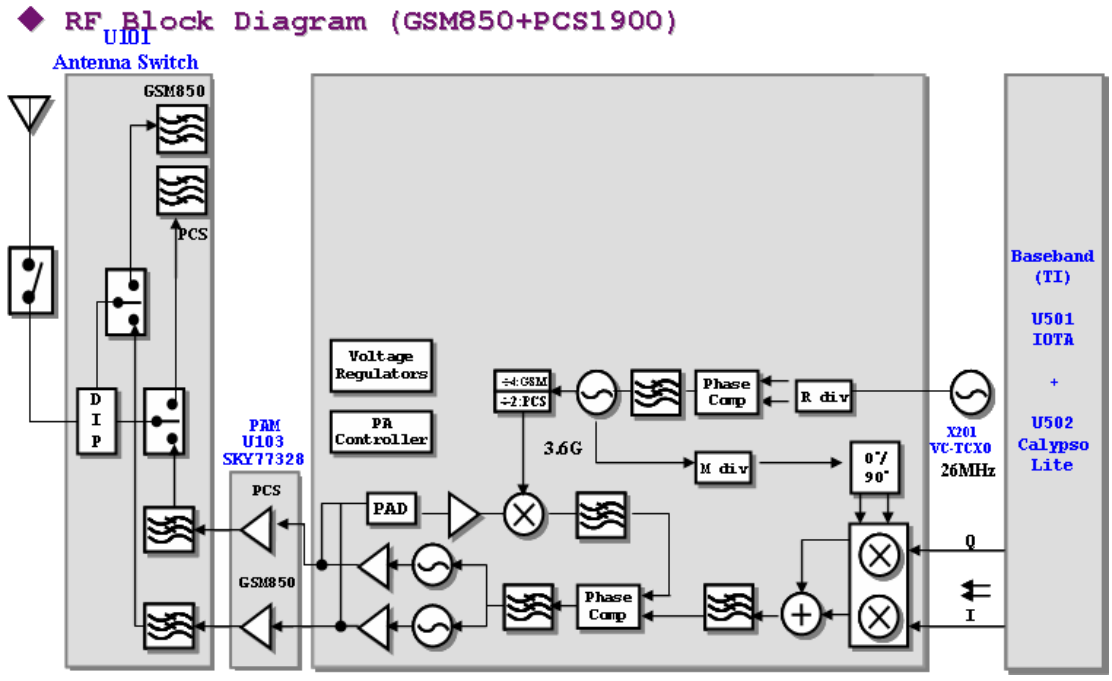
-- A divider by 4 for local oscillator (LO) generation in GSM850 and GSM850

-- A divider by 2 for LO generation in PCS1800 and PCS1900

-- A programmable M divider for IF generation

-- A power-amplifier controller including all the functions required to design a power-sensing control loop, except for the sensing diodes

Figure 2 Transmitter Block Diagram



B. Power Amplifier

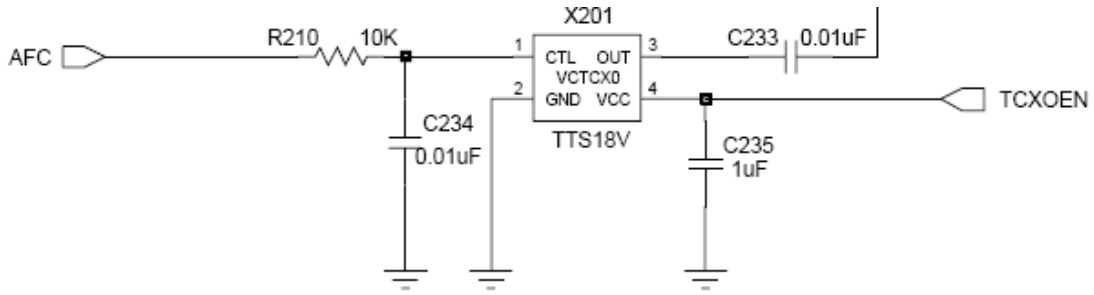
The SKY77328[U103] is a high-power, high-efficiency power amplifier module with integrated power control. The device is a self-contained 7mmx7mmx0.9mm lead frame module(LFM) with 50Ω input

and output terminals. The power control function is also incorporated, eliminating the need for directional couplers, detector diodes, power control ASICs and other power control circuitry; this allows the module to be driven directly from the DAC output. The device is designed for use as the final RF amplifier in GSM850, EGSM850, PCS and PCS handheld digital cellular equipment and other applications in the 824MHz to 849MHz, 880MHz to 915MHz, 1710MHz to 1785MHz and 1850MHz to 1910MHz bands.

2.5 26 MHz Clock

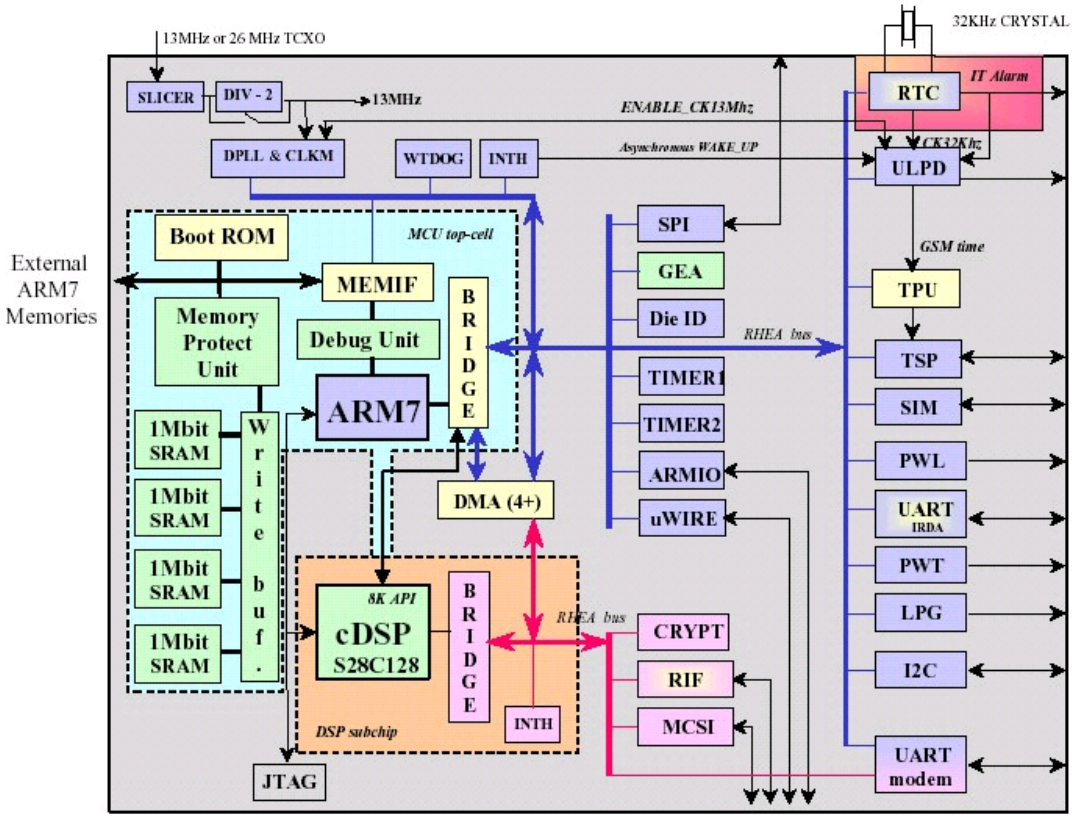
The 26 MHz clock(X201) consists of a TCXO(Temperature Compensated Crystal Oscillator) which oscillates at a frequency of 13 MHz. It is used within the TRF6151C RF Main Chip, BB Analog chip-set(IOTA), Digital chip-set(Calypso Lite).

Figure 5 VCTCXO Circuit



2.7 Digital Baseband(DBB) Processor

Figure 7 Top level block diagram of the Calypso G2(HERCROM400G2)



A. General Description

CALYPSO is a chip implementing the digital base-band processes of a GSM/GPRS mobile phone. This chip combines a DSP sub-chip (LEAD2 CPU) with its program and data memories, a Micro--Controller core with emulation facilities (ARM7TDMIE), internal 8Kb of Boot ROM memory, 4M bit SRAM memory, a clock squarer cell, several compiled single-port or 2-ports RAM and CMOS gates. The chip will fully support the Full-Rate, Enhanced Full-Rate and Half-Rate speech coding. CALYPSO implements all features for the structural test of the logic (full-SCAN, BIST, PMT, JTAG boundary-SCAN).

B. Block Description

CALYPSO architecture is based on two processor cores ARM7 and DSP using the generic RHEA bus standard as interface with their associated application peripherals.

CALYPSO is composed from the following blocks:

- ARM7TDMIE : ARM7TDMI CPU core
- DSP subchip
- ARM peripherals:

General purpose peripherals

- ARM Memory Interface for external RAM, Flash or ROM
- 4 Mbit Static RAM with write-buffer

Application peripherals

- ARM General purposes I/O with keyboard interface and two PWM modulation signals
- UART 16C750 interface (UART_IRDA) with
  - IRDA control capabilities (SIR)
  - Software flow control (UART mode).
- UART 16C750 interface (UART_MODEM) with
  - hardware flow protocol (DCD, CTS/RTS)
  - autobaud function
- SIM Interface.
- TPU(Time Processing Unit) : Processing for GSM time base
- TSP(Time Serial Port) : GSM data interface with RF and ABB

Memory Interface : External/Internal Memory Interface

nCS0 : FLASH1, 16bit access, 3 wait state

nCS1 : FLAHS2, 16bit access, 3 wait state

nCS2 : Ext SRAM, 16bit access, 3 wait state

nCS3 : Main LCD(16bit access), OEL(8bit access) addressing, 3 wait state (See Fig 3-11)

nCS4 : MIDI(8bit access), USB(8bit access) addressing, 3 wait state (See Fig 3-12)

nCS6 : Int SRAM, 32bit access, 0 wait state

* Calypso is internally 39MHz machine (25ns machine cycle), so it requires 3 wait-state for 80ns access(25*4 = 100 ns).

C. External Devices connected to memory interface

Table 2 External Device Spec. connected to memory interface

Interface SPEC					
Device	**Name**	**Maker**	**Write Access Time**	**Read Access Time**	
FLASH 1	TH50VPF5683CDSB	Toshiba	70ns	70ns	
SRAM	TH50VPF5683CDSB	Toshiba	70ns	70ns	
MAIN LCD	RB187Z10A	SII	50ns	50ns	
Melody IC	YMU762	Yamaha	50ns	80ns	

D. RF Interface (TPU, TSP block)

Calypso uses this interface to control Nausica_CS(ABB Processor) and Clara(RF Processor) with GSM Time Base

Table 3 RF Interface Spec.

TSP (Time Serial Port)		
Resource	**Interconnection**	**Description**
TSPDO	ABB & RF main Chip	Control Data
TSPEN0	ABB	ABB Control Data Enable Signal
TSPEN1	RF main Chip	RF Control Data Enable Signal
TPU (Time Processing Unit) Parallel Port		
TSPACT00	RESET_RF	RF main Chip Reset Signal
TSPACT05	PA_ON	Power Amp ON signal

E. SIM interface

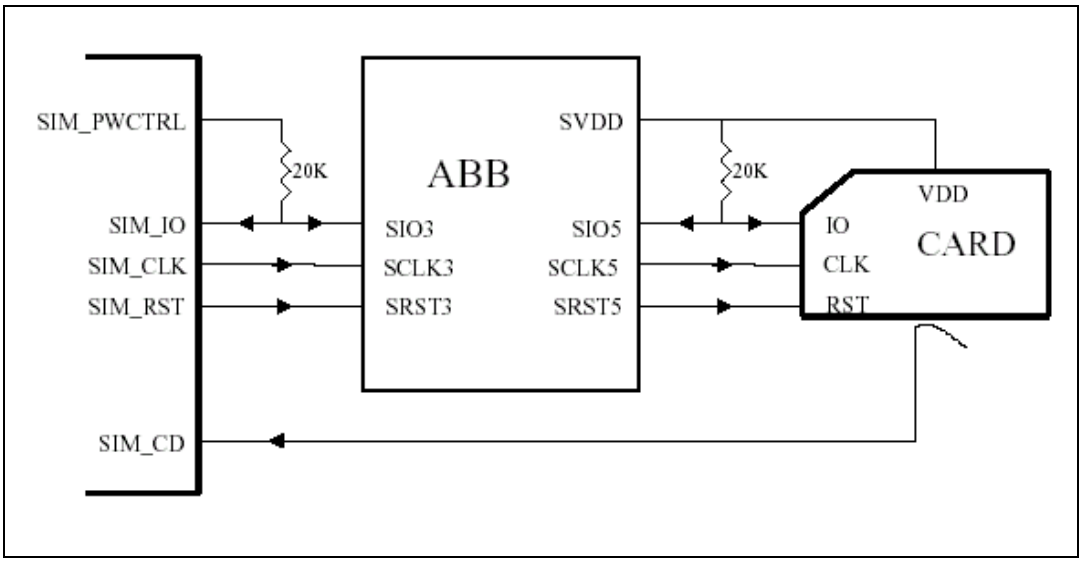
SIM interface scheme is shown in (Figure 10).

SIM_IO, SIM_CLK, SIM_RST ports are used to communicate DBB with ABB and the Charge Pump in ABB enables 1.8V/3V SIM operation

SIM Interface

SIM_CLK SIM card reference clock
SIM_RST SIM card async/sync reset
SIM_IO SIM card bidirectional data line
SIM_PWCTRL SIM card power activation
SIM_RnW SIM card data line direction
SIM_CD SIM card presence detection

Figure.10 SIM Interface



F. GPIO map

In total 16 allowable resources, UP-100 is using 13 resources except 3 resources dedicated to SIM and Memory. UP-100 GPIO(General Purpose Input/Output) Map, describing application, I/O state, and enable level, is shown in below table.

Table .4 GPIO Map Table

I/O #	Application	I/O	Resource State	Inactive State	Active State
I/O (0)	DSR	I	GPIO	HIGH (Open)	LOW (Closed)
I/O (1)	LCD_BACKLIGHT	O	GPIO	HIGH	LOW
I/O (2)	NC		GPIO	LOW	HIGH
I/O (3)	NC		GPIO	HIGH	LOW
I/O (4)	LED_ON		GPIO		
I/O (5)	SIM_PWCTRL	O	SIM	HIGH	HIGH
I/O (6)	EN_VIB	O	GPIO	LOW	HIGH
I/O (7)	LCD_RESET	O	GPIO	HIGH	LOW
I/O (8)	NC		GPIO	LOW	HIGH
I/O (9)	PCM TX	O	GPIO	HIGH	LOW
I/O (10)	PCM RX	O	GPIO	LOW	HIGH
I/O (11)	PCM CLK	O	GPIO	LOW	HIGH
I/O (12)	PCM_SYNC	O	GPIO	HIGH	LOW
I/O (13)	AMP_SHDN	O	GPIO	HIGH	LOW
I/O (14)	BHE	O	MEMORY		
I/O (15)	BLE	O	MEMORY		

2.8 Analog Baseband(ABB) Processor

A. General Description

IOTA is Analog Baseband (ABB)Chip supports GSM850, PCS1800, PCS, GPRS Class 10 with Digital Basband Chip(Calypso G2).

IOTA processes GSM modulation/demodulation and power management operations.

Block Description

- Audio Signal Processing & Interface
- Baseband in-phase(I), quadrature(Q) Signal Processing
- RF interface with DBB (time serial port)
- Supply voltage regulation
- Battery charging control
- Switch ON/OFF
- 1.8V/3V SIM card Interface
- 4 internal & 4external ADC channels

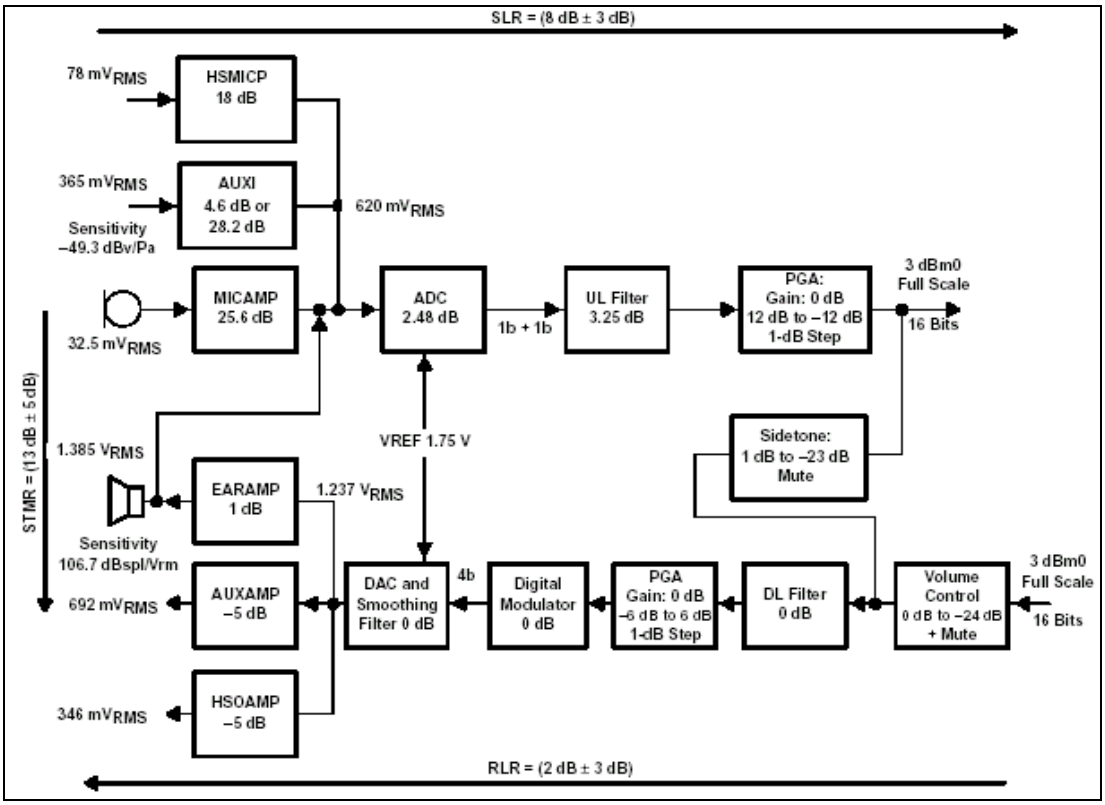
B. Audio Signal Processing & Interface

Audio signal processing is divided Uplink path and downlink path..

The uplink path amplifies the audio signal from MIC and converts this analog signal to digital signal and then transmit it to DBB Chip. This transmitted signal is reformed to fit in GSM Frame format and delivered to RF Chip. MICBIAS is 2.0Vlevel.

The downlink path amplifies the signal from DBB chip and outputs it to Receiver(or Speaker).

Figure11 Audio Interface Block Diagram



C. Baseband Codec(BBC)

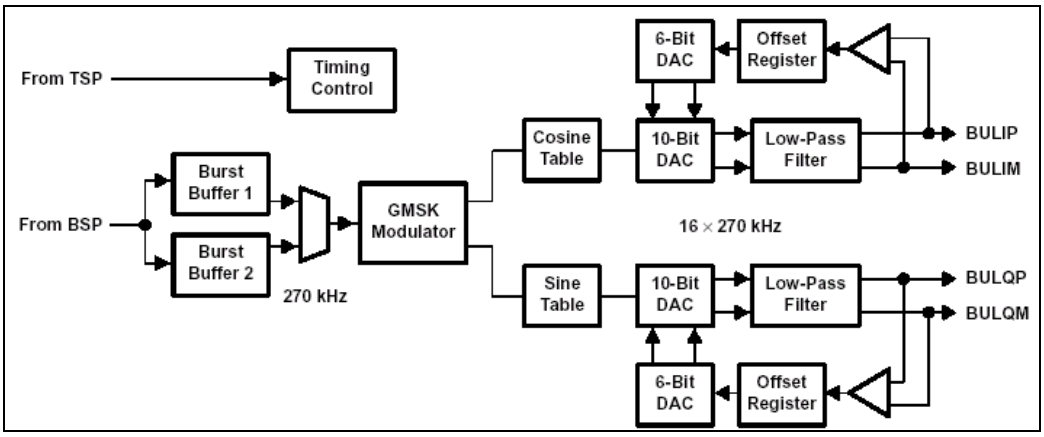
Baseband codec is composed of baseband uplink path(BUL) and baseband downlink path(BDL).

BUL makes GMSK(Gaussian Minimum Shift Keying) modulated signal which has In-phase(I) component and quadrature(Q) component with burst data from DBB. This modulated signal is transmitted through RF section via air.

BDL process is opposite procedure of BUL. Namely, it performs GMSK demodulation with input analog I&Q signal from RF section, and then transmit it to DSP of DBB chip with 270.833kHz data rate through BSP.

Figure12 Baseband Codec Block Diagram

	Output Voltage	Usage
VRDBB	1.5V	Digital Core of DBB
VRIO	2.8V	Peripheral devices
VRMEM	2.8V	External memory
VRRAM	2.8V	LCD & peripheral devices
VRABB	2.8V	Analog Block of ABB
VRSIM	2.85	SIM card driver
VRRTC	1.5V	RTC & 32kHz-crystal



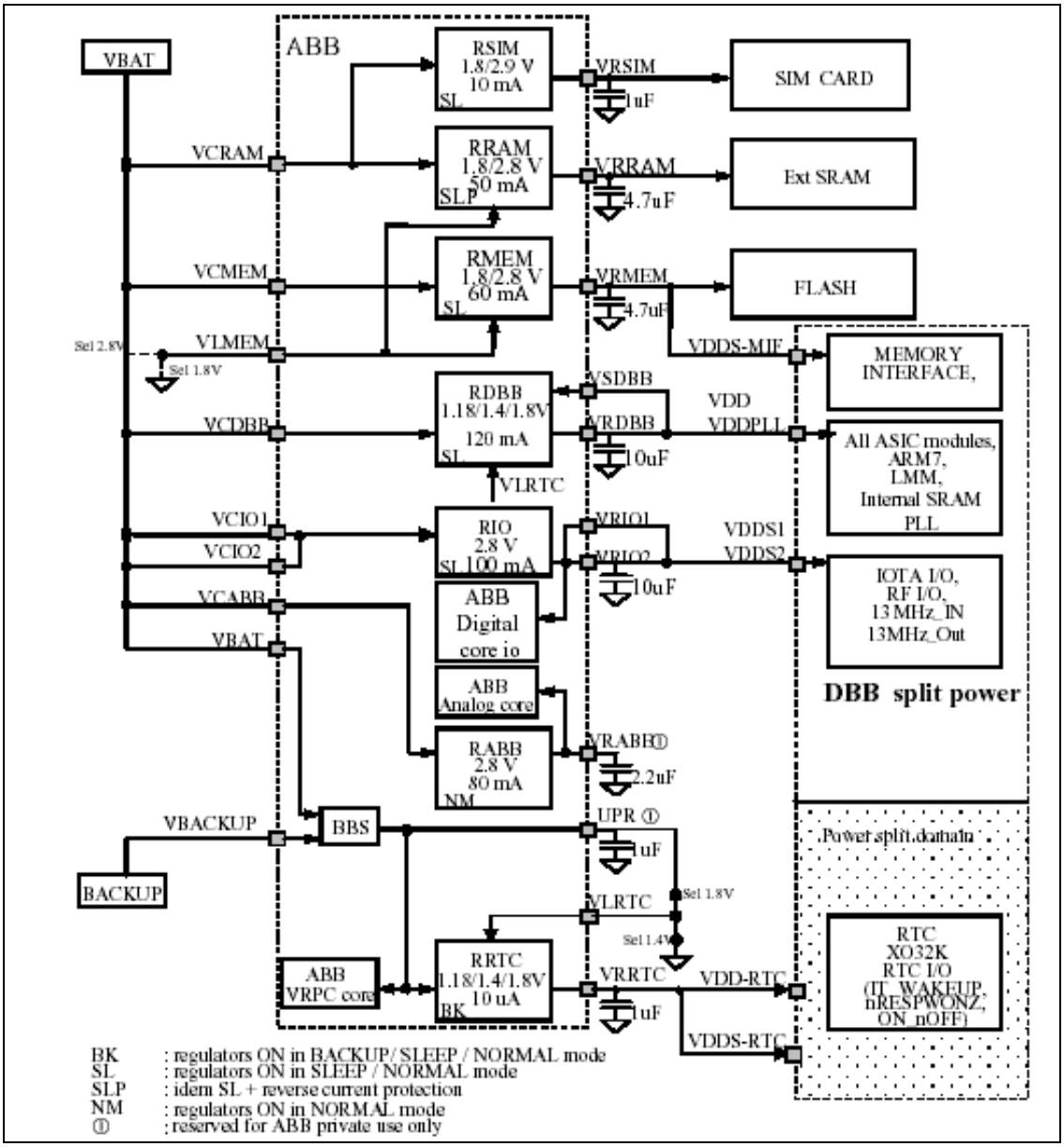
D. Voltage Regulation(VREG)

There are 7 LDO(Low Drop Output) regulators in ABB chip.

The output of these 7 LDOs are as following table. (Figure13) shows the power supply related blocks of DBB/ABB and their interfaces in UP-100.

Table 5 LDO Output Table

Figure13 Power Supply Scheme



E. ADC Channels

ABB ADC block is composed of 4 internal ADC(Analog to Digital Converter) channels and 4 external ADC channel. This block operates charging process and other related process by reading battery voltage and other analog values.

Table 6 ADC Channel Spec.

ADC 8 channels		
Resource	**Name**	**Description**
VCHG	VCHG	Charging Management
VBAT	VBAT	
ICHG	ICHG	
VBACKUP	VBACKUP	Backup Battery
ADIN1	JACK_DETECT	Jack plug-in detect
ADIN2	BATT_TEMP	Battery Detect
ADIN3	TEMPSENSE	Temperature Sensing
ADIN4	HOOK_DETECT	HOOK_DETECT

F. Charging

Charging block in ABB processes charging operation by using VBAT, ICHG value through ADC channel. Battery Block Indication and SPEC of UP-100 is as follow.

1. Charging method : CC-CV
2. Charger detect voltage : 4.2V
3. Charging time : 2h30min
4. Charging current : 500mA
5. CV voltage : 4.2V
6. Cutoff current : 50mA
7. Recharge voltage : 4.15V
8. Low battery alarm
   a. Idle : 3.62V
   b. Dedicated : 3.50V
9. Low battery alarm interval :
   a. Idle : 3min
   b. Dedicated:1min
10. Switch-off voltage : 3.35V

G. Switch ON/OFF

UP-100 Power State : Defined 4cases as follow

- Power-ON : mobile is powered by main battery or backup battery.
- Power-OFF : mobile isn't any battery.
- Switch-ON : mobileis powered and waken up from switch-off state.
- Switch-OFF : mobile is powered to maintain only the permanent function(ULPD).

To enter into Switch-ON state, one of followinf 4 condition is satisfied.

- **PWR-ON** pushed after a debouncing time of 30ms.
- **ON_REMOTE** : After debouncing, when a falling edgeis detected on RPWON pin.
- **IT_WAKE_UP** : When a rising edge is detected on RTC_ALARM pin.
- **CHARGER_IC** :When a charger voltage is above VBAT+0.4V on VCHG.

H. Memories

32Mbit Flash + 4Mbit SRAM

16 bit parallel data bus

ADD01 ~ ADD22

I. Display & FPCB Interface

LCD module include:

Main LCD : 120*64 Mono Scale LCD

Main LCD Backlight : EL-Backlight

LCD module is connected to main board with 25 pin.

FPCB Interface Spec

Table 7 FPCB Interface Spec.

No	Pin Name	Function
1	V0	
2	V4	
3	V3	
4	V2	
5	V1	LCD Read Control
6	C2-	
7	C2+	
8	C1+	
9	C1-	
10	C3+	
11	VOUT	
12	GND	VSS
13	VDD	
14	D(7)	Data input
15	D(6)	Data input
16	D(5)	Data input
17	D(4)	Data input
18	D(3)	Data input
19	D(2)	Data input
20	D(1)	Data input
21	D(0)	Data input
22	WR	LCD Write Control
23	A(1)	Address Line
24	LCD_RESET	LCD Reset

25	MAIN_CS	LCD Chip set

J. KeyPad Switching & Scanning

Keypad Map

Table 8 Keypad Map

	KBC0	KBC1	KBC2	KBC3
KBR0	[►]	[◄]	[▲]	[▼]
KBR1	[1]	[2]	[3]	CLR
KBR2	[4]	[5]	[6]	[F1]
KBR3	[7]	[8]	[9]	[SEND]
KBR4	[#]	[0]	[*]	[F2]

DBB supports 25 keymap and Switch-ON Key is connected directly to ABB as (Figure15).

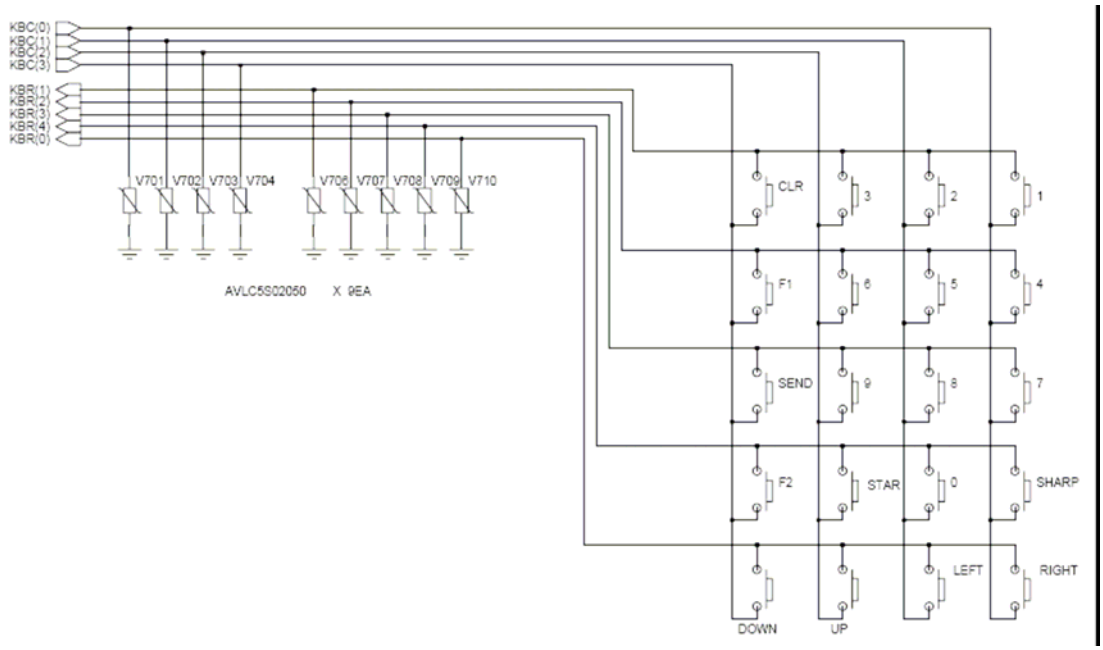


Figure 15 Keypad Scanning Scheme

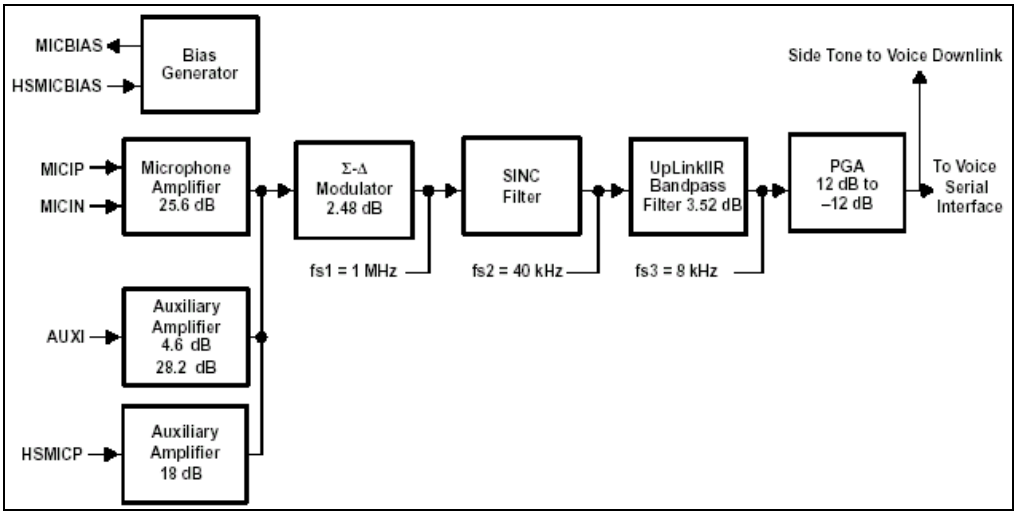
K. Audio

(Uplink)

The microphone is soldered to the main PCB. The uplink signal is passed to MICIP and MICIN pins of IOTA.

The MICBIAS voltage is supplied from IOTA(dedicated mode only). When the headset is inserted, ADC value of HOOK_DETECT(IO6) terminal is between 20 to 150 (decimal value). On detecting this, Calypso makes IOTA switches the MIC amplifier path from main to auxiliary.

Figure16 Uplink Path



(Downlink)

The downlink signal is passed from EARP and EARN pins of IOTA. When the headset is inserted and Calypso detects 'Jack pluged state' from HOOK_DETECT terminal, Calypso makes IOTA switches the downlink path from 'EARP' and 'EARN' to auxiliary outputs('AUXOP' and 'AUXON' or 'HSO').

Figure17 Downlink Path

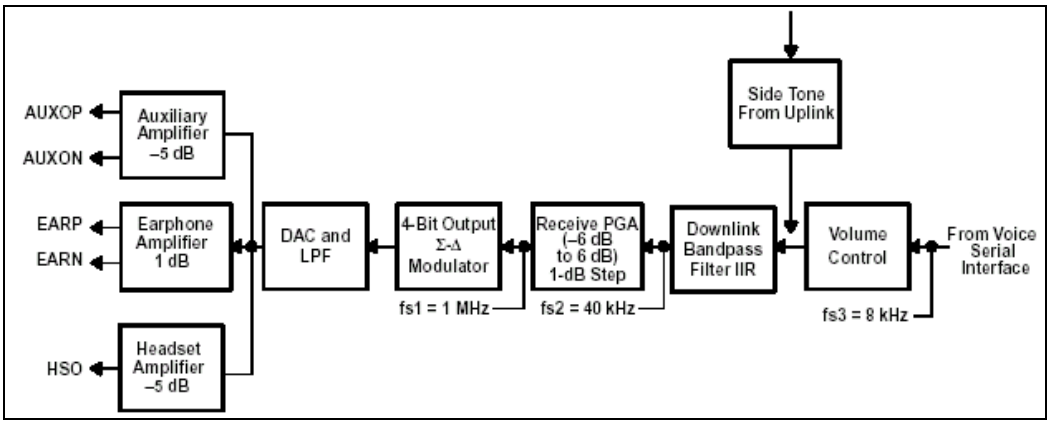
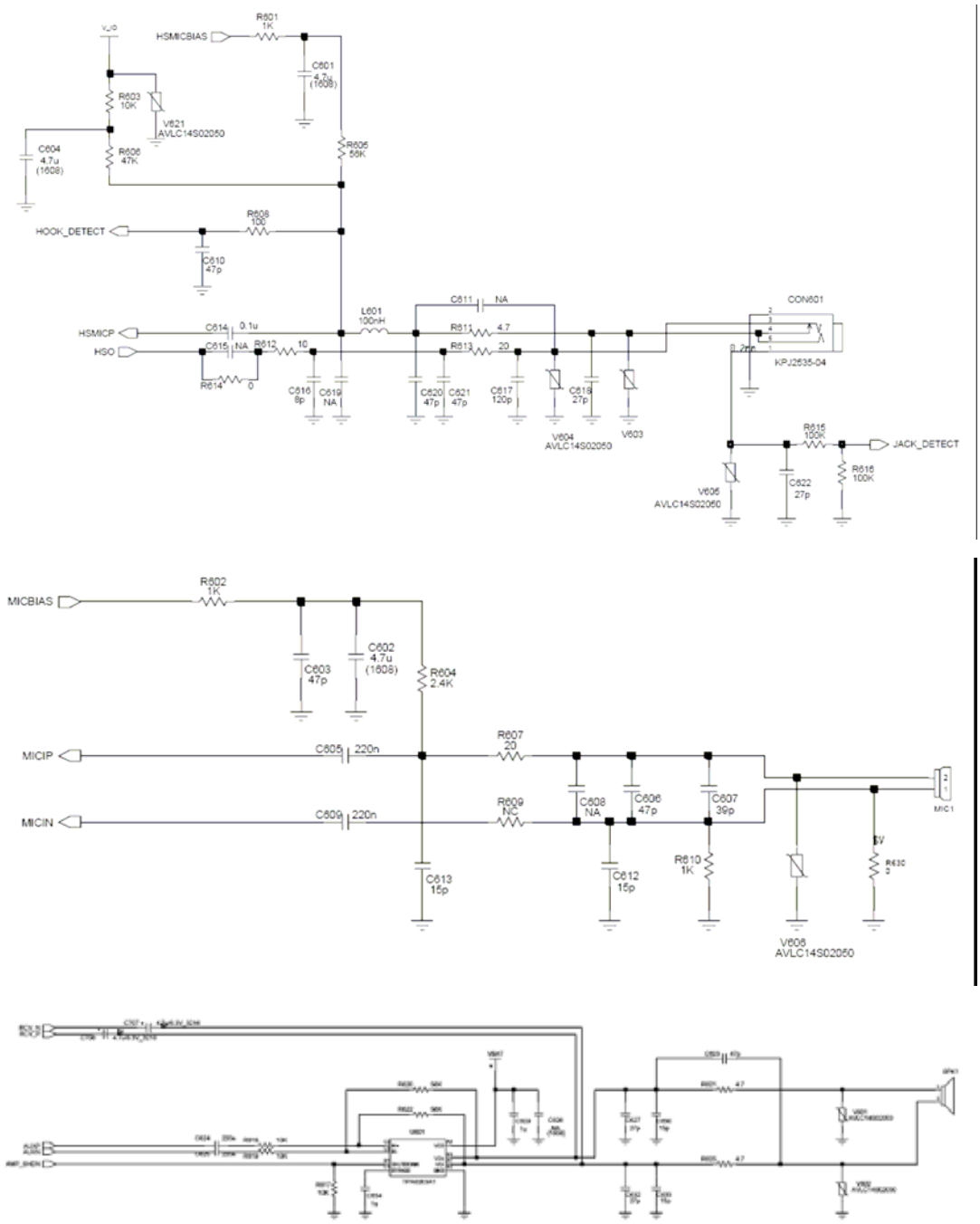


Figure18 Audio Circuit

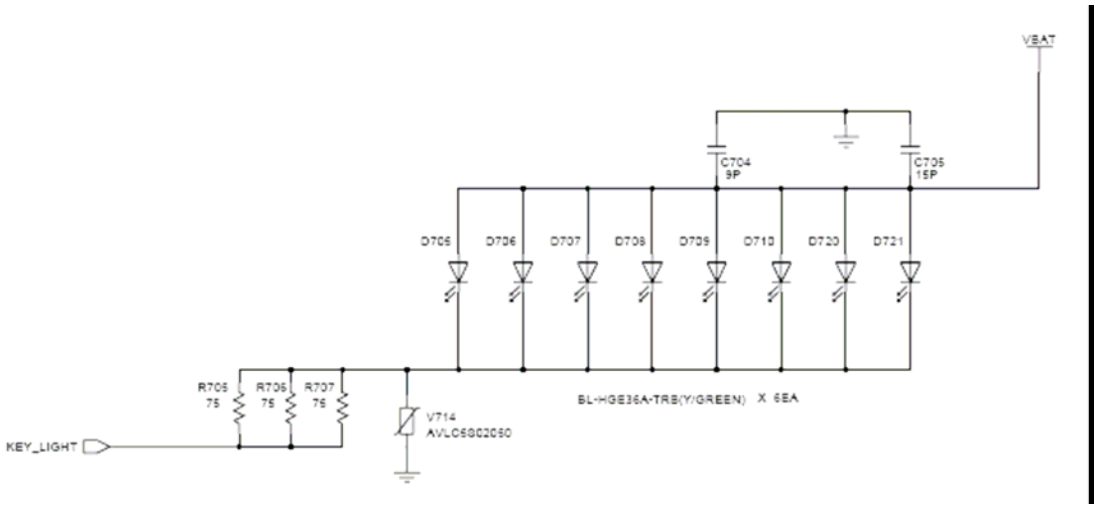


L. Keypad back-light Illumination

There are 6 Amber LEDs in Main Board for Keypad Backlight.

Keypad Back-light is driven by ‘LEDB’ line from IOTA .

Figure19 Keypad Back-light Scheme



M. Main_LCD Illumination

There is EL-Backlight Sheet in the LCD module for LCD backlighting. DC-DC converter is mounted in LCD module.

Figure20 Main-LCD Back-light Scheme