APPENDIX G – OPERATIONAL DESCRIPTION

NEO200_850T
Circuit Description

REVISED HISTORY

DATE	ISSUE	CONTENTS OF CHANGES	S/W VERSION
September / 2005	ISSUE 1.0	Initial Release	

* The information in this manual is subject to change without notice and should not be construed as a commitment by BELLWAVE Inc. Furthermore, BELLWAVE Inc. reserves the right, without notice, to make changes to equipment design as advances in engineering and manufacturing methods warrant.

* This manual provides the information necessary to install, program, operate and maintain the NEO200_850T.

SECTION 1. PERFORMANCE

1.1 H/W Feature

Item	Feature	Comment
Standard Battery	Li-ion, 720mAh Size: 4.45(T)x31.5(W)x52.3(L) mm Weight: 16g	
AVG TCVR Current	GSM850: 230mA, DCS1800/PCS1900: 180mA	
Standby Current	< 4.0mA	
Talk time	< 4 hours (GSM TX Level 7)	
Standby time	200 hours (Paging Period:2, RSSI: -85dBm)	
Charging time	2.5 hours	
RX Sensitivity	GSM850 : -108dBm, DCS/PCS : -106dBm	
TX output power	GSM850: 32.2dBm (Level 5) DCS1800/PCS1900: 29.3dBm (Level 0)	
GPRS compatibility	Class 10	
SIM card type	1.8V/3V Small	
Display	128 × 160 dots main LCD, 96 × 96 sub LCD	
Status Indicator	2 color LED	
ANT	Internal Antenna	
EAR Phone Jack	8 pole earphone jack	
PC Synchronization	Yes	
Speech coding	EFR/FR	
Data and Fax	Yes	
Vibrator	Yes	
Buzzer	Yes	
Voice Recoding	Yes	
C-Mike	Yes	
Receiver	Yes	
Travel Adapter	Yes	
Options	No	

1.2 Technical Specification

<table>
<tr><td>Item</td><td>Description</td><td>Specification</td></tr>
<tr><td>1</td><td>Frequency Band</td><td>GSM 850 TX : 824– 849 MHz
GSM 850 RX : 869 – 894 MHz
DCS 1800 TX : 1710 – 1785 MHz
DCS 1800 RX : 1805 – 1880 MHz
PCS 1900 TX : 1850 – 1910 MHz
PCS 1900 RX : 1930 – 1990 MHz</td></tr>
<tr><td>2</td><td>Phase Error</td><td>RMS < 5 degrees
Peak < 20 degrees</td></tr>
<tr><td>3</td><td>Frequency Error</td><td>< 0.1ppm</td></tr>
<tr><td>4</td><td>Power Level</td><td>
<table>
<tr><td colspan="6">GSM850</td></tr>
<tr><td>Level</td><td>Power</td><td>Toler.</td><td>Level</td><td>Power</td><td>Toler.</td></tr>
<tr><td>5</td><td>33 dBm</td><td>±2dB</td><td>13</td><td>17 dBm</td><td>±3dB</td></tr>
<tr><td>6</td><td>31 dBm</td><td>±3dB</td><td>14</td><td>15 dBm</td><td>±3dB</td></tr>
<tr><td>7</td><td>29 dBm</td><td>±3dB</td><td>15</td><td>13 dBm</td><td>±3dB</td></tr>
<tr><td>8</td><td>27 dBm</td><td>±3dB</td><td>16</td><td>11 dBm</td><td>±5dB</td></tr>
<tr><td>9</td><td>25 dBm</td><td>±3dB</td><td>17</td><td>9 dBm</td><td>±5dB</td></tr>
<tr><td>10</td><td>23 dBm</td><td>±3dB</td><td>18</td><td>7 dBm</td><td>±5dB</td></tr>
<tr><td>11</td><td>21 dBm</td><td>±3dB</td><td>19</td><td>5 dBm</td><td>±5dB</td></tr>
<tr><td>12</td><td>19 dBm</td><td>±3dB</td><td></td><td></td><td></td></tr>
<tr><td colspan="6">DCS1800/1900</td></tr>
<tr><td>Level</td><td>Power</td><td>Toler.</td><td>Level</td><td>Power</td><td>Toler.</td></tr>
<tr><td>0</td><td>30 dBm</td><td>±2dB</td><td>8</td><td>14 dBm</td><td>±3dB</td></tr>
<tr><td>1</td><td>28 dBm</td><td>±3dB</td><td>9</td><td>12 dBm</td><td>±4dB</td></tr>
<tr><td>2</td><td>26 dBm</td><td>±3dB</td><td>10</td><td>10 dBm</td><td>±4dB</td></tr>
<tr><td>3</td><td>24 dBm</td><td>±3dB</td><td>11</td><td>8 dBm</td><td>±4dB</td></tr>
<tr><td>4</td><td>22 dBm</td><td>±3dB</td><td>12</td><td>6 dBm</td><td>±4dB</td></tr>
<tr><td>5</td><td>20 dBm</td><td>±3dB</td><td>13</td><td>4 dBm</td><td>±4dB</td></tr>
<tr><td>6</td><td>18 dBm</td><td>±3dB</td><td>14</td><td>2 dBm</td><td>±5dB</td></tr>
<tr><td>7</td><td>16 dBm</td><td>±3dB</td><td>15</td><td>0 dBm</td><td>±5dB</td></tr>
</table>
</td></tr>
</table>

5	Output RF Spectrum (due to modulation)	GSM850	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600 ~ 1,200	-60
		1,200 ~ 1,800	-60
		1,800 ~ 3,000	-63
		3,000 ~ 6,000	-65
		6,000	-71
		DCS1800/PCS1900	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600 ~ 1,200	-60
		1,200 ~ 1,800	-60
		1,800 ~ 3,000	-65
		3,000 ~ 6,000	-65
		6,000	-73
6	Output RF Spectrum (due to switching transient)	GSM850	
		Offset from Carrier (kHz)	Max. (dBm)
		400	-19
		600	-21
		1,200	-21
		1,800	-24
		DCS	
		Offset from Carrier (kHz)	Max. (dBm)
		400	-22
		600	-24
		1,200	-24
		1,800	-27
7	Spurious Emissions	Conduction, Emission Status Conduction, Emission Status	

<table>
<tr><td>8</td><td>Bit Error Ratio</td><td colspan="3">GSM850
BER (Class II) < 2.439% @-102dBm
DCS1800/PCS1900
BER (Class II) < 2.439% @-100dBm</td></tr>
<tr><td>9</td><td>Rx Level Report accuracy</td><td colspan="3">± 3 dB</td></tr>
<tr><td>10</td><td>SLR</td><td colspan="3">8 ± 3 dB</td></tr>
<tr><td rowspan="10">11</td><td rowspan="10">Sending Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>/</td></tr>
<tr><td>200</td><td>0</td><td>/</td></tr>
<tr><td>300</td><td>0</td><td>-12</td></tr>
<tr><td>1,000</td><td>0</td><td>-6</td></tr>
<tr><td>2,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,400</td><td>4</td><td>-9</td></tr>
<tr><td>4,000</td><td>0</td><td>/</td></tr>
<tr><td>12</td><td>RLR</td><td colspan="3">2 ± 3 dB</td></tr>
<tr><td rowspan="12">13</td><td rowspan="12">Receiving Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>/</td></tr>
<tr><td>200</td><td>0</td><td>/</td></tr>
<tr><td>300</td><td>2</td><td>-7</td></tr>
<tr><td>500</td><td>*</td><td>-5</td></tr>
<tr><td>1,000</td><td>0</td><td>-5</td></tr>
<tr><td>3,000</td><td>2</td><td>-5</td></tr>
<tr><td>3,400</td><td>2</td><td>-10</td></tr>
<tr><td>4,000</td><td>2</td><td></td></tr>
<tr><td colspan="3">* Mean that Adopt a straight line in between 300 Hz and 1,000 Hz to be Max. level in the range.</td></tr>
<tr><td>14</td><td>STMR</td><td colspan="3">13 ± 5 dB</td></tr>
<tr><td>15</td><td>Stability Margin</td><td colspan="3">> 6 dB</td></tr>
<tr><td rowspan="8">16</td><td rowspan="8">Distortion</td><td>dB to ARL (dB)</td><td colspan="2">Level Ratio (dB)</td></tr>
<tr><td>-35</td><td colspan="2">17.5</td></tr>
<tr><td>-30</td><td colspan="2">22.5</td></tr>
<tr><td>-20</td><td colspan="2">30.7</td></tr>
<tr><td>-10</td><td colspan="2">33.3</td></tr>
<tr><td>0</td><td colspan="2">33.7</td></tr>
<tr><td>7</td><td colspan="2">31.7</td></tr>
<tr><td>10</td><td colspan="2">25.5</td></tr>
<tr><td>17</td><td>Side tone Distortion</td><td colspan="3">Three stage distortion < 10%</td></tr>
<tr><td>18</td><td><Change> System frequency (26 MHz) tolerance</td><td colspan="3">≤ 2.5 ppm</td></tr>
<tr><td>19</td><td><Change>32.768KHz tolerance</td><td colspan="3">≤ 30ppm</td></tr>
</table>

20	Power consumption	Full power < 250mA (GSM850) ; < 200mA (DCS/PCS) Standby - Normal Mode ≤ 4.0mA(Mix. power) - Using Test mode on DSP Sleep function ≤ 6mA	
21	Talk Time	GSM850/Level 7 (Battery Capacity 720mA):1800 Min GSM850/Level 12(Battery Capacity720:250 Min	
22	Standby Time	Under conditions, at least 200 hours: 1. Brand new and full 740mAh battery 2. Full charge, no receive/send and keep GSM in idle mode. 3. Broadcast set off. 4. Signal strength display set at 3 level above. 5. Backlight of phone set off.	
23	Ringer Volume	At least 80 dB under below conditions: 1. Ringer set as ringer. 2. Test distance set as 50 cm	
24	Charge Voltage	Fast Charge : < 500 mA Slow Charge: < 60 mA	
25	Antenna Display	Antenna Bar Number	Rx level
		0	Rx≤-103dBm
		1	Rx≤-95dBm
		2	Rx≤-91dBm
		3	Rx≤-86dBm
		4	Rx≤-81dBm
		5	Rx＞-81dBm
26	Battery Indicator	Battery Bar Number	Voltage
		0	3.4~ 3.54 V
		1	3.55 ~ 3.68 V
		2	3.69 ~ 3.81 V
		3	3.82 ~4.2V
27	Low Voltage Warning	3.35~3.60 V (Call)	
		3.35~3.50V (Standby)	
28	Forced shut down Voltage	3.35 ± 0.03 V	
29	Battery Type	1 Li-ion Battery Standard Voltage = 3.7 V Battery full charge voltage = 4.2 V Capacity: 720mAh	
30	Travel Charger	Switching-mode charger Input: 100 ~ 240 V, 50/60Hz Out put: 5.2V, 600mA	

SECTION 2. TECHNICAL BRIEF

2.1 General Description

RF part consists of a transmit part, a receive part, a voltage supply part. The RF main chipset SMARTi SD2 is a single-chip multi-band GSM850 and DCS/PCS (GPRS) wireless communication (voice and data applications). This device integrated a receive section based on a zero-IF receiver architecture and a transmit section based on an offset phase-locked loop (OPLL) with a fully integrated transmit VCO.

2.2 Receiver Part

A. RF Front End Demodulator

RF front end is consists of FEM(U100), Tri band LNAs integrated in transceiver.
The Received RF signals (GSM 925MHz ~ 960MHz, DCS 1805MHz ~ 1880MHz, PCS 1930MHz ~1990MHz) are fed into the antenna or FEM. An antenna matching circuit is between the antenna and the FEM.
The FEM control the Rx and Tx paths.
And, the input signals VC1 and VC2 of the FEM are directly connected to baseband control signals to switch either Tx or Rx path on. The FEM(U100) is Front End Module for Tri band.
The logic and current is given below The SMARTi SD2 RF front-end contains four integrated SNAs for GSM900/DCS1800/PCS1900 with balanced inputs. The amplified RF-signal is direct converted by a quadrature demodulator to the final output signals at the baseband frequency. The orthogonal LO signals are internally generated by a divider by four for GSM850 band and by two for the DCS/PCS band.

Table 1.

Table 1 The Logic and Current

	VC1	VC2	Current
GSM850 TX	2.4 ~ 2.8 V	.0 V	8.0 mA max
DCS1800/PCS1900 TX	0 V	2.4 ~ 2.8 V	8.0 mA max
GSM/DCS/PCS RX	0 V	0 V	< 0.1 mA

B. Transceiver

Receive section:

The SMARTi SD2 features a fully integrated quad-band constant gain direct conversion receiver, i.e. there is no interstage filter needed and the baseband level at the analog I/Q interface follows directly the RF input level. Dependent on the baseband ADC dynamic range single or multiple step gain switching schemes are applicable. An integrated self-aligning low-pass filter ensures the receivers functionality under blocking and reference interference conditions as well as avoids aliasing by baseband sampling. Furthermore an automatic DC offset compensation is implemented and can be switched on dependent on the gain setting. All receiver settings are programmed in the RXTX word.

-- Constant gain direct conversion receiver with integrated blocking filter.

-- Optimized for 72dB dynamic range ADC RX baseband interface.

-- GPRS(class 1 to 12 / type1).

-- Four integrated LNAs.

-- No need of interstage and IF Filter.

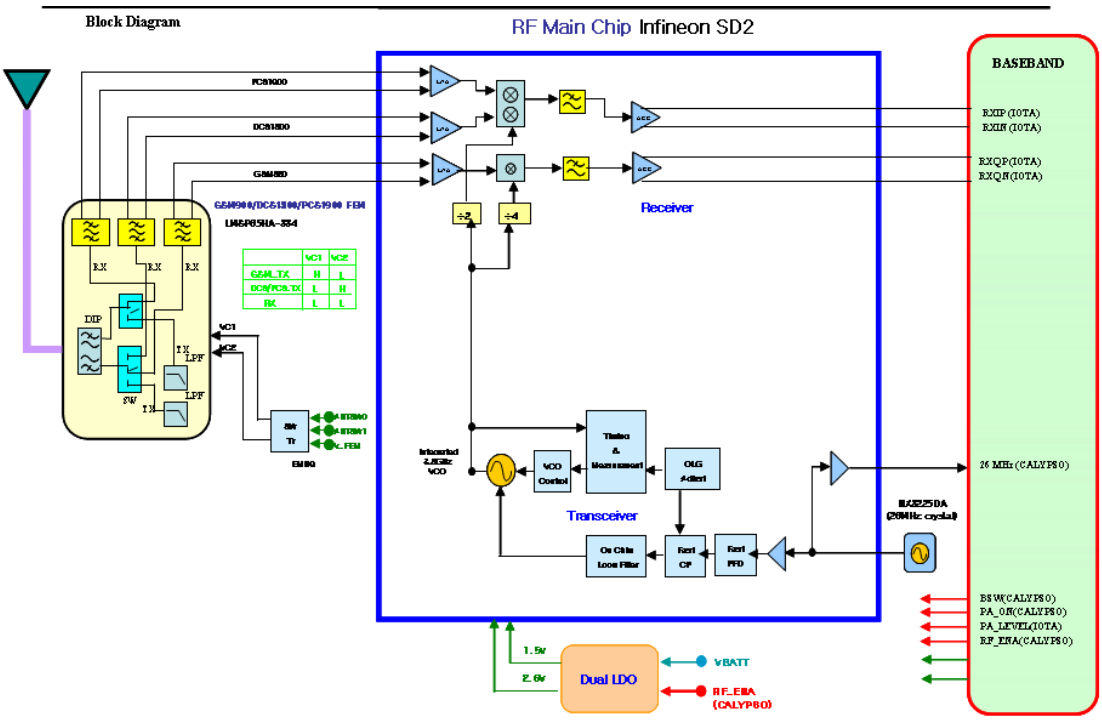
-- Highly linear RF quadrature demodulator.

-- Programmable DC output level.

-- Very low power budget.

Figure 1 Receiver Part Block Diagram

◆ RF Rx Block Diagram (GSM850+DCS1800/PCS1900)



2.3 Synthesizer Part

-- ΣΔSynthesizer for multi-slot operation supports GPRS class 12.

-- Fast lock-in times(<150 μsec)

-- Integrated loop filter

2.4 Transmitter Part

A. Transceiver

The digital transmitter architecture is based on a fractional-N sigma-delta symthesizer for constant envelope GMSK modulation. This confiquration allows a very low power desing with a reduced count of external components.

The modulation is transferred via the standard I/Q interface of the SMARTi SD2.

The analog I/Q signals are converted to digital using two ADCs to regenerate the digital data stream for the digital modulator.

The following Gaussian filter shapes the digital data stream for the GMSK modulation. Additionally a predistortion filter compensates the attenuation of the PLL transfer function resulting in a very low distortion at the transmit output.

The filtered digital data stream is scaled appropriately and added to the channel word. Thins sum is fed into the MASH modulator. The output of the MASH modulator is a sequence of integer divider values representing the high resolution fractional input signal. This sequence controls the MMD(multi modulus divider) at a sample rate of 26MHz. Thus a tightly controlled frequency modulation of the VCO is achieved.

The output signal of the VCO is divided by four for GSM900 or by two for GSM1800 respectively. Finally the divided signal is amplified by a single ended output driver with 50Ohm output impedance to allow a direct connection to the PA.

The transmitter achieves a very low ou-of-band noise, typically -165.5dBc/Hz @ 20MHz offset, and a very low rms phase error of 0.7 degree typically in GSM900.

Transmit section:

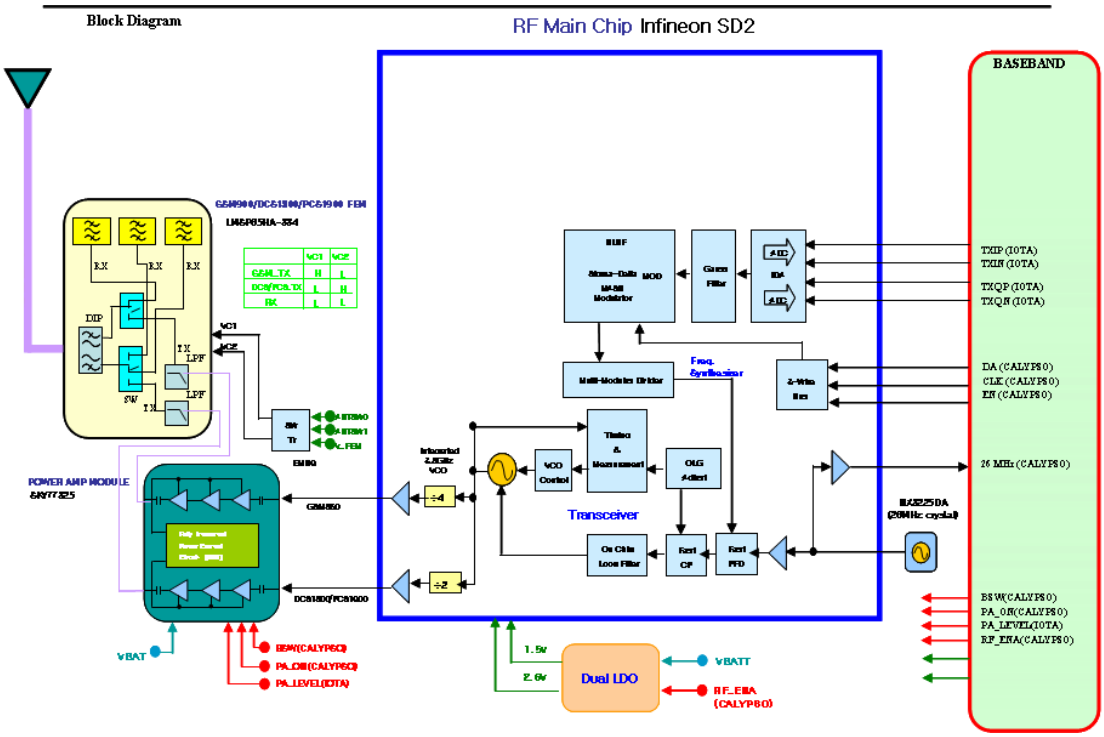
-- Digital Sigma-Delta modulator for GMSK modulation, typ. -163.5 dBc/Hz @ 20MHz

-- Single ended outputs to PA, Pout =+ 3.5dBm

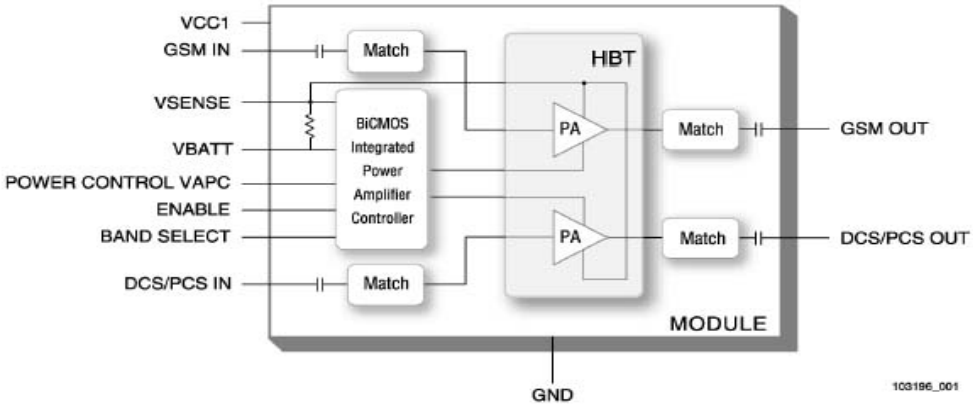
-- Standard analog I/Q interface(IDA) for the digital modulator.

-- Very low power budget.

Figure 2 Transmitter Block Diagram



B. Power Amplifier



The SKY77325 Power Amplifier Module(PAM) is designed in a low profile (1.2mm), compact form factor for quad-band cellular handsets comprising GSM850/900, DCS1800 and PCS1900 operation. The PAM also supports Class 12 GPRS multi-slot operation.

The module consists of separate GSM900 PA and DCS1800 PA blocks, impedance matching circuitry for 50Ohm input and output impedances, and a Power Amplifier Control(PAC) block with an internal current-sense resistor. The custom BiCMOS integrated circuit provides the internal PAC function and interface circuitry.

Fabricated onto a single Gallium Arsenide(GaAs) die, one Hetero junction Bipolar Transistor(HBT) PA block supports the GSM900 bands and the other supports the DCS1800 band. Both PA blocks share common power supply pins to distribute current. The GaAs die, the Silicon die, and the passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold.

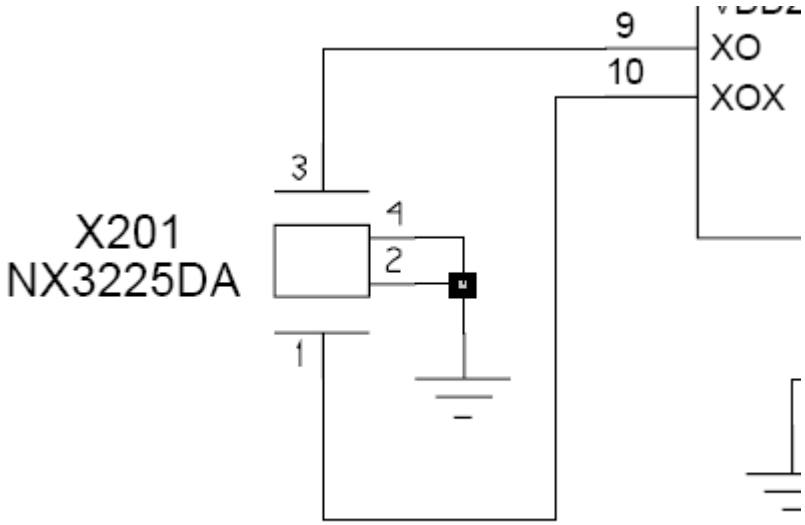
RF input and output ports of the SKY77325 are internally matched to a 50Ohm load to reduce the number of external components for a quad-band design. Extremely low leakage current (2.5Ua, typical) of the dual PA module maximizes handset standby time. The SKY77325 also contains band-select switching circuitry to select GSM(logic 0) or DCS/PCS(logic 1) as determined from the Band Select(BS) signal. The BS pin selects the PA output (DCS/PCS OUT or GSM850 OUT) and the Analog Power Control(VAPC) controls the level of output power.

The ENABLE input allows initial turn-on of PAM circuitry to minimize battery drain.

2.5 26 MHz Clock

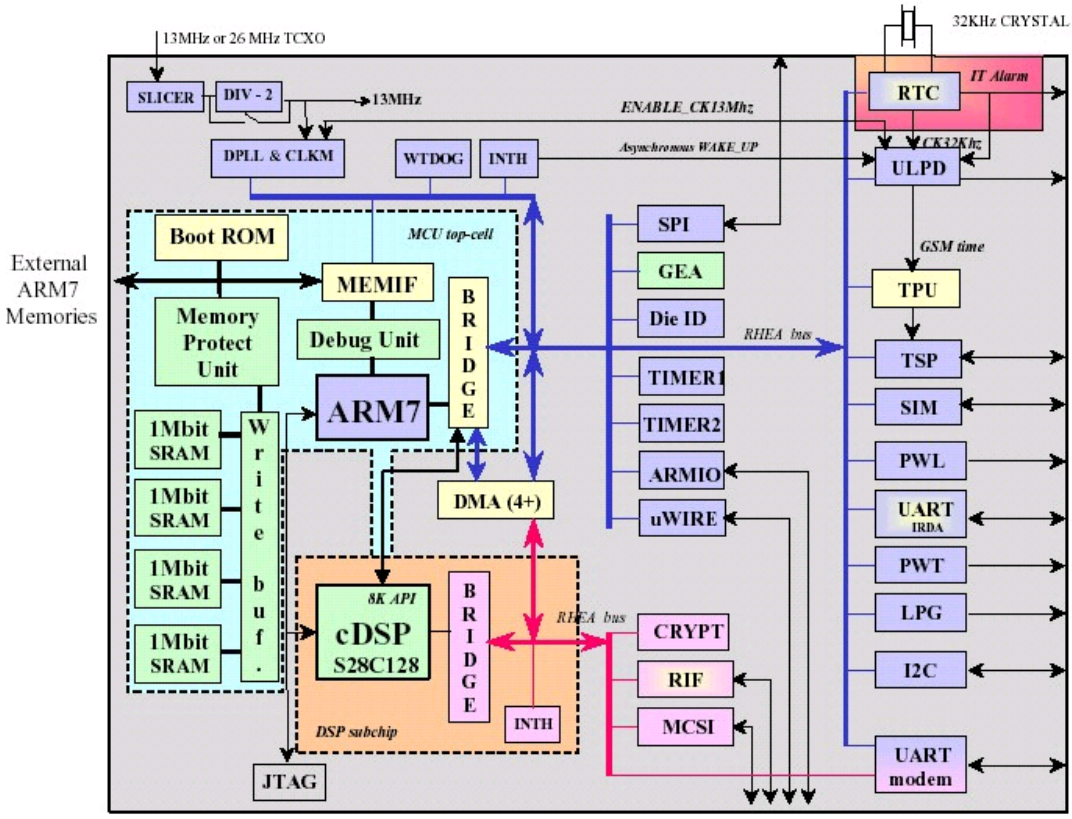
The 26 MHz clock(X201) consists of a X-Tal which oscillates at a frequency of 13 MHz. It is used within the SMARTISD2 RF Main Chip, BB Analog chip-set(IOTA), Digital chip-set(Calypso Lite).

Figure 5 X-Tal Circuit



2.7 Digital Baseband(DBB) Processor

Figure 7 Top level block diagram of the Calypso G2(HERCROM400G2)



A. General Description

CALYPSO is a chip implementing the digital base-band processes of a GSM/GPRS mobile phone. This chip combines a DSP sub-chip (LEAD2 CPU) with its program and data memories, a Micro--Controller core with emulation facilities (ARM7TDMIE), internal 8Kb of Boot ROM memory, 4M bit SRAM memory, a clock squarer cell, several compiled single-port or 2-ports RAM and CMOS gates. The chip will fully support the Full-Rate, Enhanced Full-Rate and Half-Rate speech coding. CALYPSO implements all features for the structural test of the logic (full-SCAN, BIST, PMT, JTAG boundary-SCAN).

B. Block Description

CALYPSO architecture is based on two processor cores ARM7 and DSP using the generic RHEA bus standard as interface with their associated application peripherals.

CALYPSO is composed from the following blocks:

- ARM7TDMIE : ARM7TDMI CPU core
- DSP subchip
- ARM peripherals:

General purpose peripherals

- ARM Memory Interface for external RAM, Flash or ROM
- 4 Mbit Static RAM with write-buffer

Application peripherals

- ARM General purposes I/O with keyboard interface and two PWM modulation signals
- UART 16C750 interface (UART_IRDA) with
  - IRDA control capabilities (SIR)
  - Software flow control (UART mode).
- UART 16C750 interface (UART_MODEM) with
  - hardware flow protocol (DCD, CTS/RTS)
  - autobaud function
- SIM Interface.
- TPU(Time Processing Unit) : Processing for GSM time base
- TSP(Time Serial Port) : GSM data interface with RF and ABB

Memory Interface : External/Internal Memory Interface

nCS0 : FLASH1, 16bit access, 3 wait state

nCS1 : FLAHS2, 16bit access, 3 wait state

nCS2 : Ext SRAM, 16bit access, 3 wait state

nCS3 : Main LCD(16bit access), OEL(8bit access) addressing, 3 wait state (See Fig 3-11)

nCS4 : MIDI(8bit access), USB(8bit access) addressing, 3 wait state (See Fig 3-12)

nCS6 : Int SRAM, 32bit access, 0 wait state

* Calypso is internally 39MHz machine (25ns machine cycle), so it requires 3 wait-state for 80ns access(25*4 = 100 ns).

C. External Devices connected to memory interface

Table 2 External Device Spec. connected to memory interface

Interface SPEC					
Device	**Name**	**Maker**	**Write Access Time**	**Read Access Time**	
MCP	S99PL193JC0BAWUB0	SPANSION	70ns	70ns	
NAND FLASH	K9K1208D0C-D/JIB0	SAMSUNG	45ns	50ns	
LCD DRIVER IC	HD66773	HITACHI	50ns	50ns	
Melody IC	YMU787	Yamaha	50ns	80ns	

D. RF Interface (TPU, TSP block)

Calypso uses this interface to control Nausica_CS(ABB Processor) and Clara(RF Processor) with GSM Time Base

Table 3 RF Interface Spec.

TSP (Time Serial Port)		
Resource	**Interconnection**	**Description**
TSPDO	ABB & RF main Chip	Control Data
TSPEN0	ABB	ABB Control Data Enable Signal
TSPEN1	RF main Chip	RF Control Data Enable Signal
TPU (Time Processing Unit) Parallel Port		
TSPACT00	RESET_RF	RF main Chip Reset Signal
TSPACT05	PA_ON	Power Amp ON signal

E. SIM interface

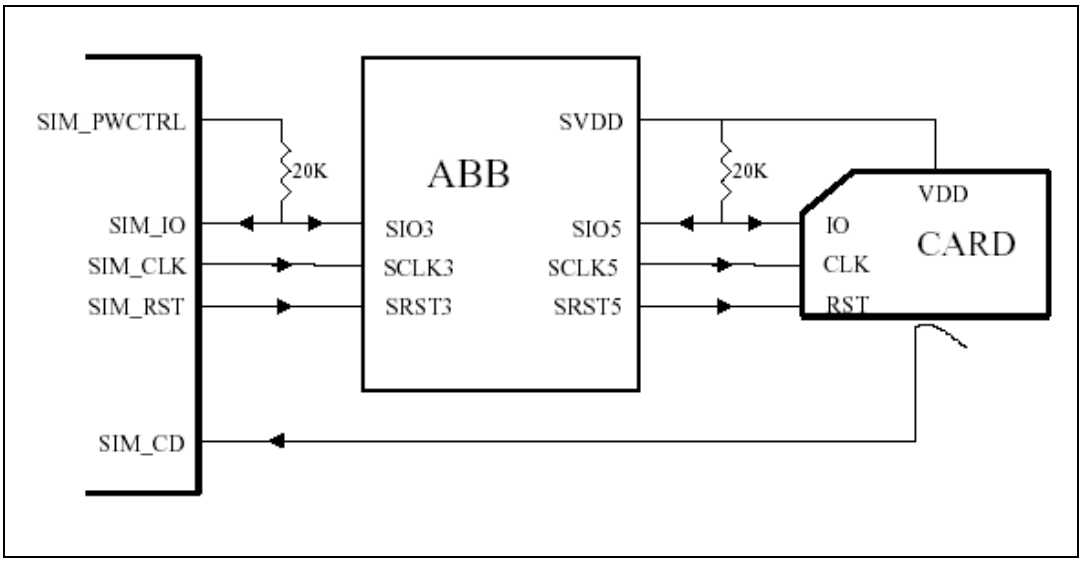
SIM interface scheme is shown in (Figure 10).

SIM_IO, SIM_CLK, SIM_RST ports are used to communicate DBB with ABB and the Charge Pump in ABB enables 1.8V/3V SIM operation

SIM Interface

SIM_CLK SIM card reference clock
SIM_RST SIM card async/sync reset
SIM_IO SIM card bidirectional data line
SIM_PWCTRL SIM card power activation
SIM_RnW SIM card data line direction
SIM_CD SIM card presence detection

Figure.10 SIM Interface



F. GPIO map

In total 16 allowable resources, NEO200_850TN is using 13 resources except 3 resources dedicated to SIM and Memory. NEO200_850TN GPIO(General Purpose Input/Output) Map, describing application, I/O state, and enable level, is shown in below table.

Table .4 GPIO Map Table

I/O #	Application	I/O	Resource State	Inactive State	Active State
I/O (0)	MELODY_IRQ	I	GPIO	LOW	HIGH
I/O (1)	MELODY_RST	O	GPIO	LOW	HIGH
I/O (2)	JACK_DET	I	GPIO	HIGH	LOW
I/O (3)	REED	O	GPIO	LOW	HIGH
I/O (4)	AIT_RST	O	GPIO	LOW	HIGH
I/O (5)	PHLCD_BY	O	GPIO	LOW	HIGH
I/O (6)	EAR_HOOK	I	GPIO	HIGH	LOW
I/O (7)	AIT_813_EN	O	GPIO	LOW	HIGH
I/O (8)	LCD_RST	O	GPIO	LOW	HIGH
I/O (9)	USB_EN	O	GPIO	LOW	HIGH
I/O (10)	RECEIVER_ON	O	GPIO	LOW	HIGH
I/O (11)	DSR	I	GPIO	LOW	HIGH
I/O (12)	V_BUS	O	GPIO	LOW	HIGH
I/O (13)	PHINT	O	GPIO	LOW	HIGH
I/O (14)	BHE	O	MEMORY	LOW	HIGH
I/O (15)	BLE	O	MEMORY	LOW	HIGH

2.8 Analog Baseband(ABB) Processor

A. General Description

IOTA is Analog Baseband (ABB)Chip supports GSM900, DCS1800, DCS, GPRS Class 10 with Digital Basband Chip(Calypso G2).

IOTA processes GSM modulation/demodulation and power management operations.

Block Description

- Audio Signal Processing & Interface
- Baseband in-phase(I), quadrature(Q) Signal Processing
- RF interface with DBB (time serial port)
- Supply voltage regulation
- Battery charging control
- Switch ON/OFF
- 1.8V/3V SIM card Interface
- 4 internal & 4external ADC channels

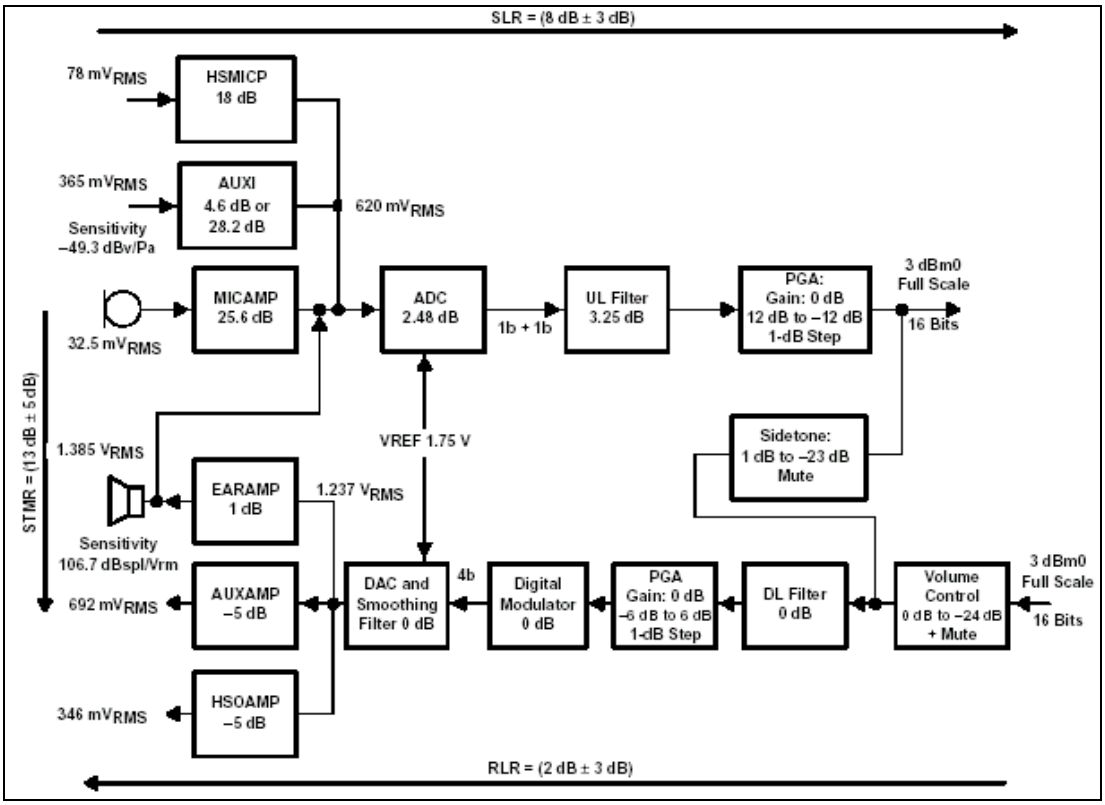
B. Audio Signal Processing & Interface

Audio signal processing is divided Uplink path and downlink path..

The uplink path amplifies the audio signal from MIC and converts this analog signal to digital signal and then transmit it to DBB Chip. This transmitted signal is reformed to fit in GSM Frame format and delivered to RF Chip. MICBIAS is 2.0Vlevel.

The downlink path amplifies the signal from DBB chip and outputs it to Receiver(or Speaker).

Figure11 Audio Interface Block Diagram



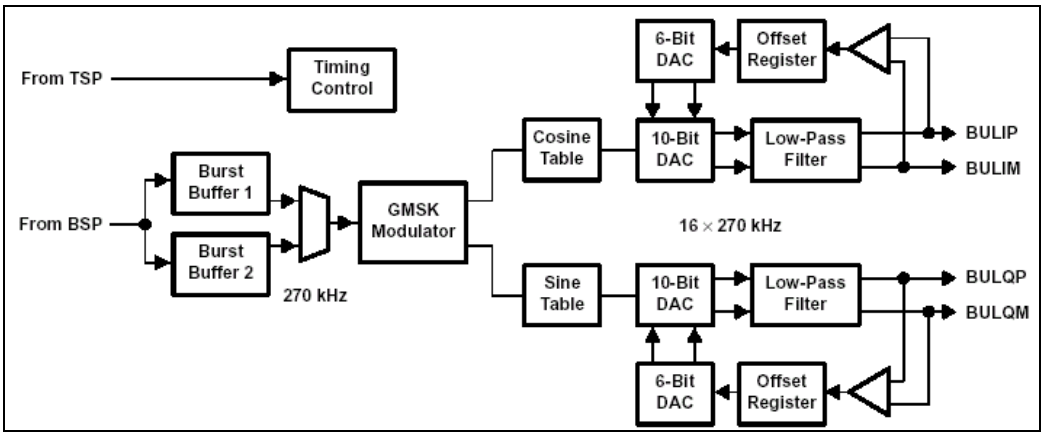
C. Baseband Codec(BBC)

Baseband codec is composed of baseband uplink path(BUL) and baseband downlink path(BDL).

BUL makes GMSK(Gaussian Minimum Shift Keying) modulated signal which has In-phase(I) component and quadrature(Q) component with burst data from DBB. This modulated signal is transmitted through RF section via air.

BDL process is opposite procedure of BUL. Namely, it performs GMSK demodulation with input analog I&Q signal from RF section, and then transmit it to DSP of DBB chip with 270.833kHz data rate through BSP.

Figure12 Baseband Codec Block Diagram



D. Voltage Regulation(VREG)

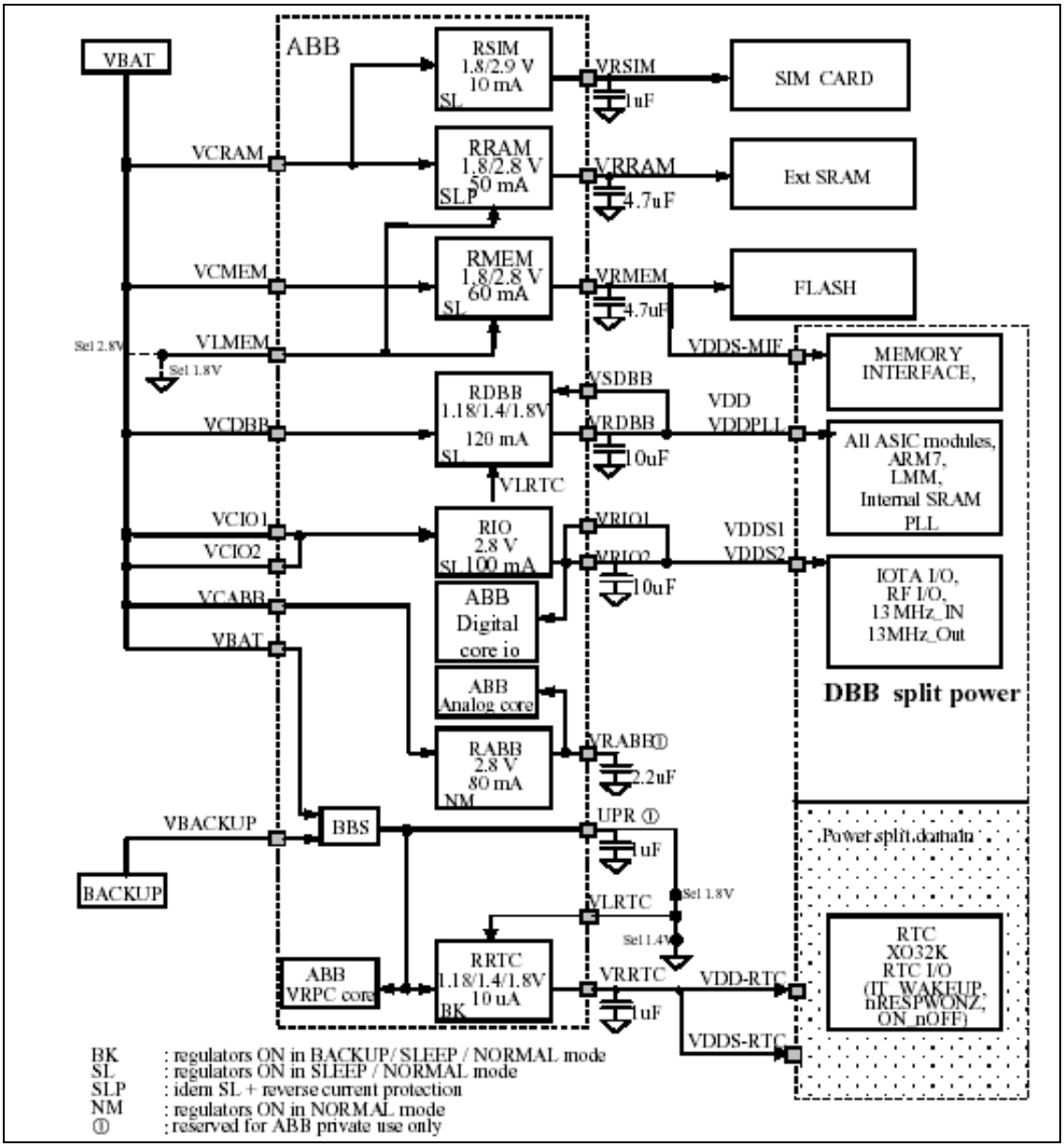
There are 7 LDO(Low Drop Output) regulators in ABB chip.

The output of these 7 LDOs are as following table. (Figure13) shows the power supply related blocks of DBB/ABB and their interfaces in NEO200_850TN.

Table 5 LDO Output Table

	Output Voltage	Usage
V DBB	1.5V	Digital Core of DBB
V IO	2.8V	Calypso I/O
V FLASH	2.8V	External ROM
V SRAM	2.8V	External RAM
V ABB	2.8V	Analog Block of ABB
V SIM	2.85	SIM card driver
V RTC	1.5V	RTC

Figure13 Power Supply Scheme



E. ADC Channels

ABB ADC block is composed of 4 internal ADC(Analog to Digital Converter) channels and 4 external ADC channel. This block operates charging process and other related process by reading battery voltage and other analog values.

Table 6 ADC Channel Spec.

ADC 8 channels		
Resource	**Name**	**Description**
VCHG	VCHG	Charging Management
VBAT	VBAT	
ICHG	ICHG	
VBACKUP	VBACKUP	Backup Battery

ADIN1	JACK_DETECT	Jack plug-in detect
ADIN2	BATT_TEMP	Battery Detect
ADIN3	TEMPSENSE	Temperature Sensing
ADIN4	HOOK_DETECT	HOOK_DETECT

F. Charging

Charging block in ABB processes charging operation by using VBAT, ICHG value through ADC channel. Battery Block Indication and SPEC of NEO200_850TN is as follow.

1. Charging method : CC-CV
2. Charger detect voltage : 4.2V
3. Charging time : 2h30min
4. Charging current : 500mA
5. CV voltage : 4.2V
6. Cutoff current : 50mA
7. Recharge voltage : 4.15V
8. Low battery alarm
   a. Idle : 3.62V
   b. Dedicated : 3.50V
9. Low battery alarm interval :
   a. Idle : 3min
   b. Dedicated:1min
10. Switch-off voltage : 3.35V

G. Switch ON/OFF

NEO200_850TN Power State : Defined 4cases as follow

- Power-ON : mobile is powered by main battery or backup battery.
- Power-OFF : mobile isn't any battery.
- Switch-ON : mobileis powered and waken up from switch-off state.
- Switch-OFF : mobile is powered to maintain only the permanent function(ULPD).

To enter into Switch-ON state, one of followinf 4 condition is satisfied.

- **PWR-ON** pushed after a debouncing time of 30ms.
- **ON_REMOTE** : After debouncing, when a falling edgeis detected on RPWON pin.
- **IT_WAKE_UP** : When a rising edge is detected on RTC_ALARM pin.
- **CHARGER_IC** :When a charger voltage is above VBAT+0.4V on VCHG.

H. Memories

192Mbit Flash + 64Mbit pSDRAM

16 bit parallel data bus

ADD01 ~ ADD22

I. Display & FPCB Interface

LCD module include:

dual LCD : 128*160 dots Main LCD, 96*96 dots Sub LCD

LCD Backlight : white LED Backlight

LCD module is connected to main board with 64 pin.

Table 7 FPCB Interface Spec.

PIN No	Pin Name	Function	PIN No	Pin Name	Function
1	VBAT	DC VOLT	**33**	MIC-	Mic -
2	VBAT1	DC VOLT	**34**	MIC+	Mic +
3	BACKUP_BATT	Back up battery connect	**35**	SPK L-	Left speaker -
4	GND1	Ground	**36**	SPK L+	Left speaker +
5	DL(0)	LCD Data line	**37**	HPOUT_R	Earphone right
6	DL(2)	LCD Data line	**38**	GND5	Ground
7	DL(4)	LCD Data line	**39**	S_DATA_C	Sccb serial interface data IO
8	DL(6)	LCD Data line	**40**	PDCLK	Pixel clk output
9	DL(8)	LCD Data line	**41**	S_CLK_C	Sccb serial interface clk
10	DL(10)	LCD Data line	**42**	DC(4)	Camera Data line
11	DL(12)	LCD Data line	**43**	DC(3)	Camera Data line
12	DL(14)	LCD Data line	**44**	DC(2)	Camera Data line
13	LCD_A(1)	Address line	**45**	DC(1)	Camera Data line
14	LC_CS_SUB	Sub LCD chip select	**46**	DC(0)	Camera Data line
15	PSEN	Camera enable	**47**	LCD_TEMP	Temp sensor
16	EN_BLUE	Blue indicator enable	**48**	LCD_RD	LCD read
17	EN_AMBER	Amber indicator enable	**49**	LCD_WR	LCD write
18	DC(5)	Camera Data line	**50**	LCD_CS_MAIN	Main LCD chip select
19	DC(6)	Camera Data line	**51**	LCD_RST	LCD RESET
20	DC(7)	Camera Data line	**52**	AVDD	Analog VDD
21	DC(8)	Camera Data line	**53**	DL(15)	LCD Data line
22	DC(9)	Camera Data line	**54**	DL(13)	LCD Data line
23	C_RESET	Camera reset	**55**	DL(11)	LCD Data line
24	PPXL_CLK	Camera clock	**56**	DL(9)	LCD Data line
25	VS_C	Vertical sync	**57**	DL(7)	LCD Data line
26	HS_C	Horizontal sync	**58**	DL(5)	LCD Data line
27	GND2	Ground	**59**	DL(3)	LCD Data line
28	SPK R+	Right speaker +	**60**	DL(1)	LCD Data line
29	SPK R-	Right speaker -	**61**	DVDD	Digital VDD
30	HPOUT_GND	Ground	**62**	LCD_BACKLIGHT	LCD backlight control
31	HPOUT_L	Earphone left	**63**	LCD_VDD1	LCD VDD
32	JACK_IN	Ear mic detection	**64**	LCD_VDD	LCD VDD

J. KeyPad Switching & Scanning

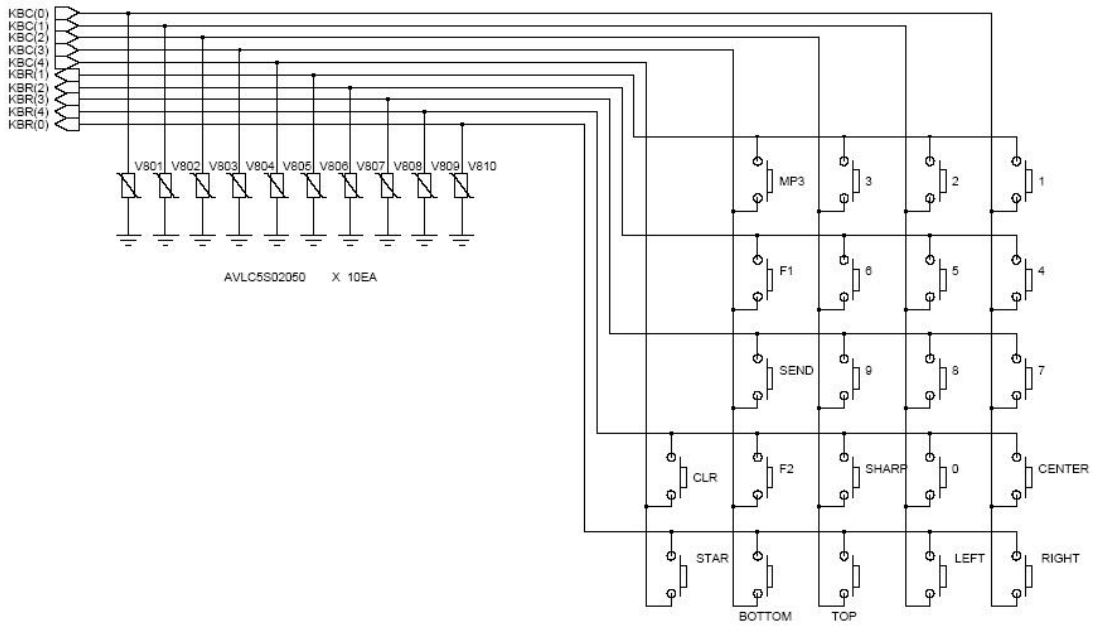
Keypad Map

Table 8 Keypad Map

	KBC0	KBC1	KBC2	KBC3	KBC4
KBR0	[►]	[◄]	[▲]	[▼]	[*]
KBR1	[1]	[2]	[3]	[MP3]	
KBR2	[4]	[5]	[6]	[F1]	
KBR3	[7]	[8]	[9]	[Send]	
KBR4	[CENTER]	[0]	[#]	[F2]	CLR

DBB supports 25 keymap and Switch-ON Key is connected directly to ABB as (Figure15).

Figure 15 Keypad Scanning Scheme



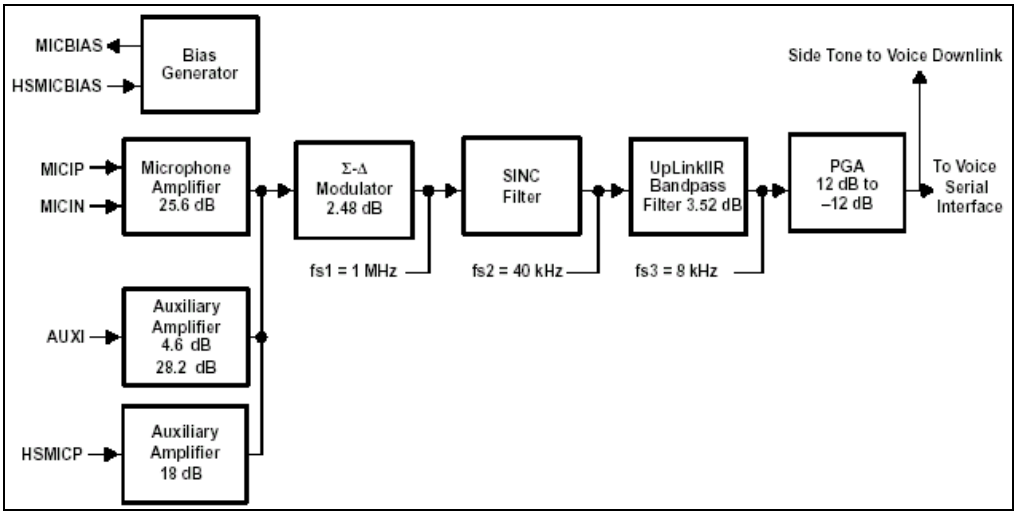
K. Audio

(Uplink)

The microphone is soldered to the main PCB. The uplink signal is passed to MICIP and MICIN pins of IOTA.

The MICBIAS voltage is supplied from IOTA(dedicated mode only). When the headset is inserted, ADC value of HOOK_DETECT(IO6) terminal is between 20 to 150 (decimal value). On detecting this, Calypso makes IOTA switches the MIC amplifier path from main to auxiliary.

Figure16 Uplink Path



(Downlink)

The downlink signal is passed from EARP and EARN pins of IOTA. When the headset is inserted and Calypso detects 'Jack pluged state' from HOOK_DETECT terminal, Calypso makes IOTA switches the downlink path from 'EARP' and 'EARN' to auxiliary outputs('AUXOP' and 'AUXON' or 'HSO').

Figure17 Downlink Path

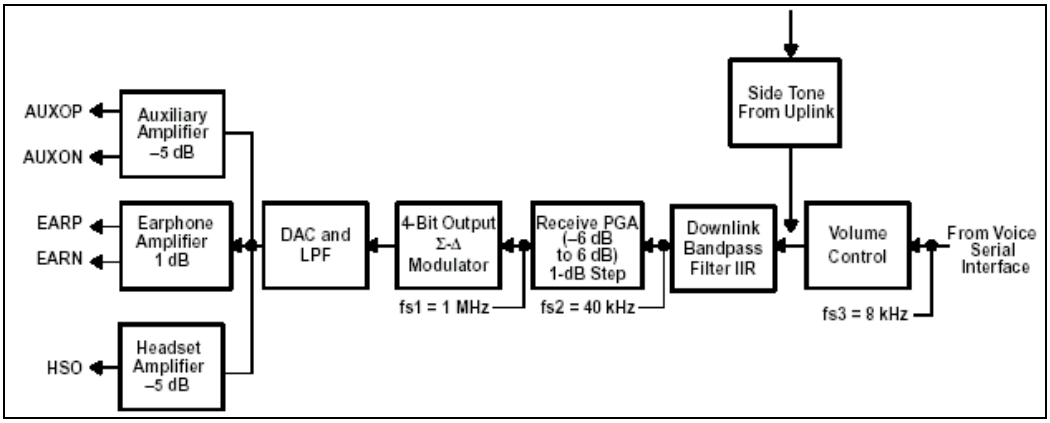
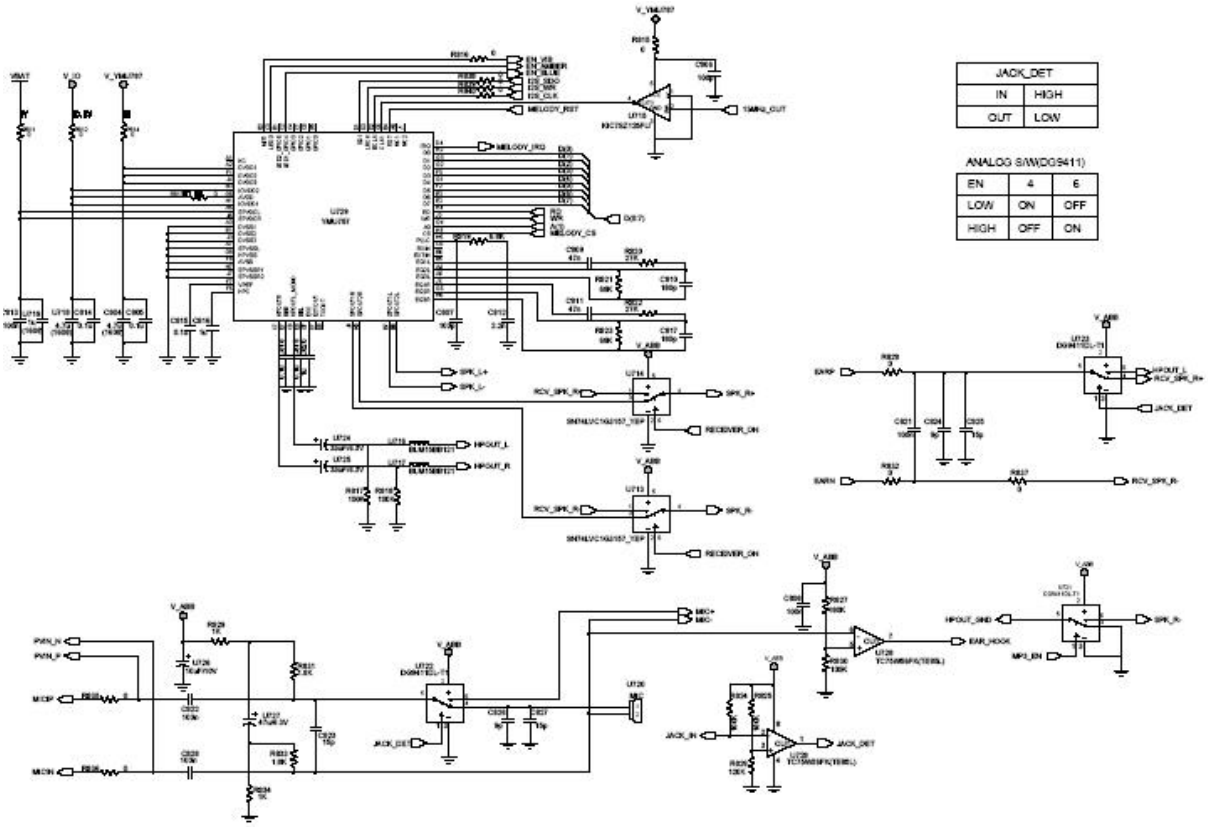


Figure18 Audio Circuit

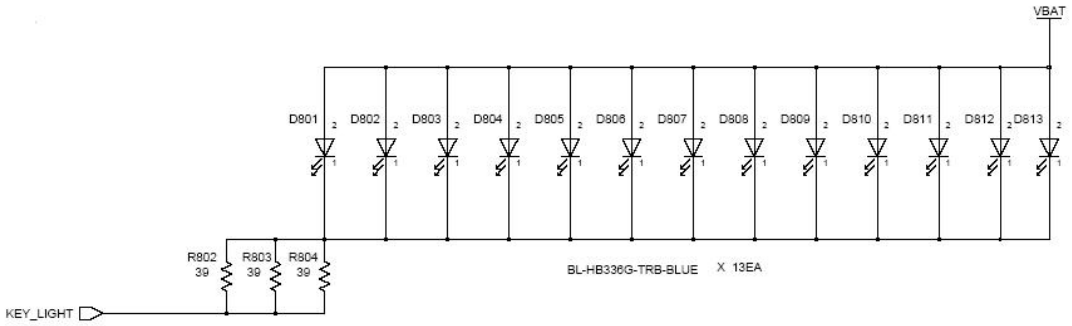


L. Keypad back-light Illumination

There are 6 Amber LEDs in Main Board for Keypad Backlight.

Keypad Back-light is driven by 'LEDB' line from IOTA .

Figure19 Keypad Back-light Scheme



M. Main_LCD Illumination

There is Backlight schematic in the LCD module for LCD backlighting. DC-DC converter is mounted in LCD module.

Figure20 Main-LCD Back-light Scheme