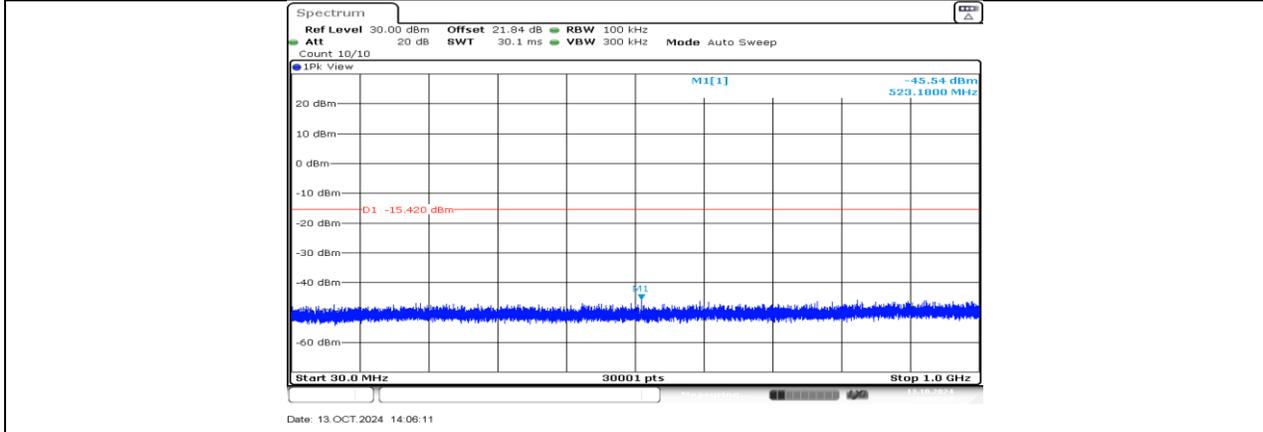
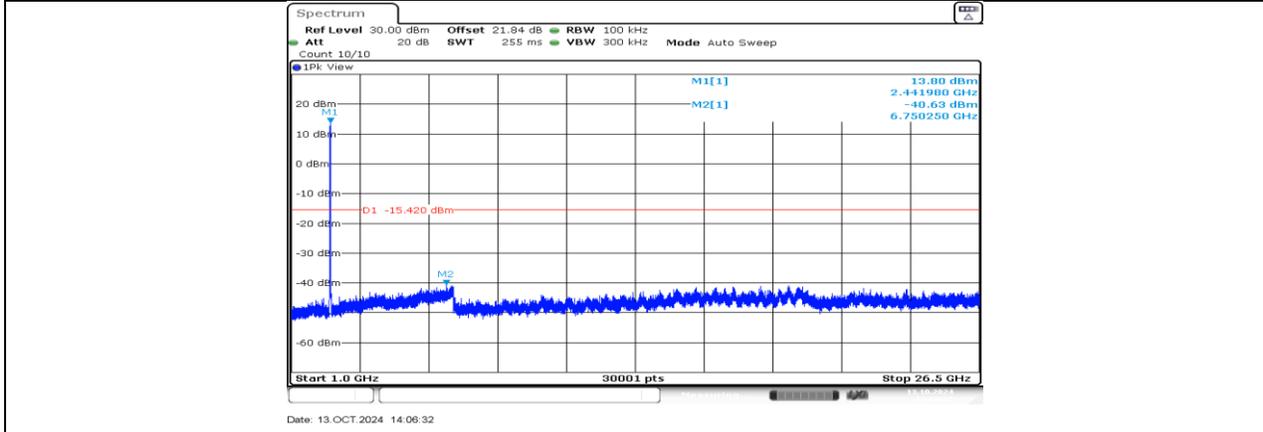


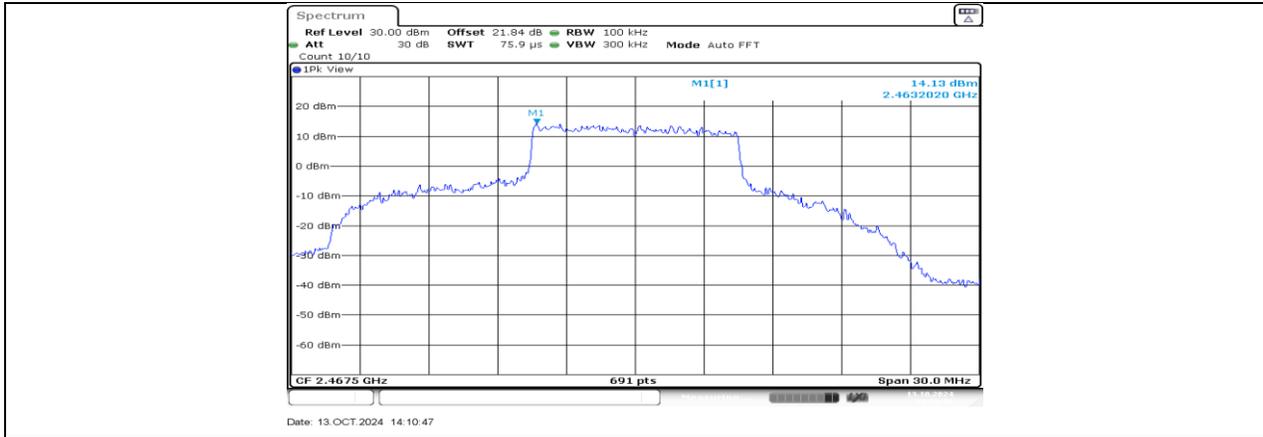
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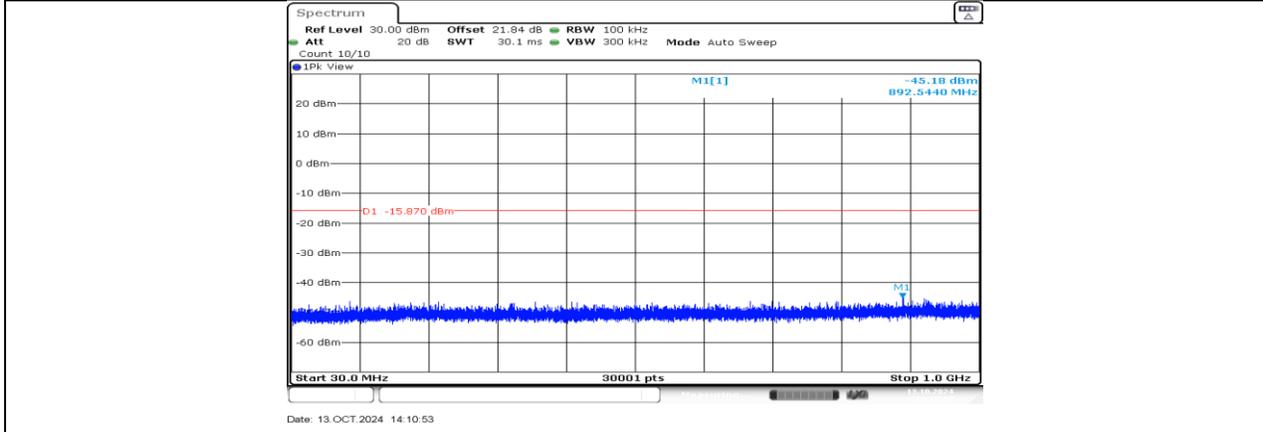
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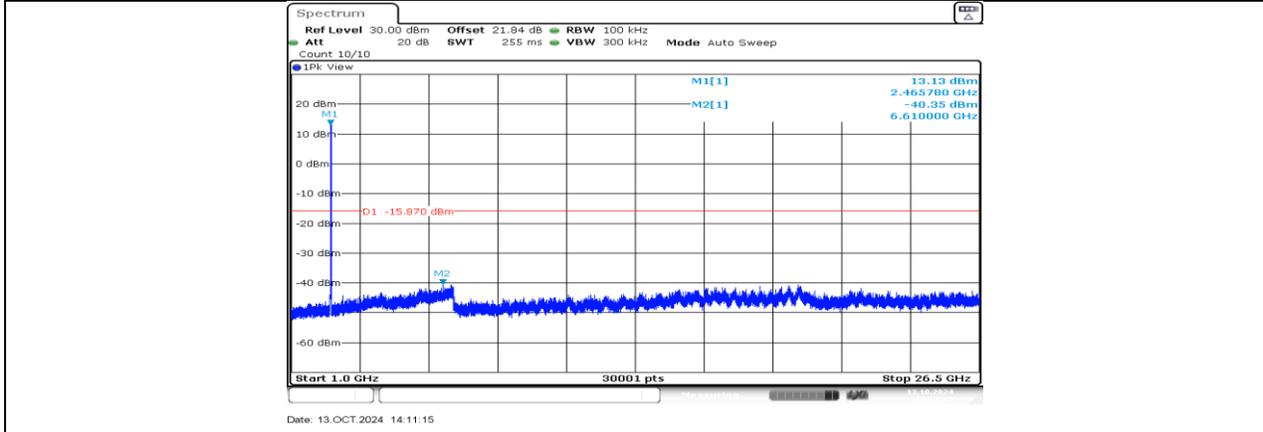
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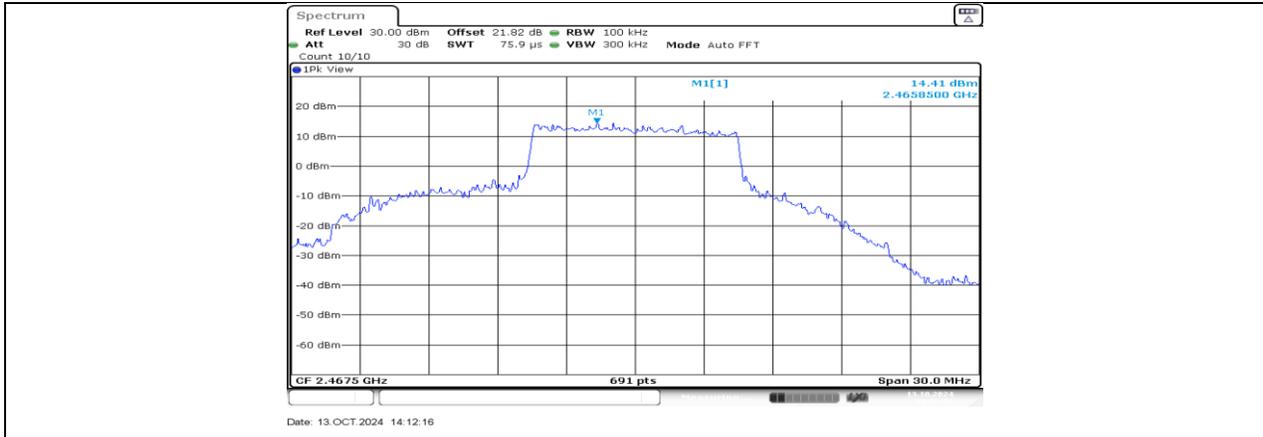
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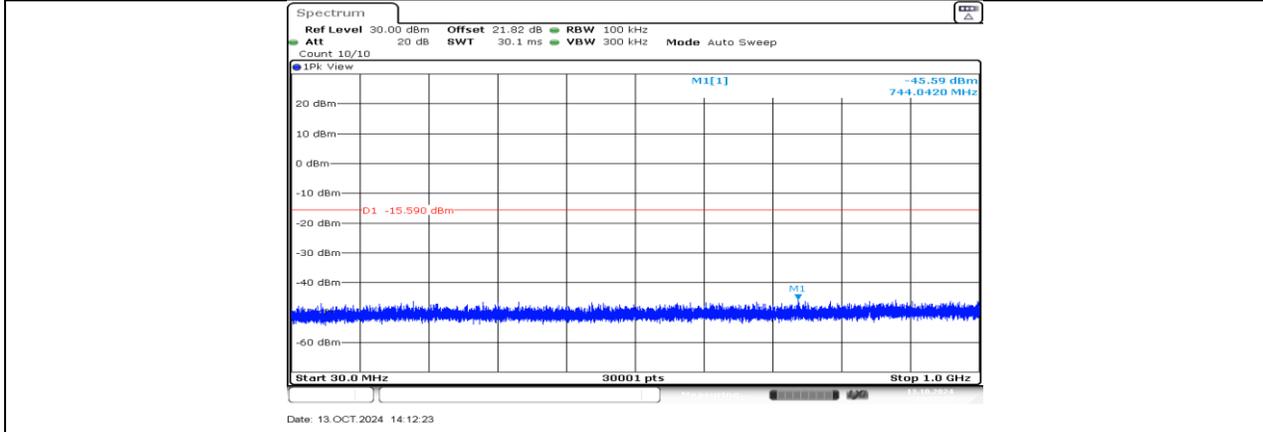
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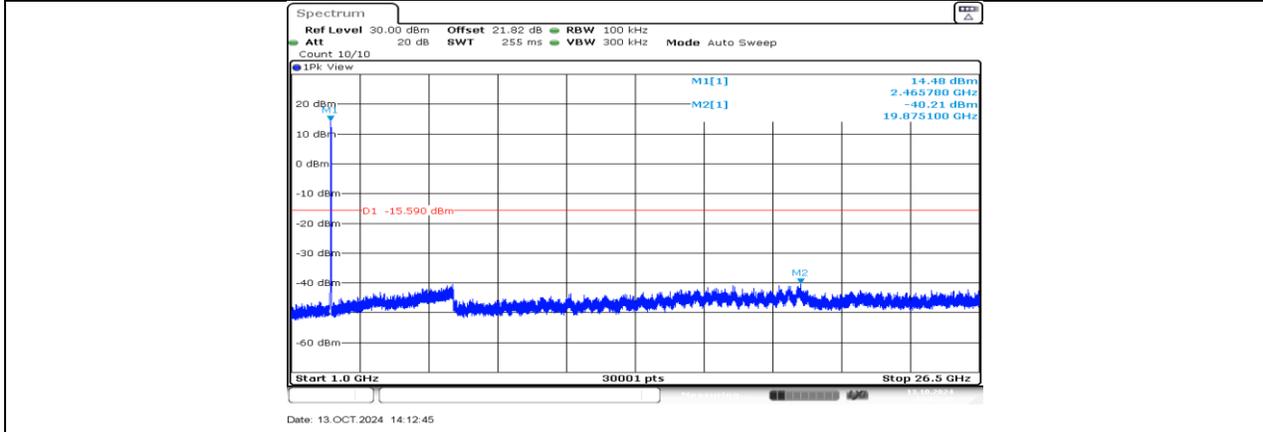
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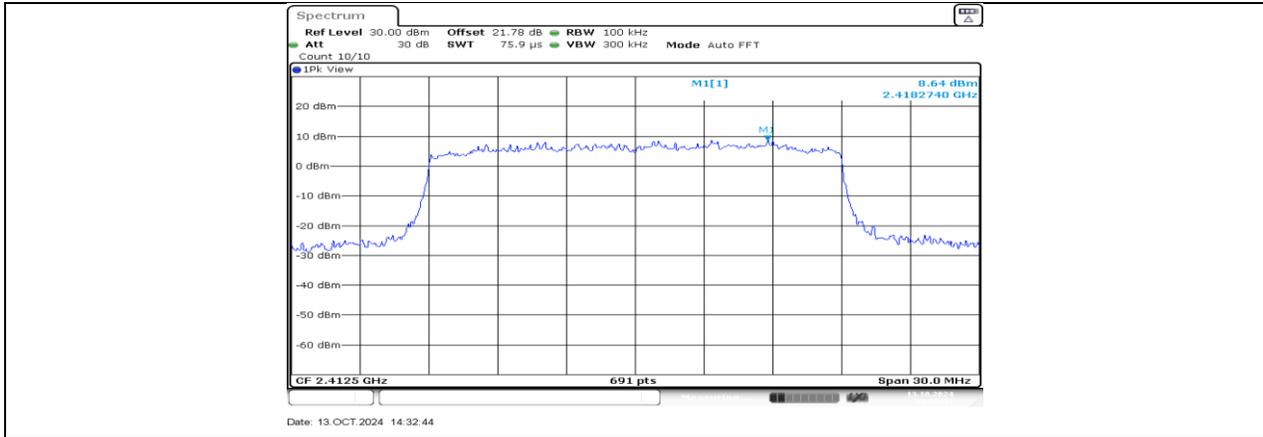
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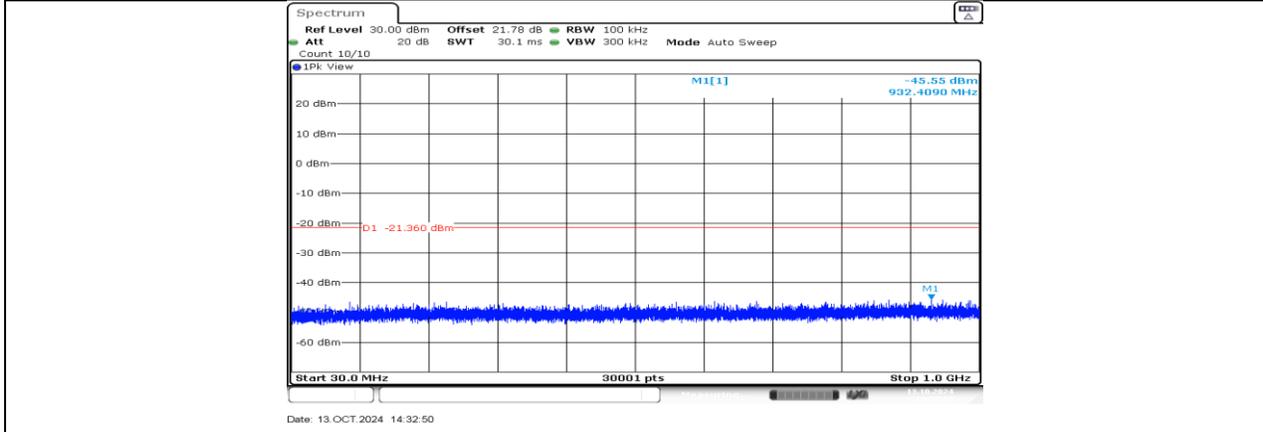
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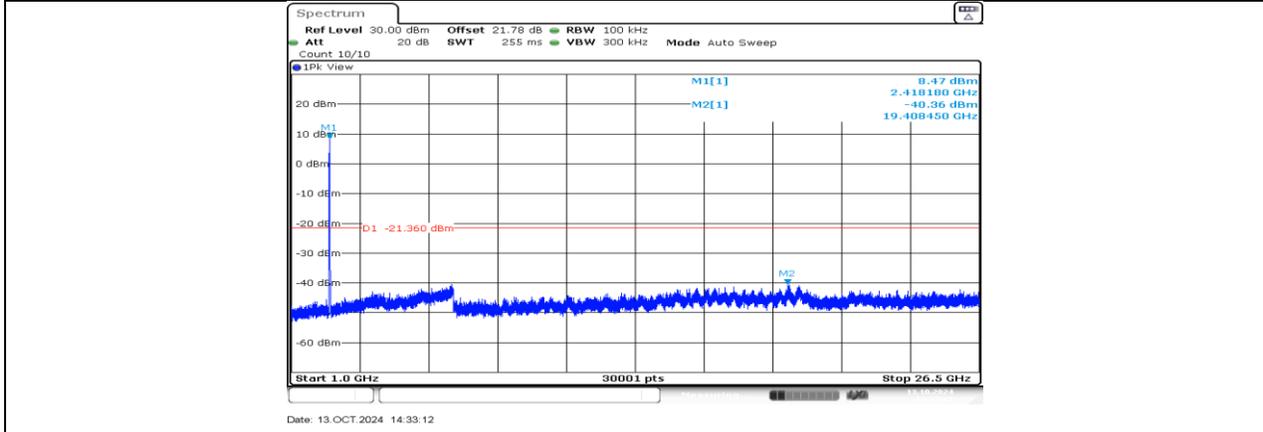
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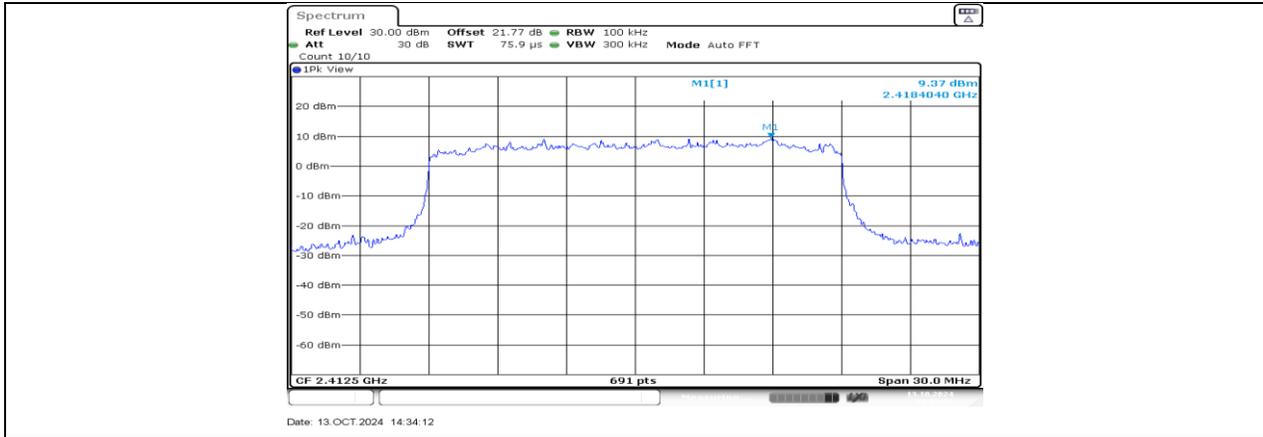
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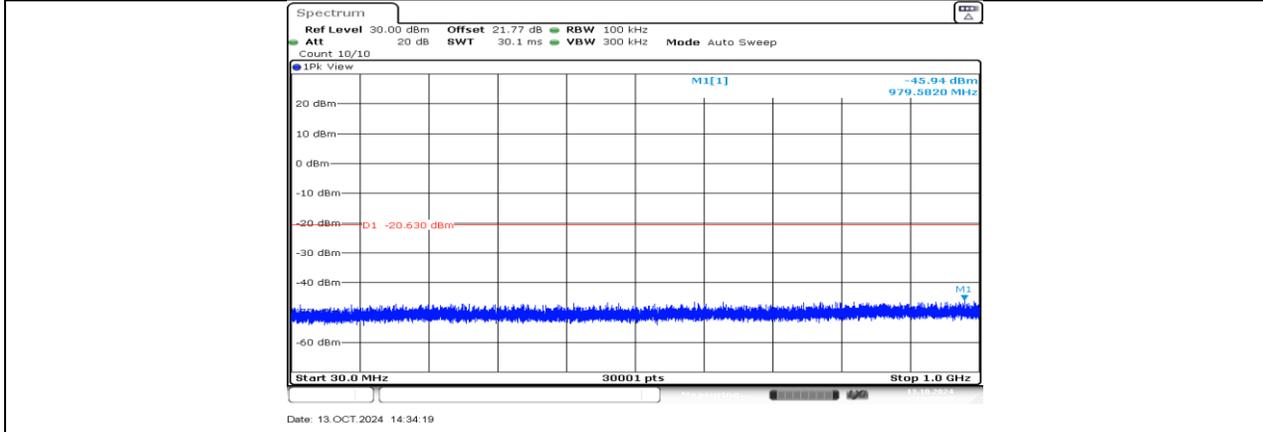
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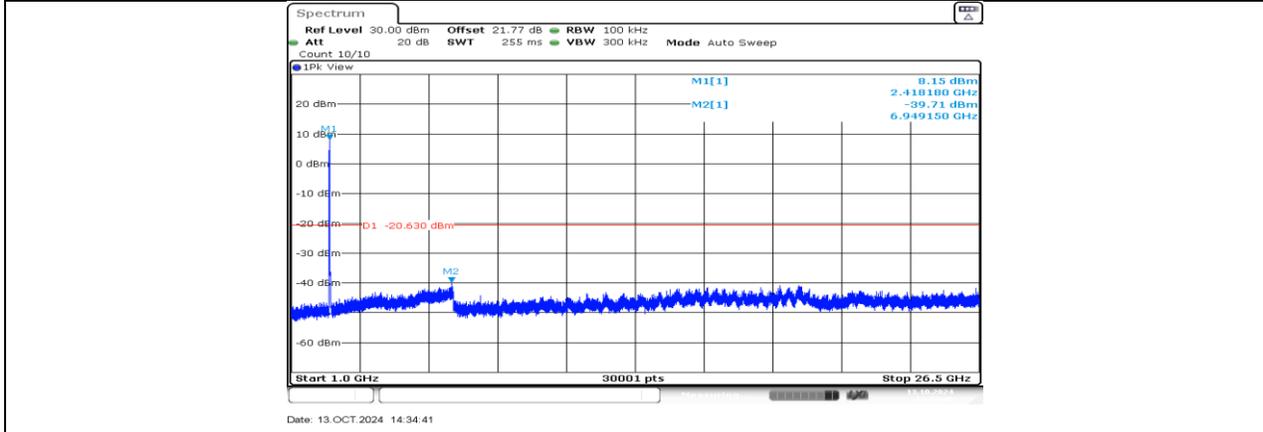
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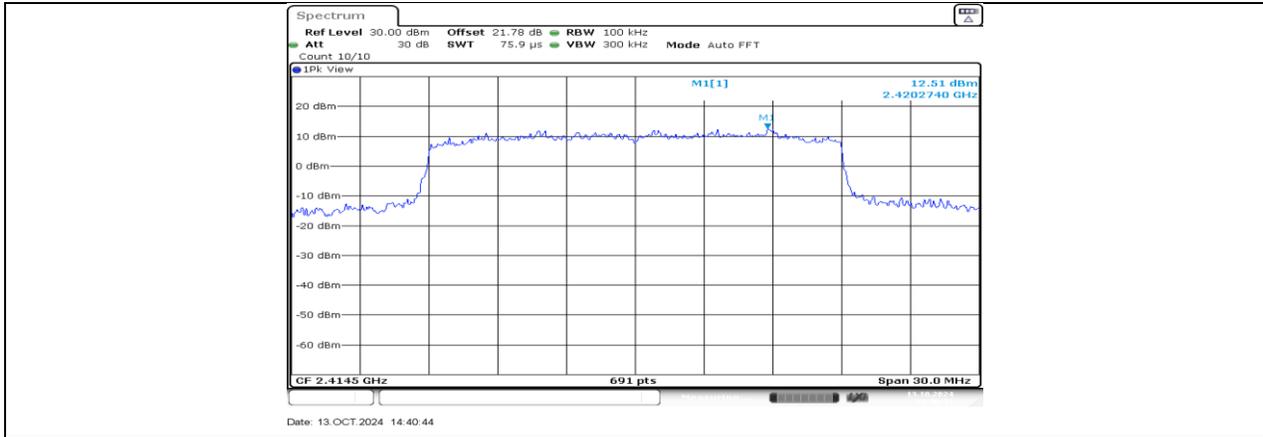
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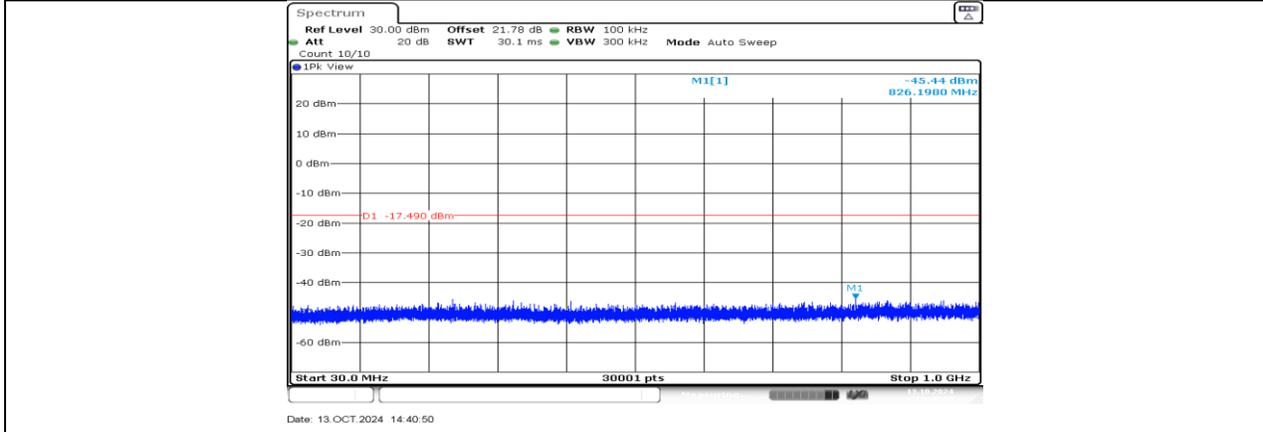
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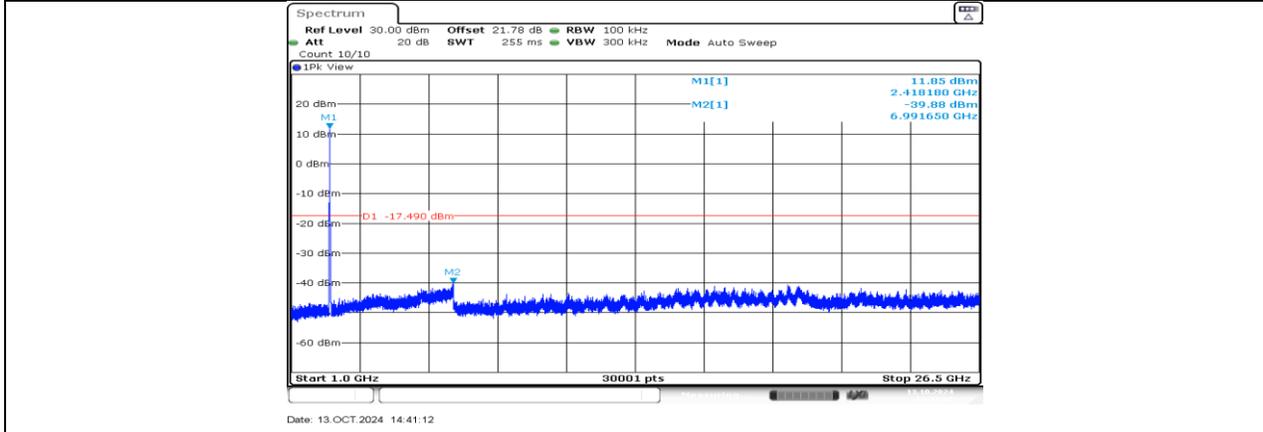
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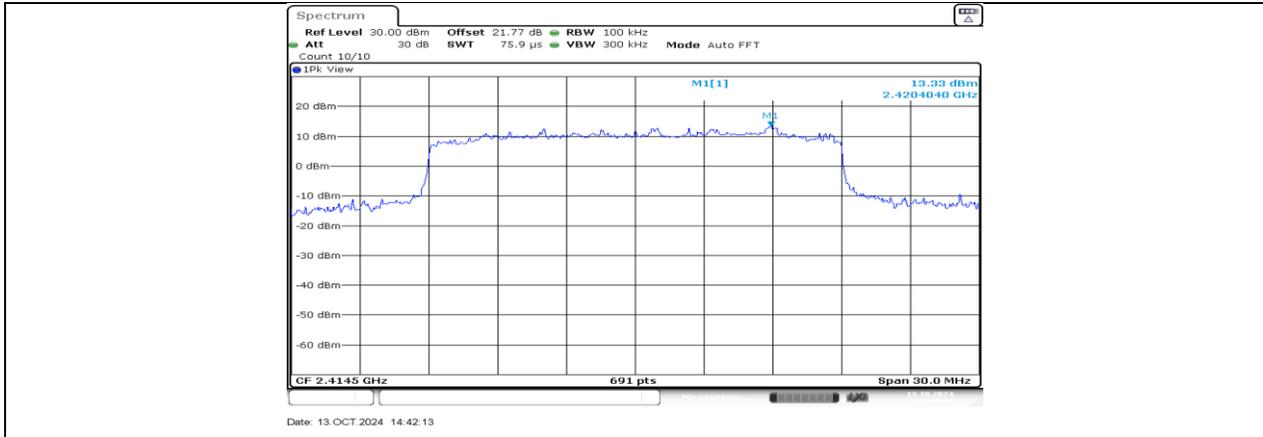
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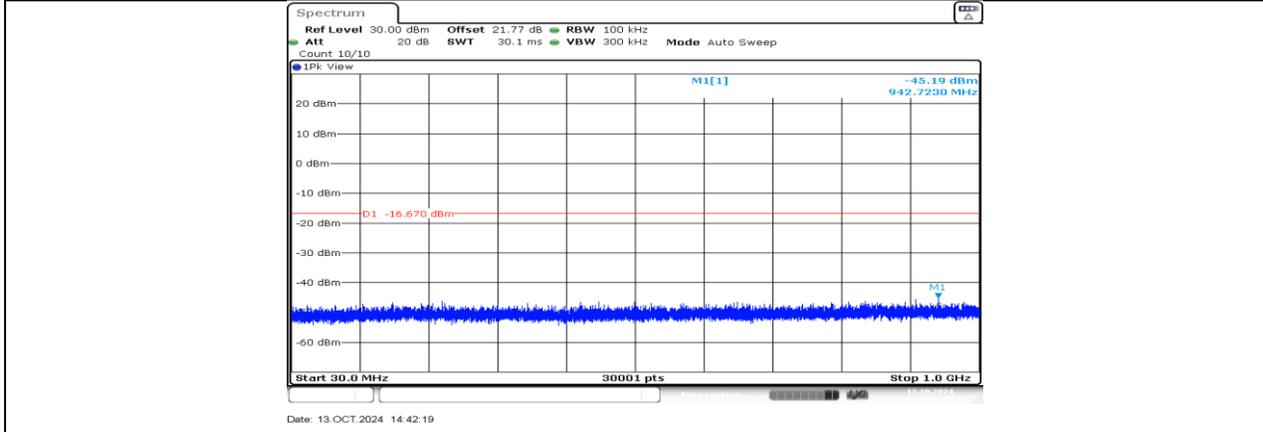
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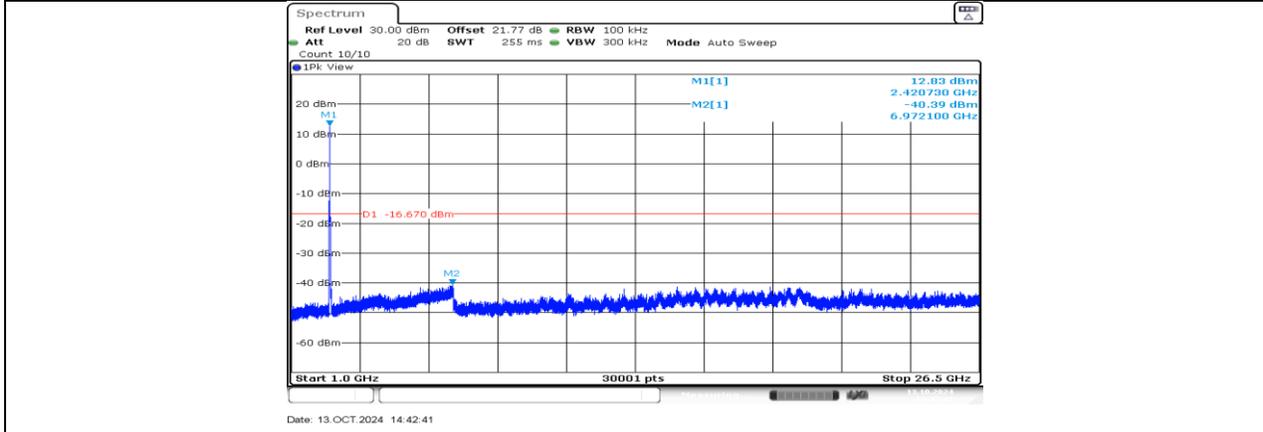
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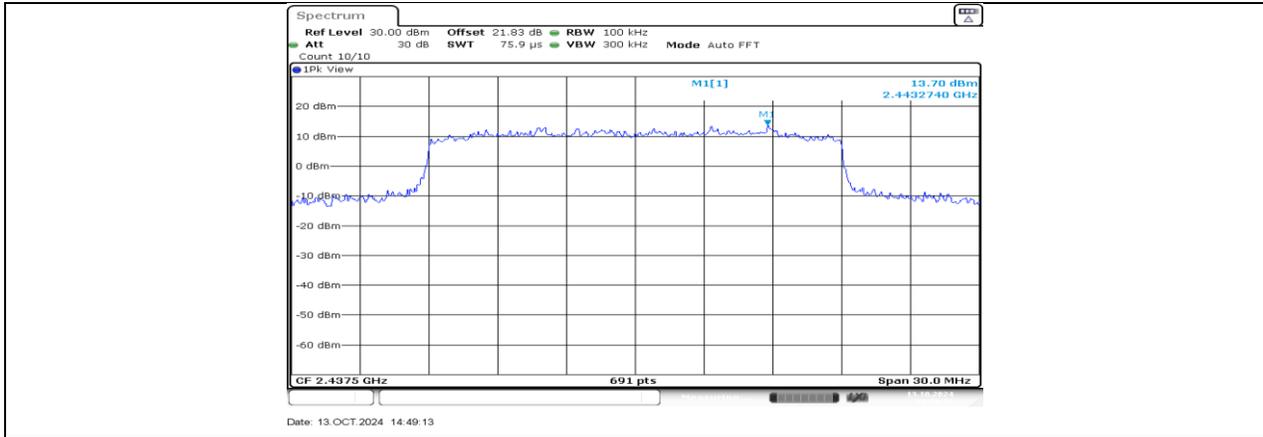
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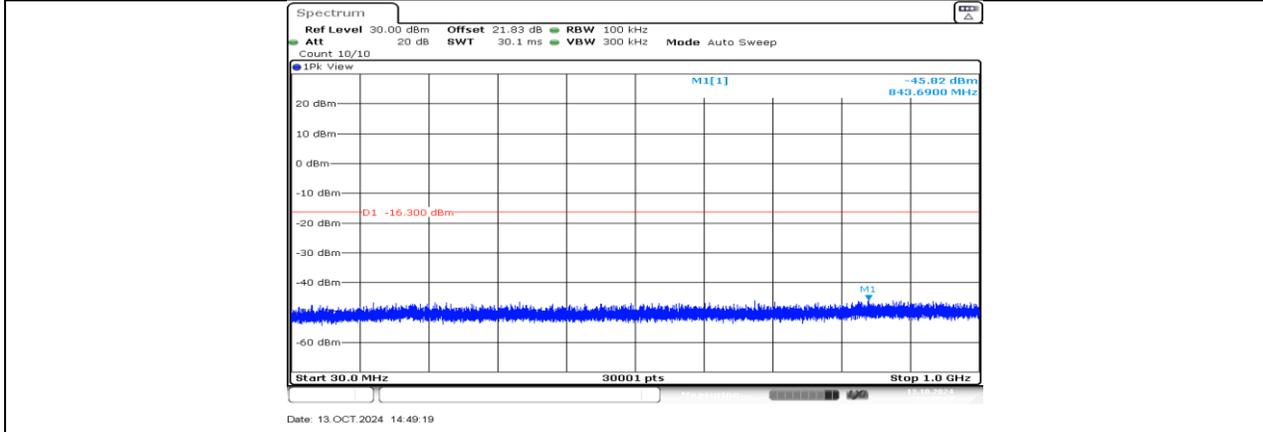
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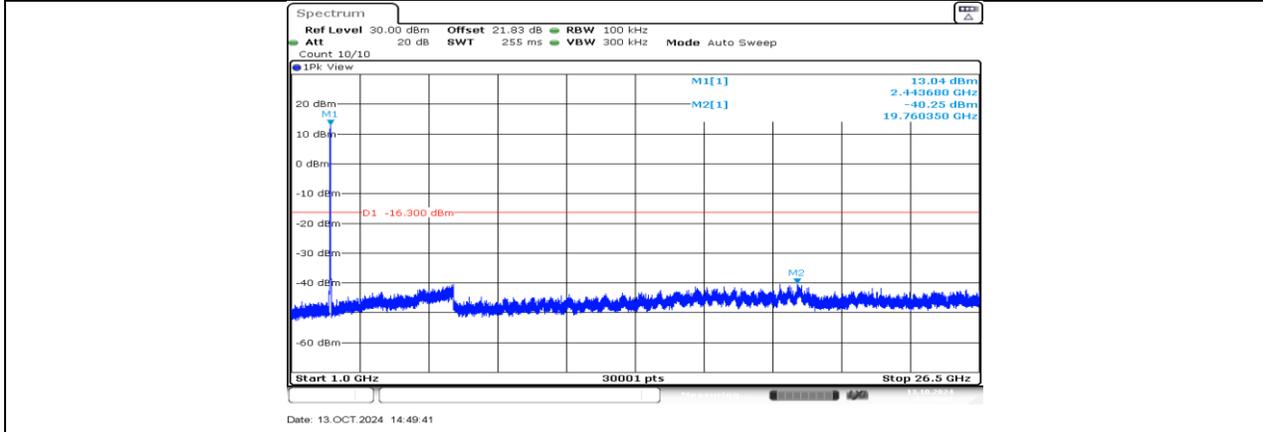
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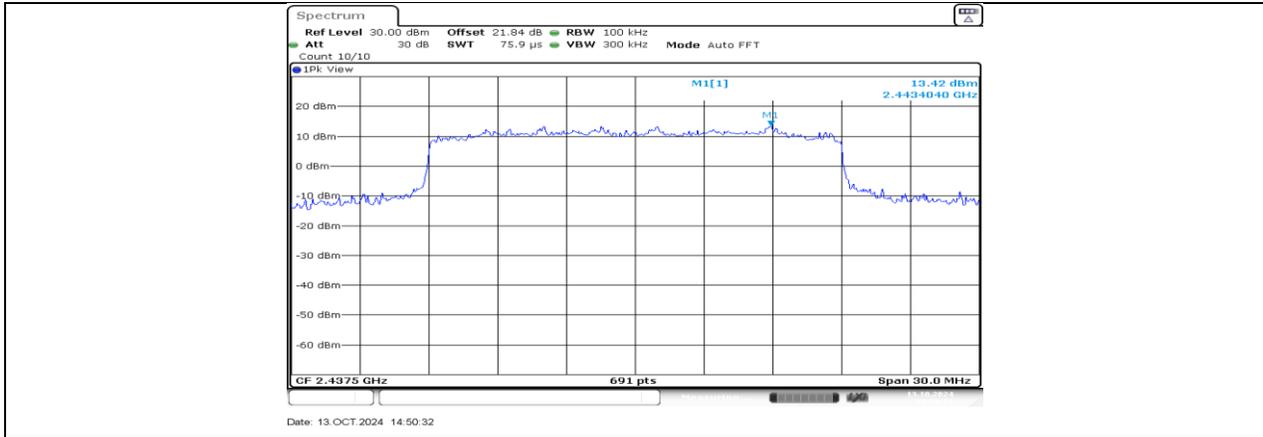
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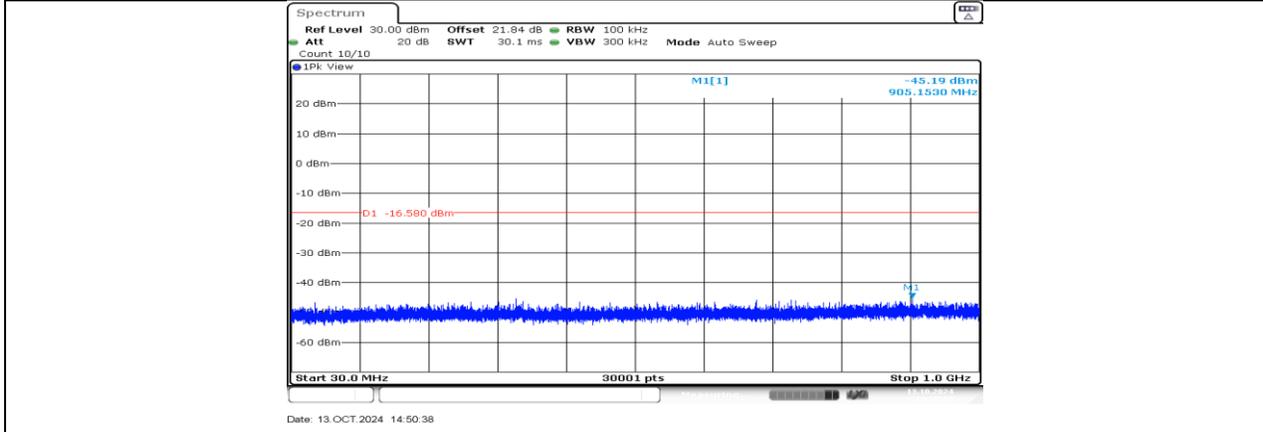
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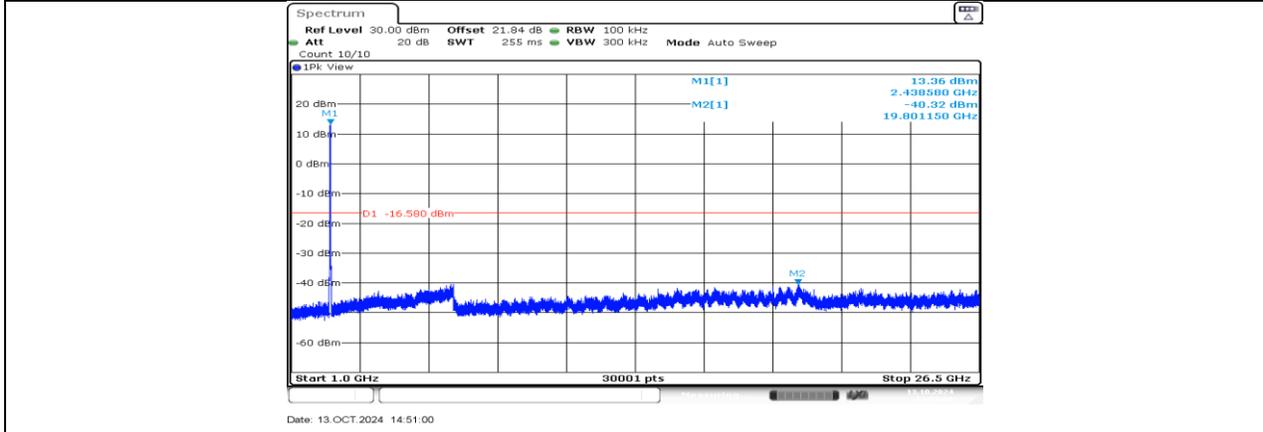
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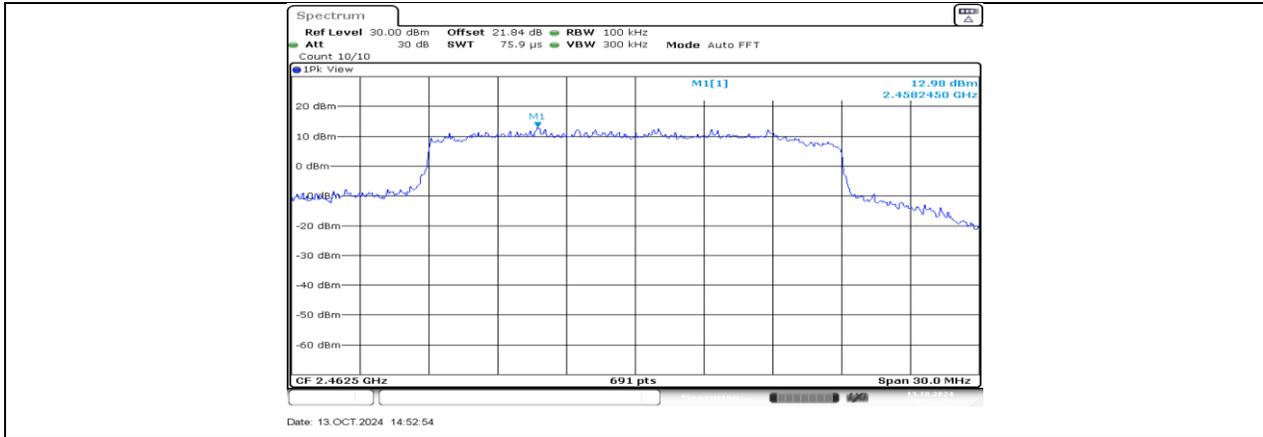
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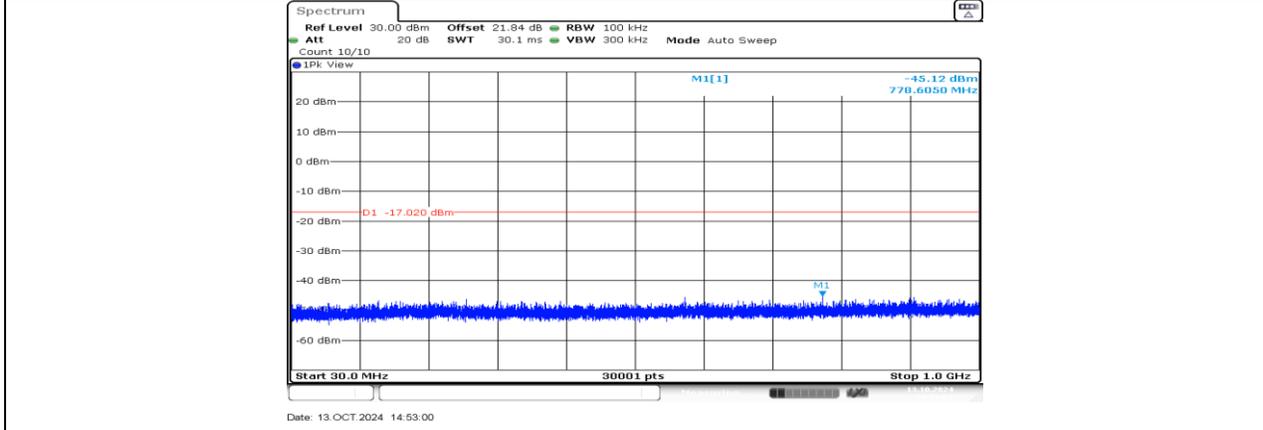
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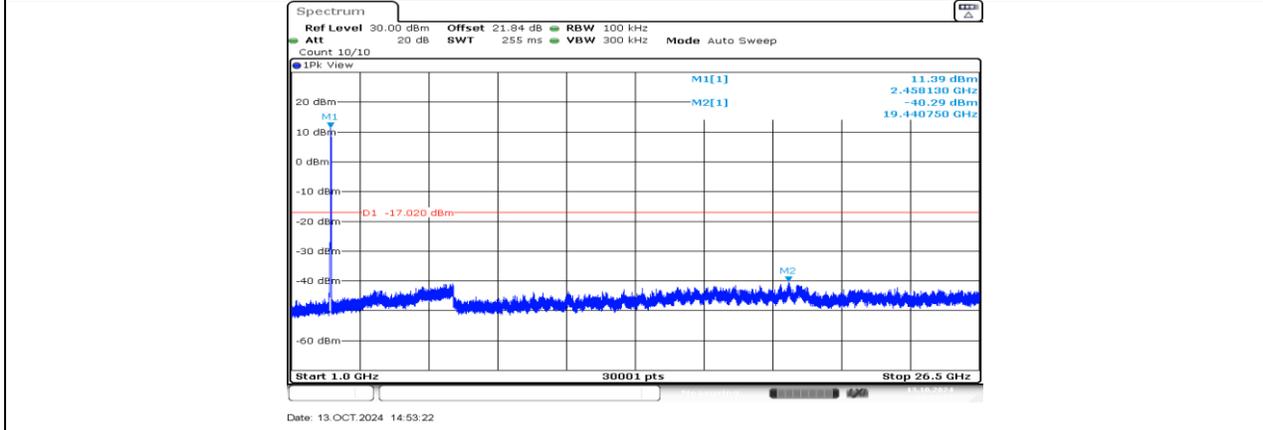
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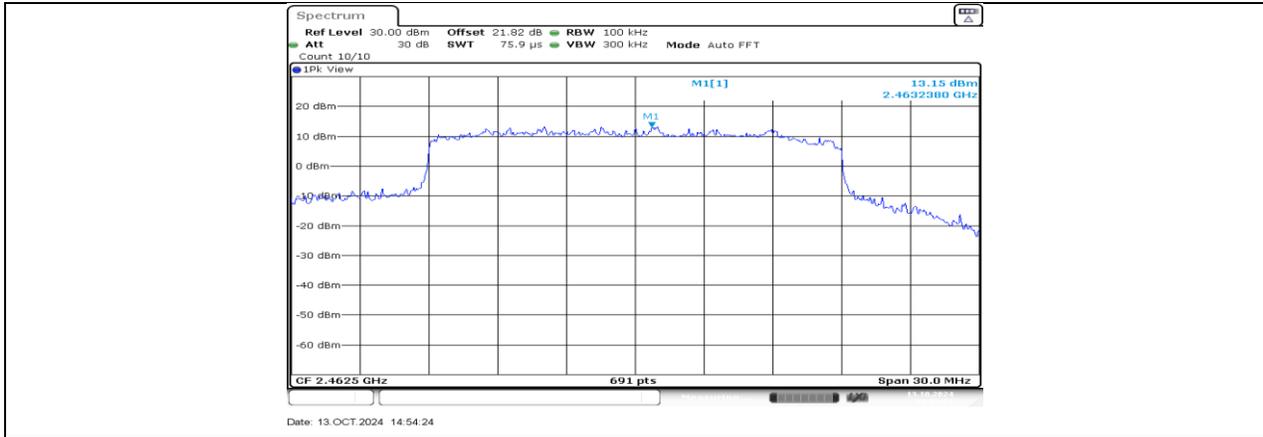
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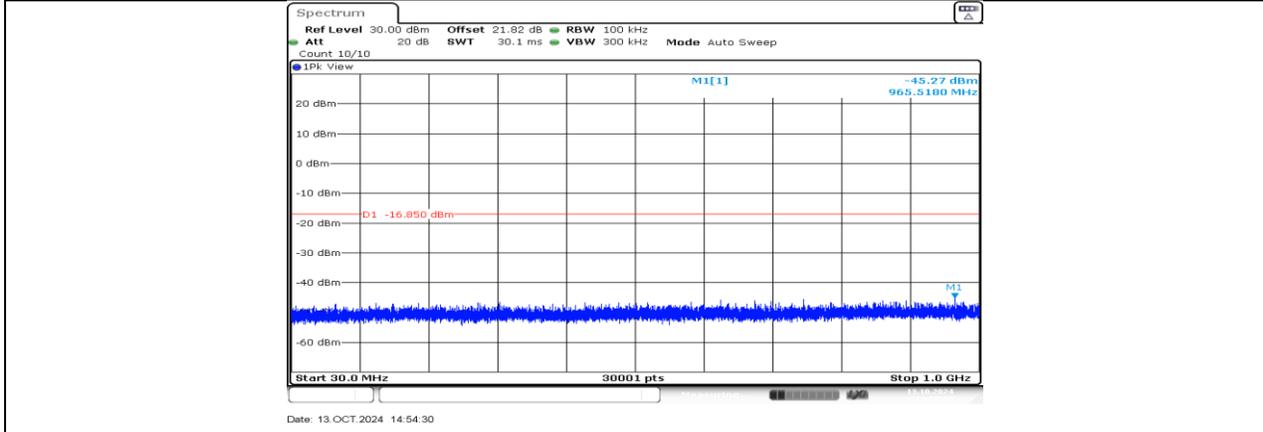
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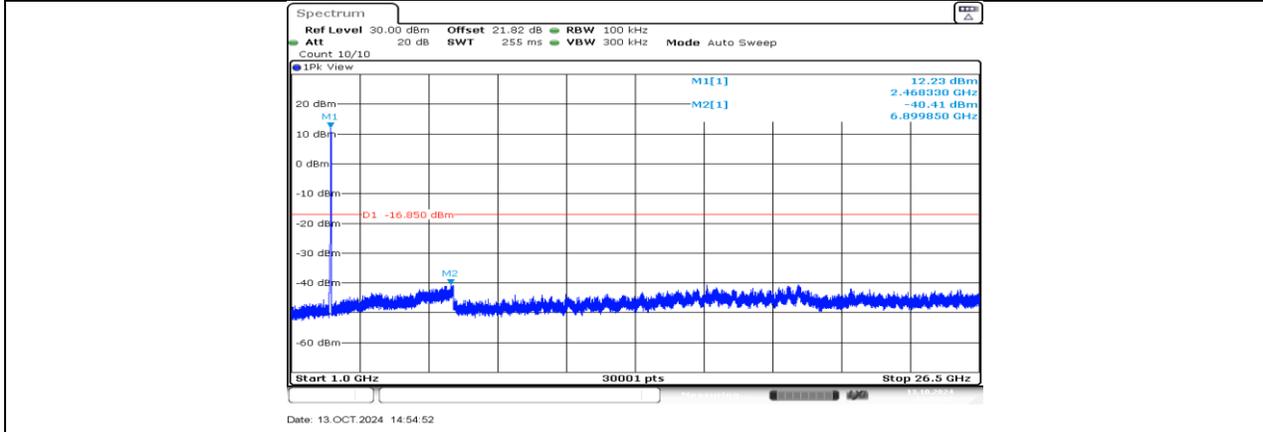
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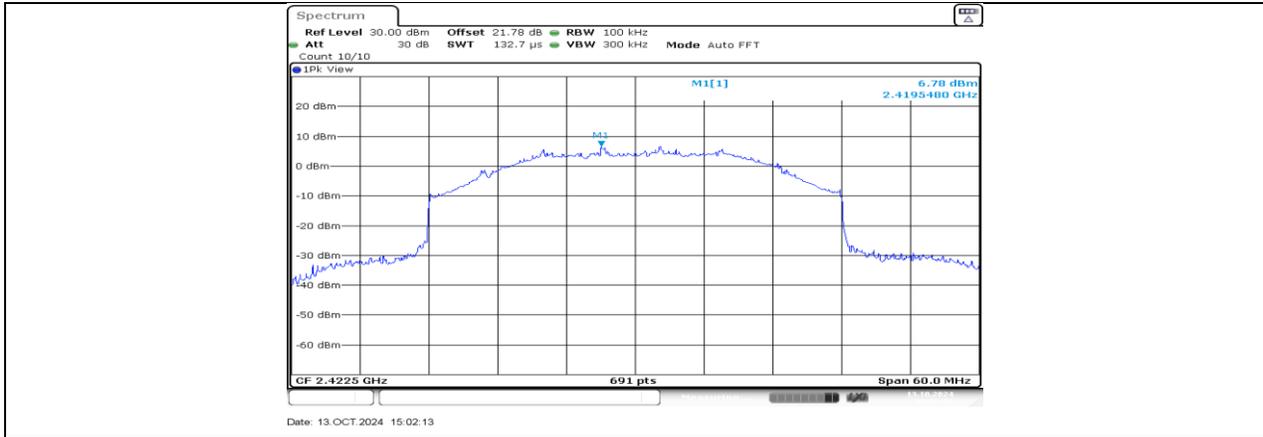
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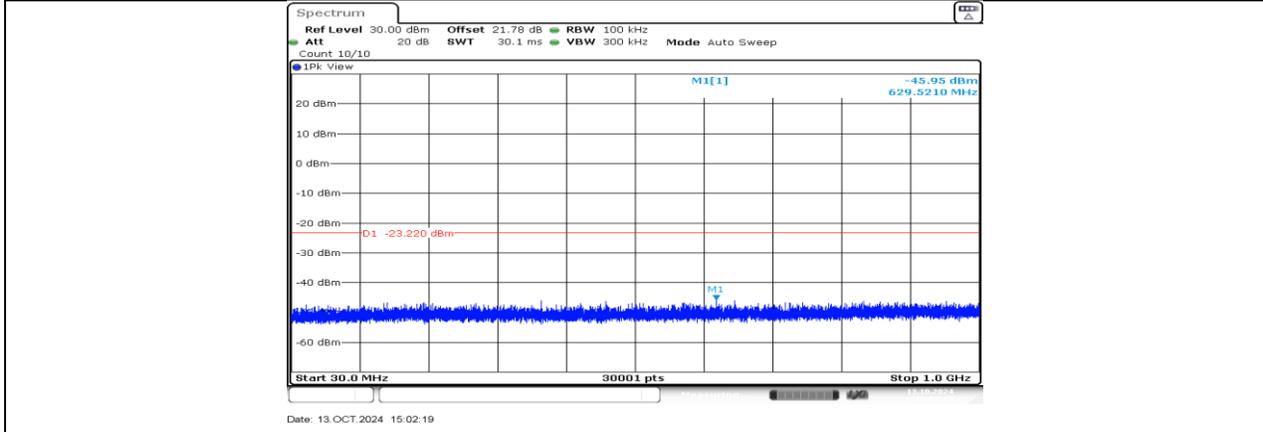
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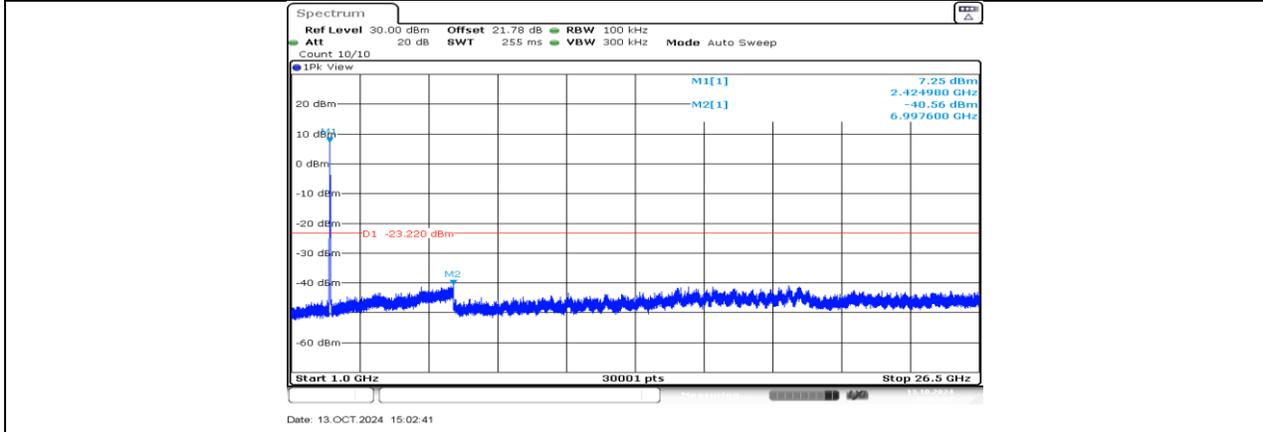
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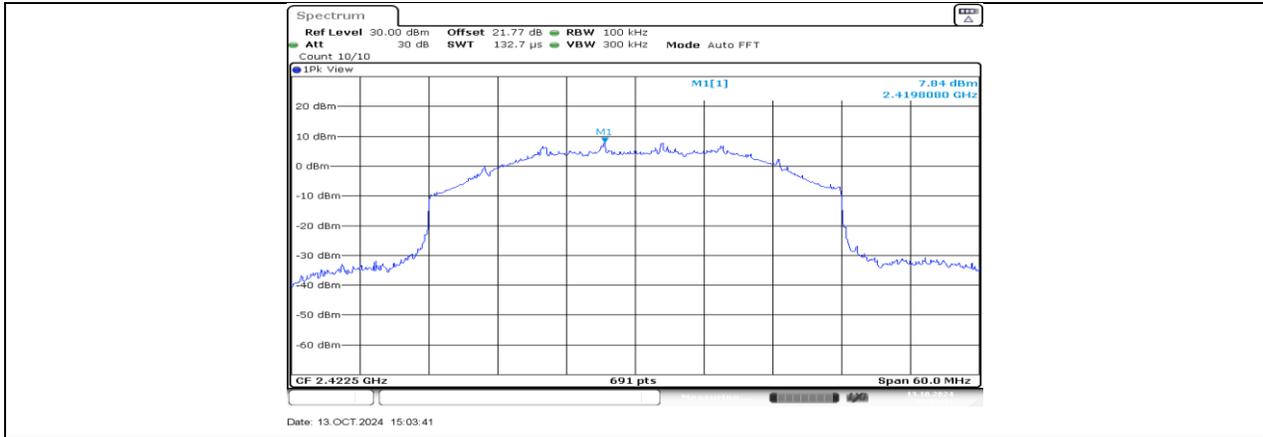
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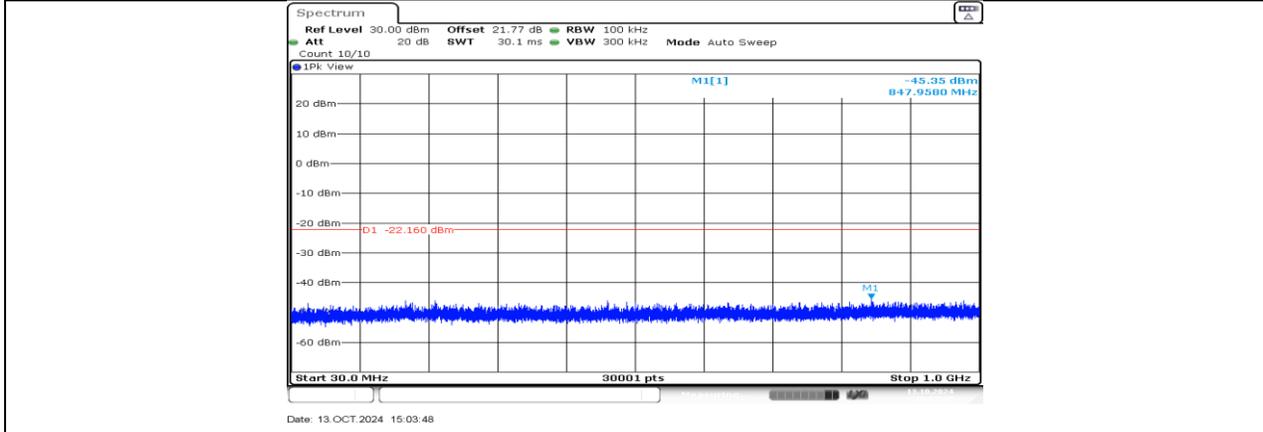
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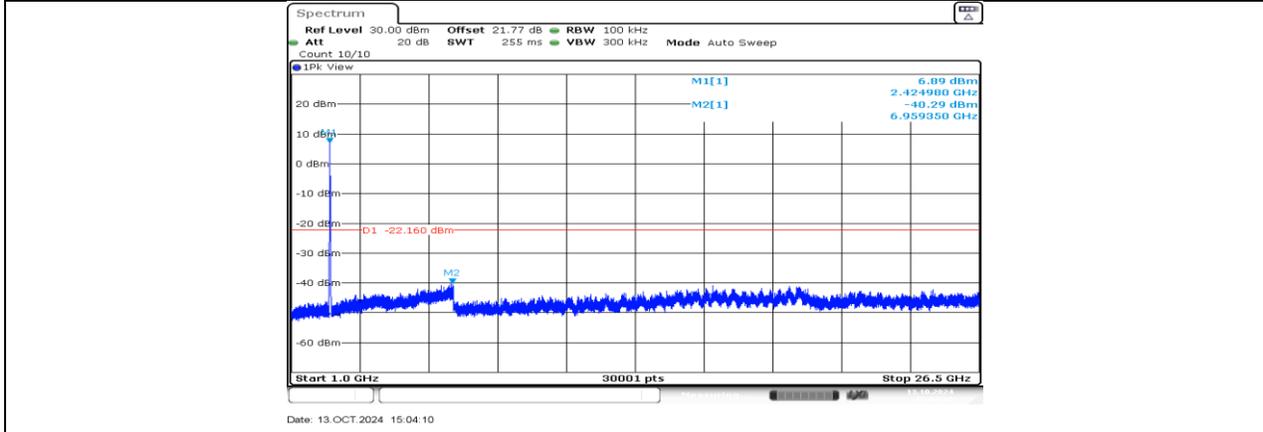
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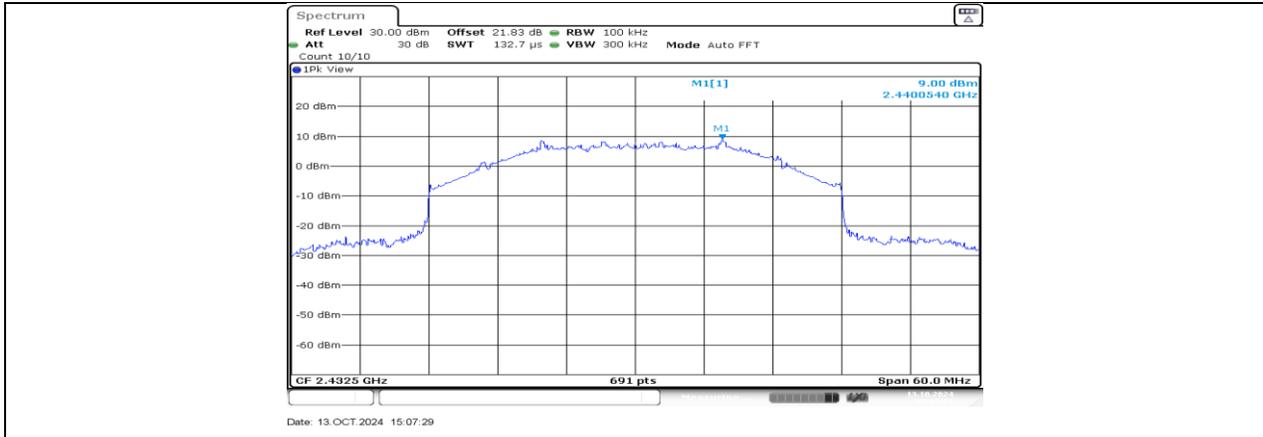
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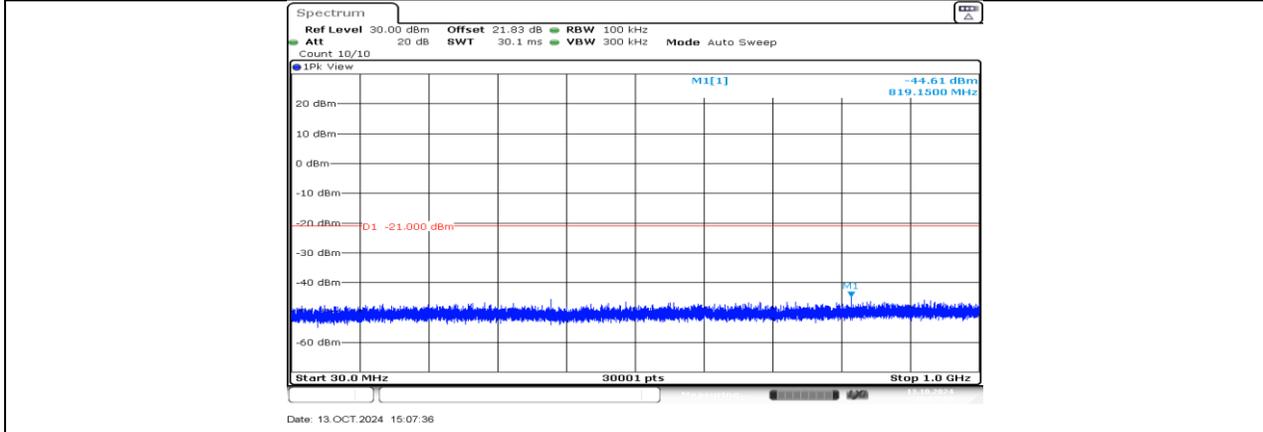
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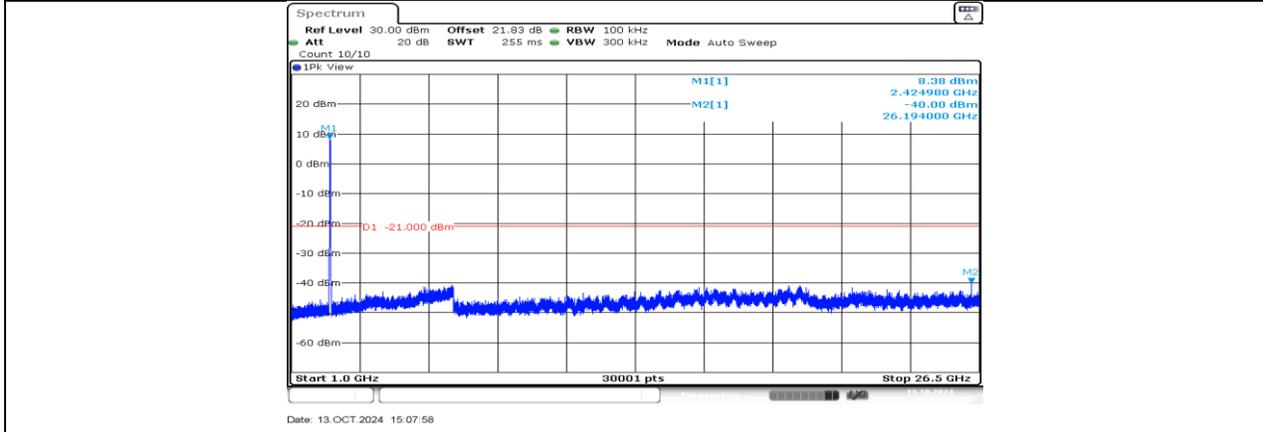
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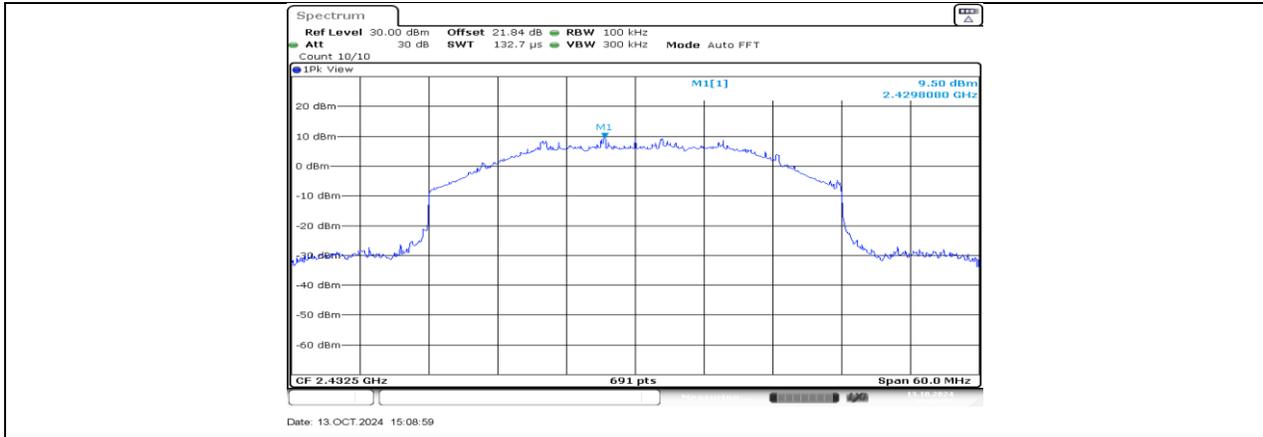
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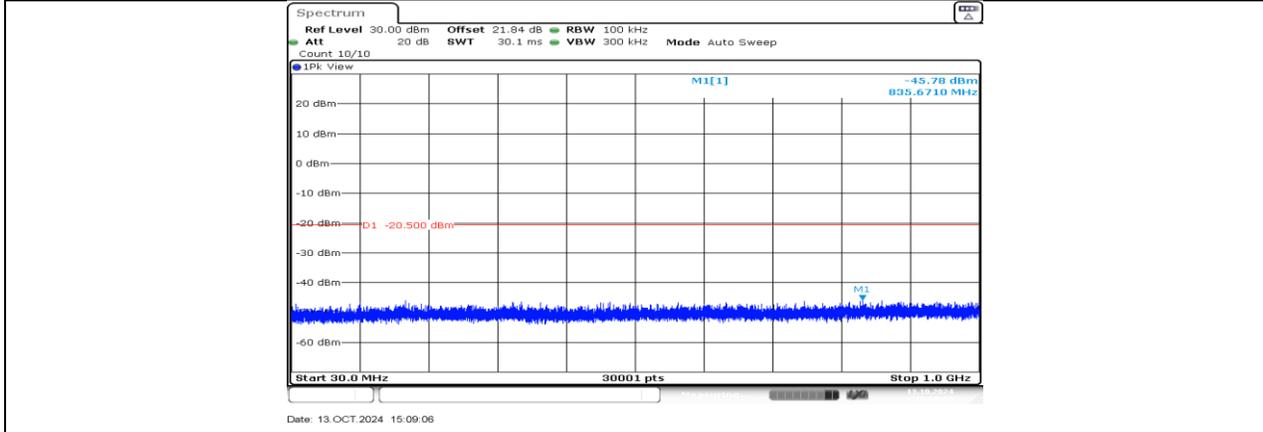
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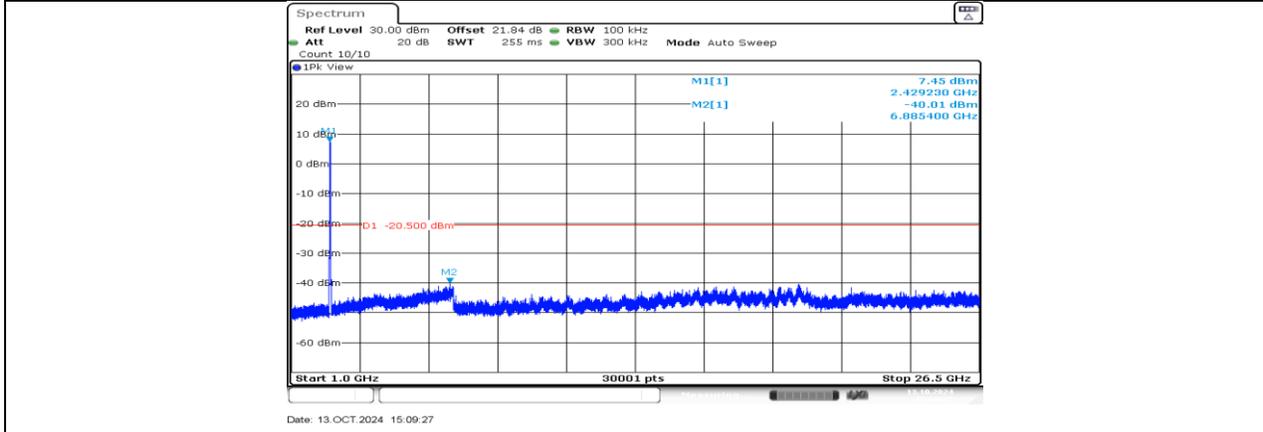
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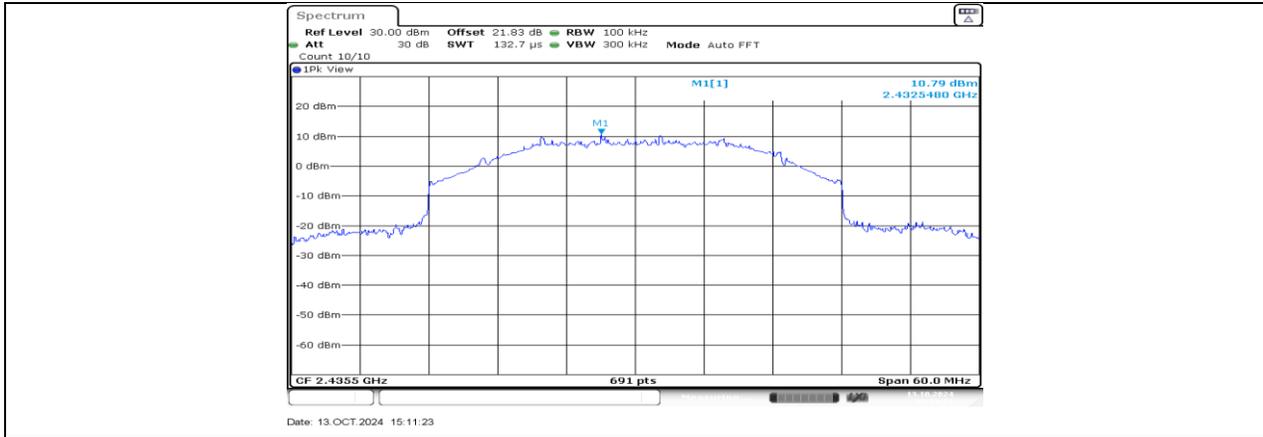
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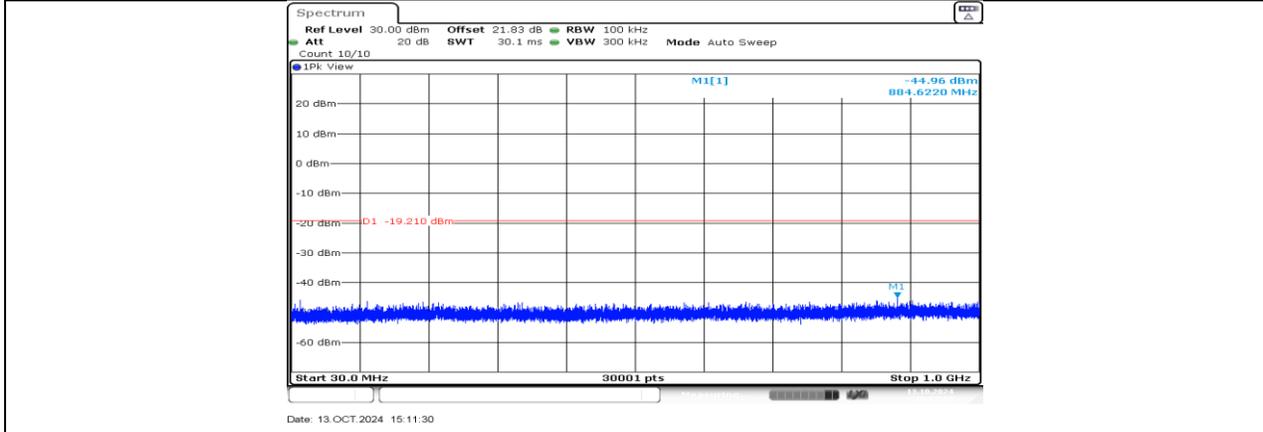
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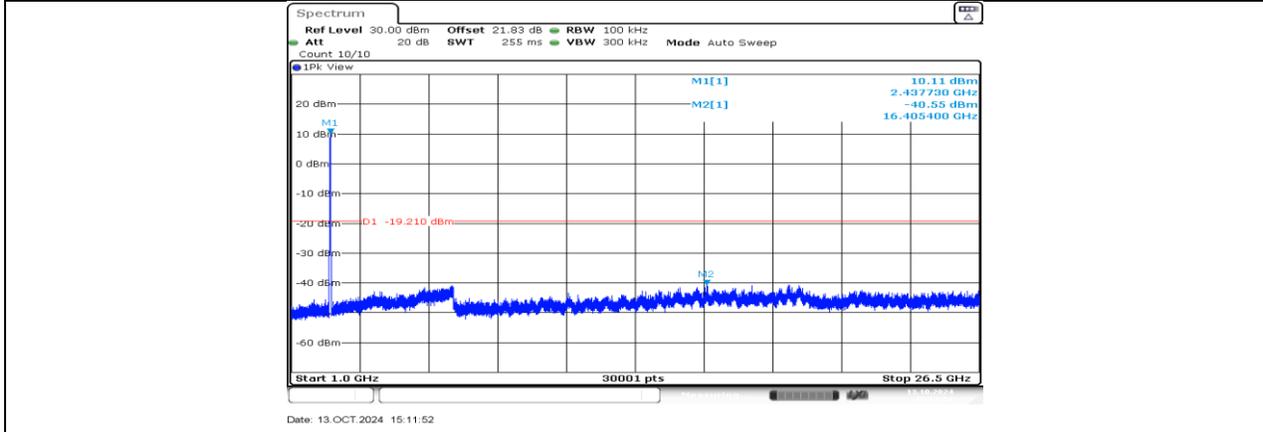
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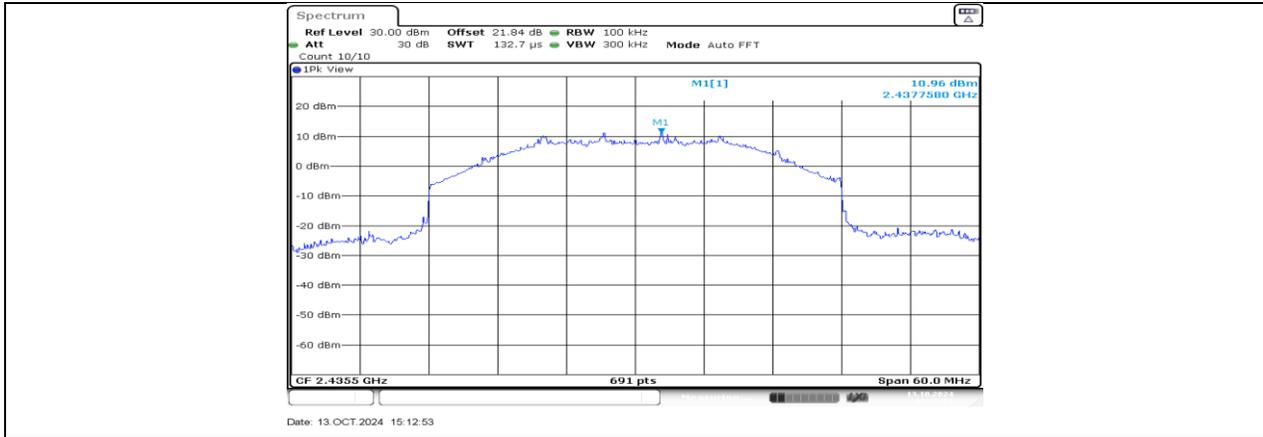
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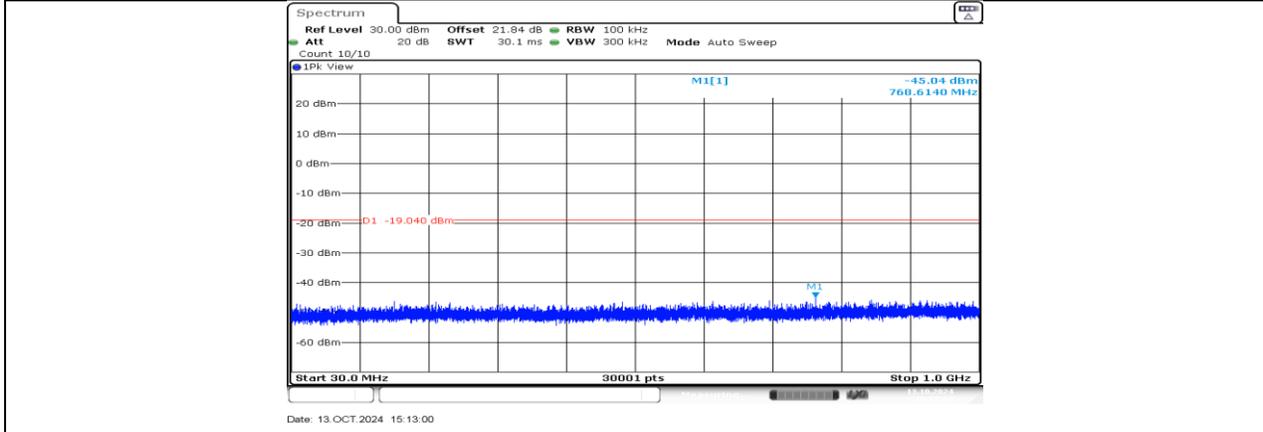
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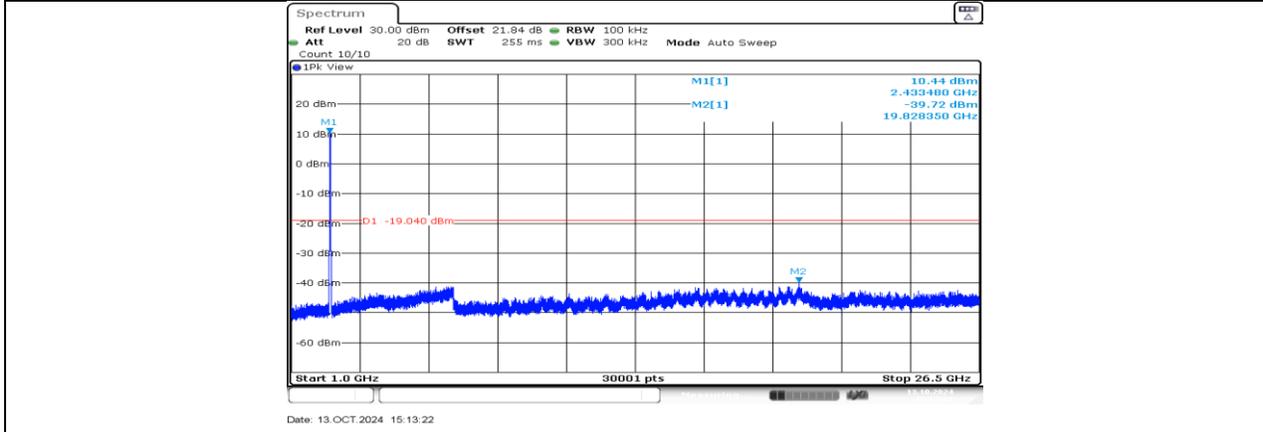
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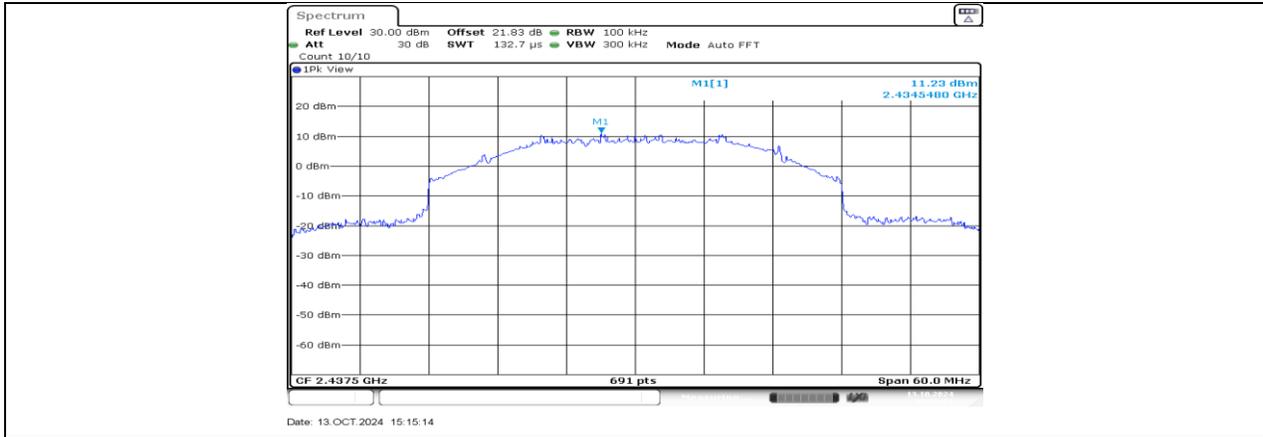
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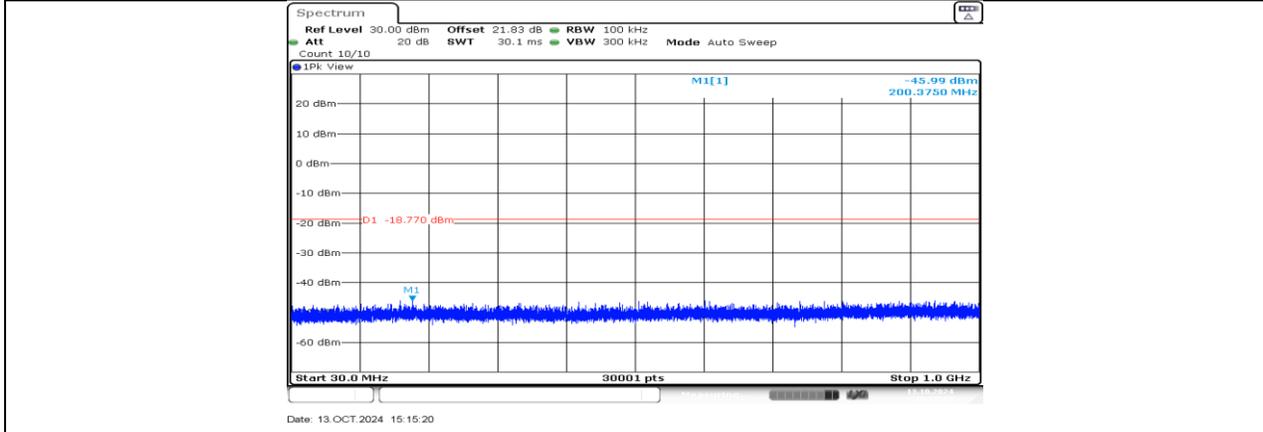
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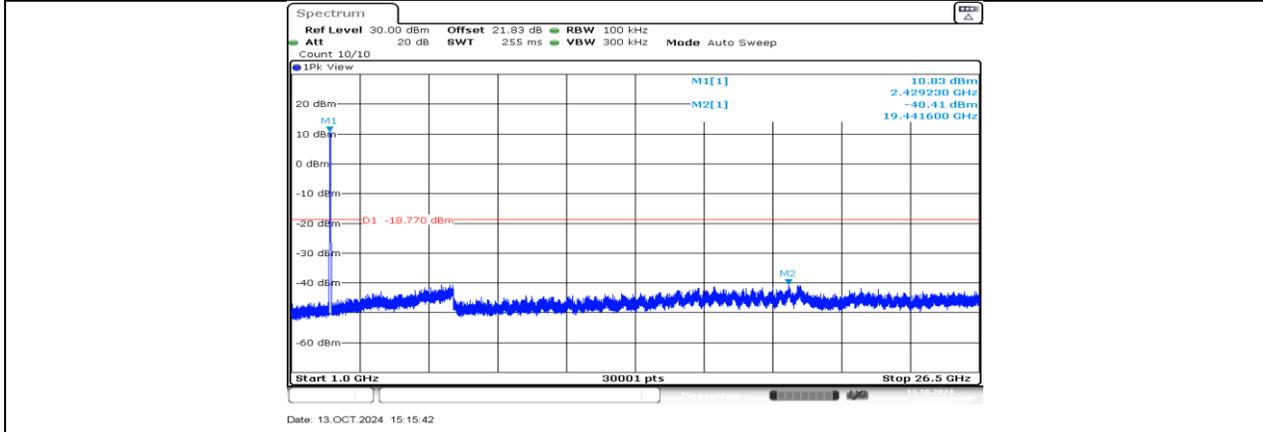
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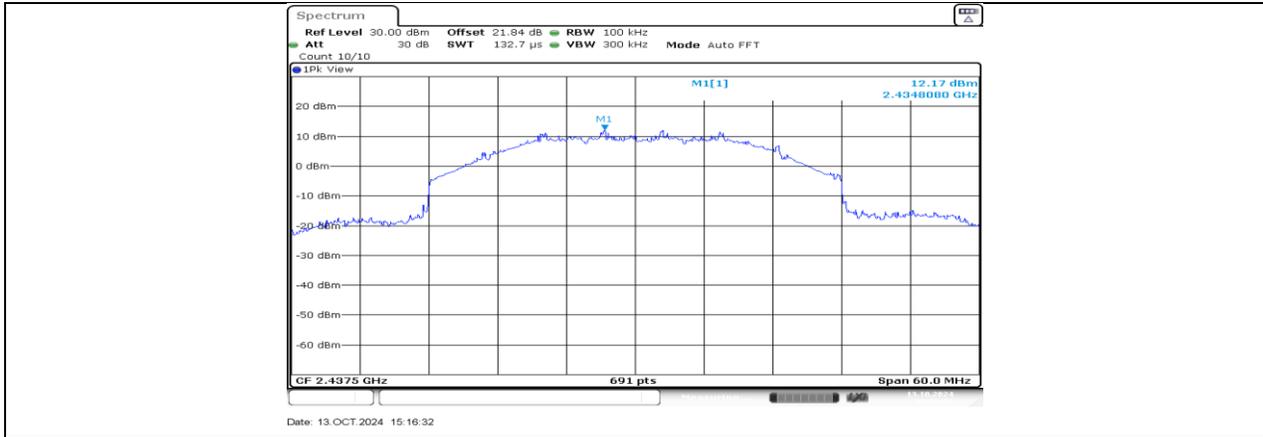
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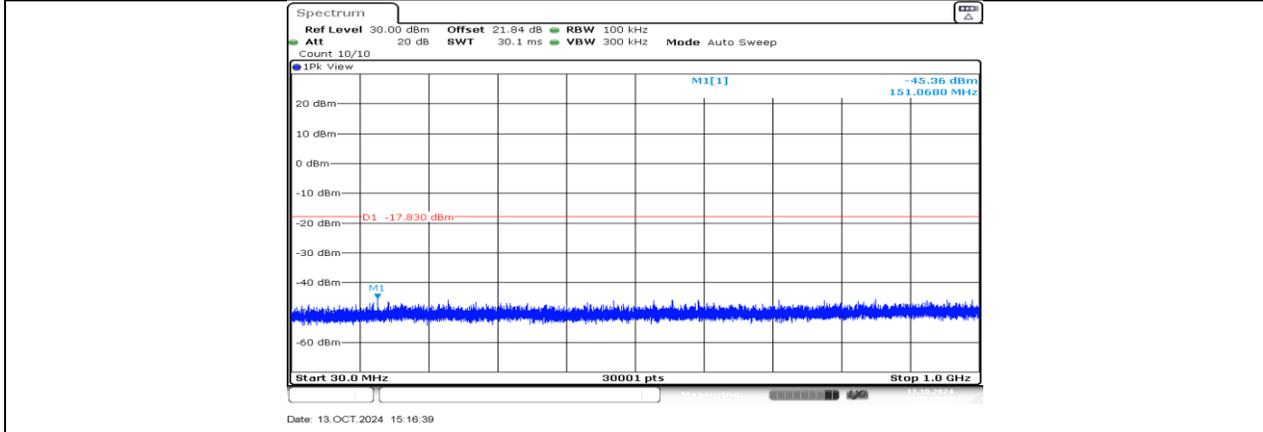
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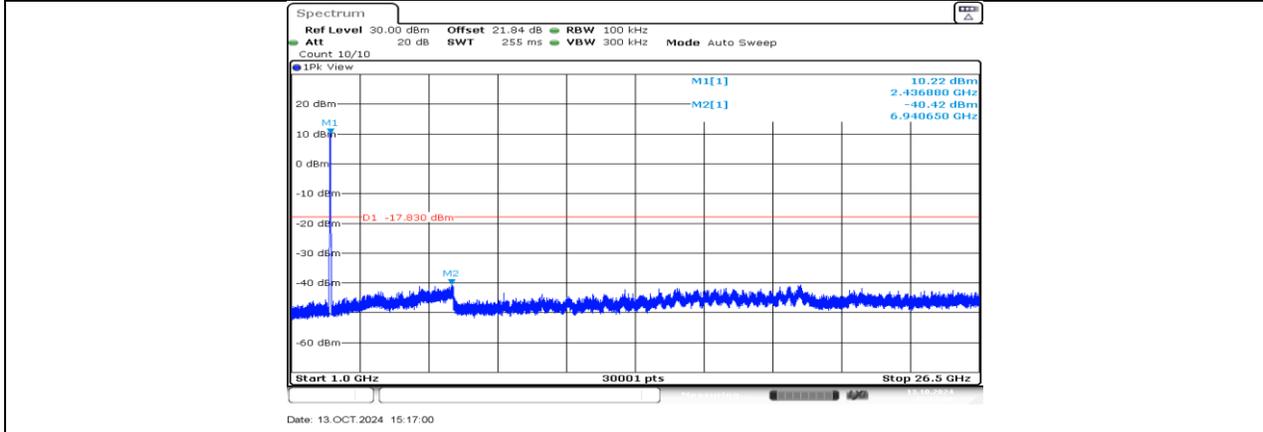
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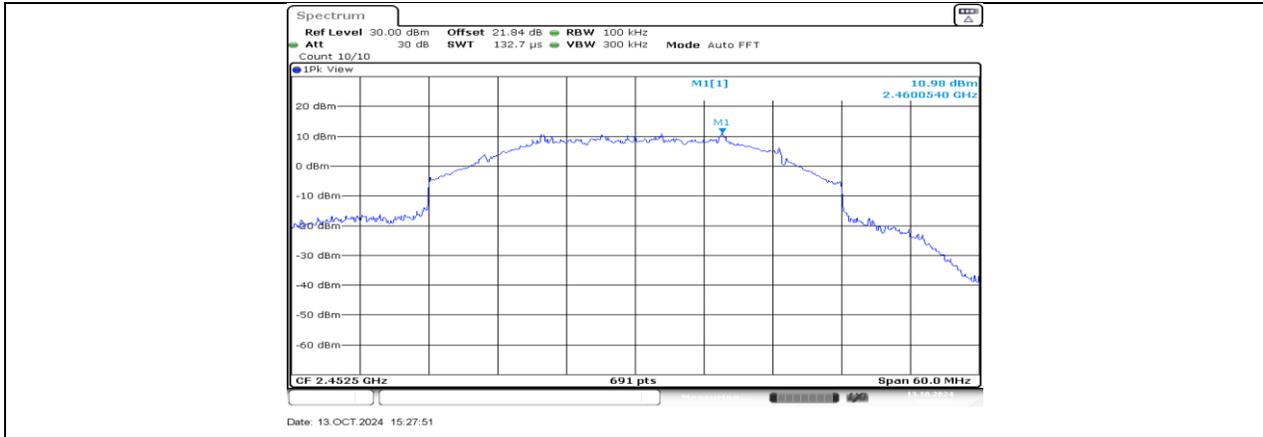
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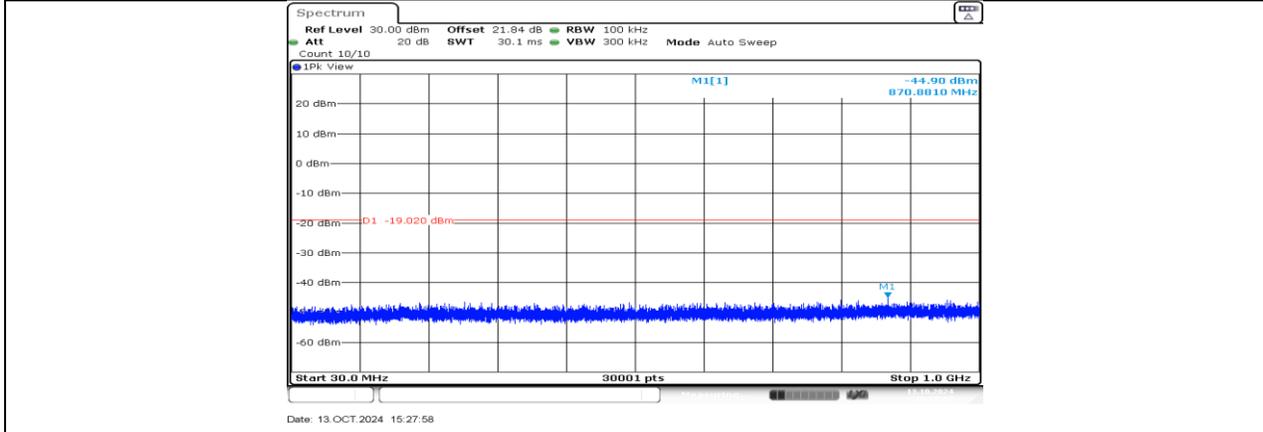
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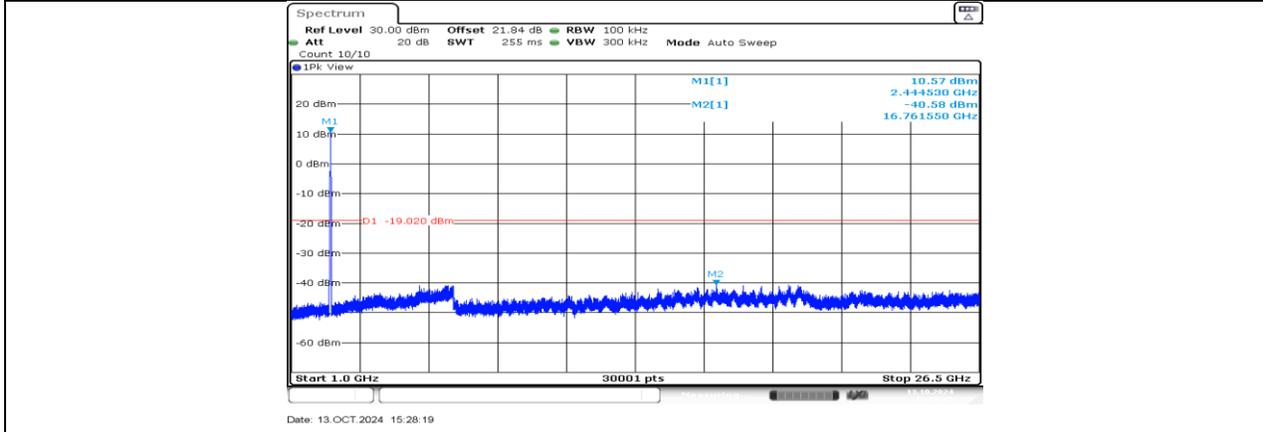
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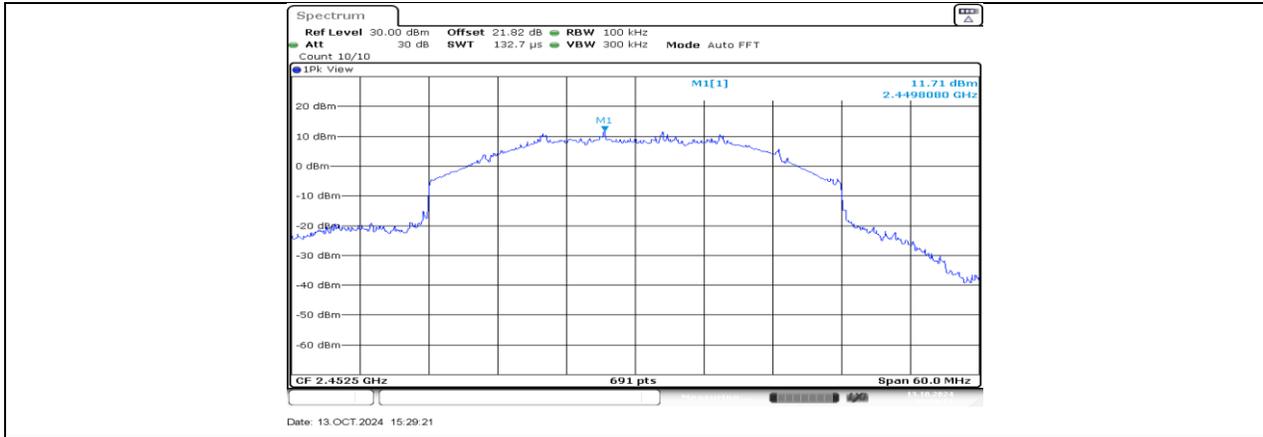
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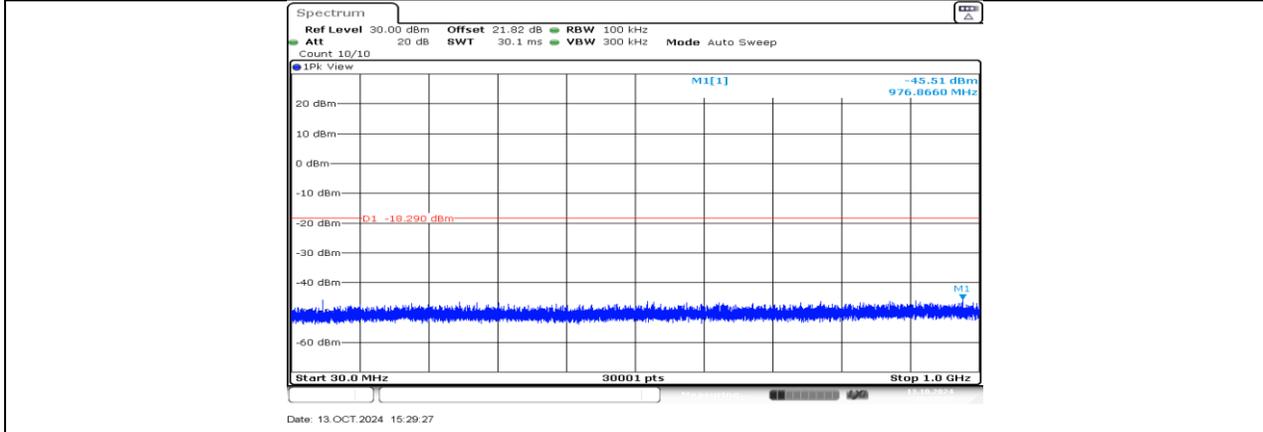
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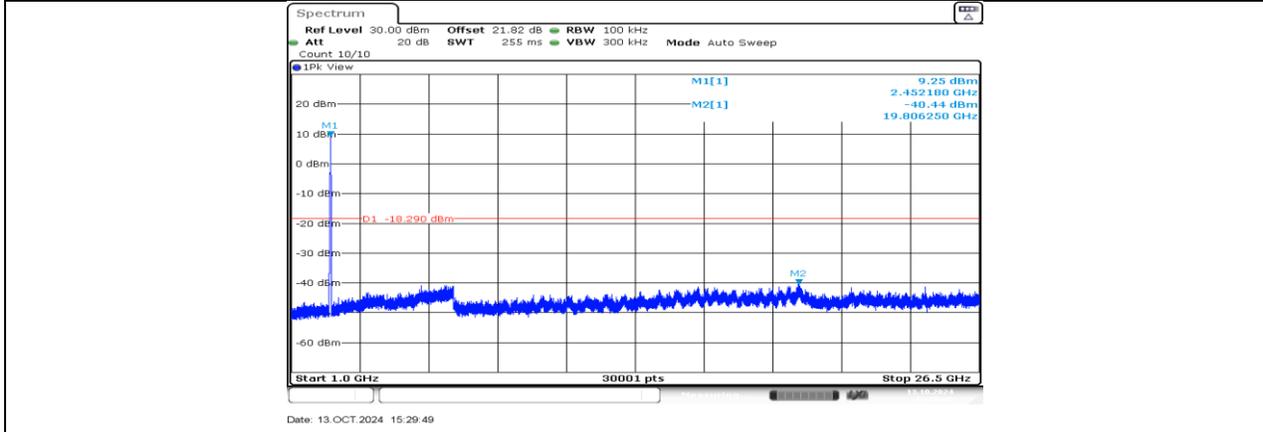
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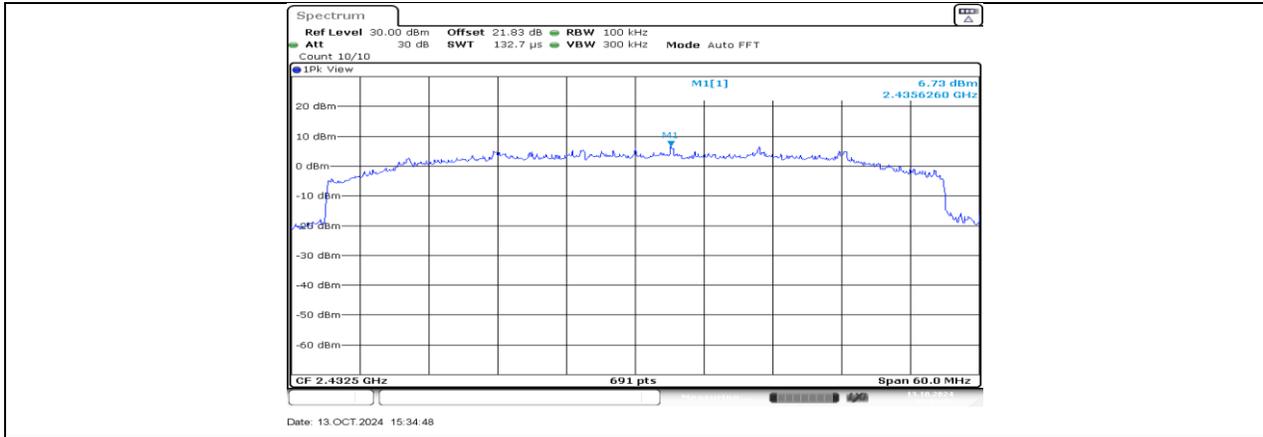
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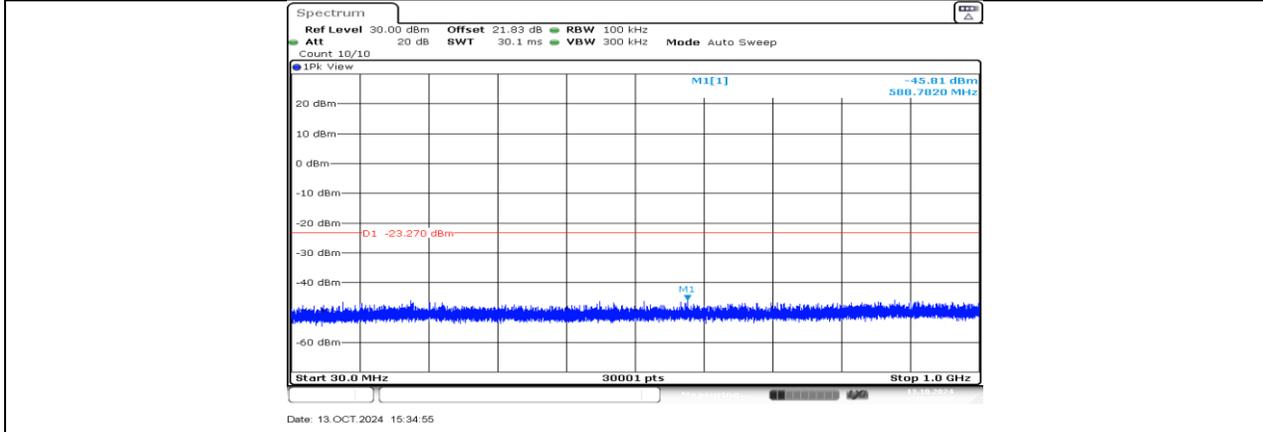
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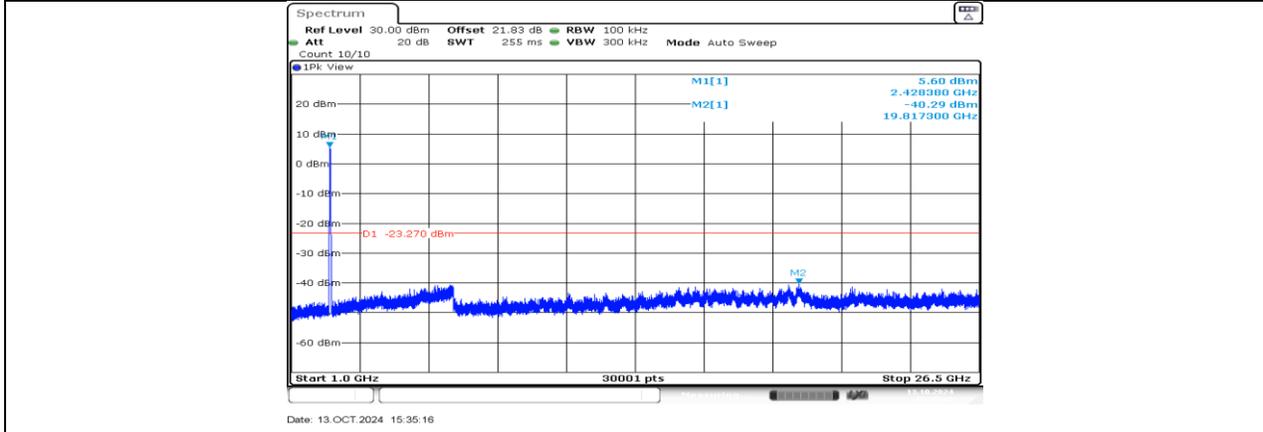
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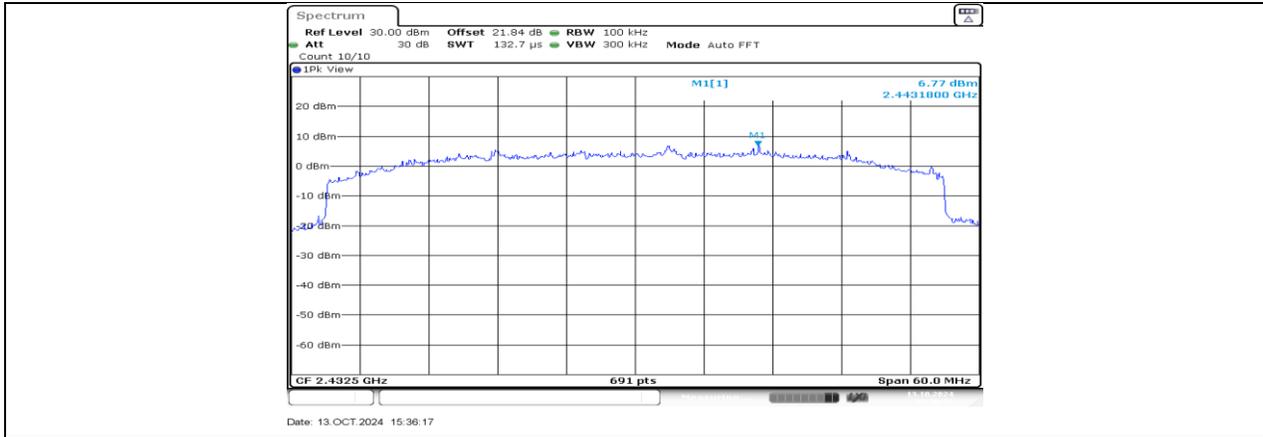
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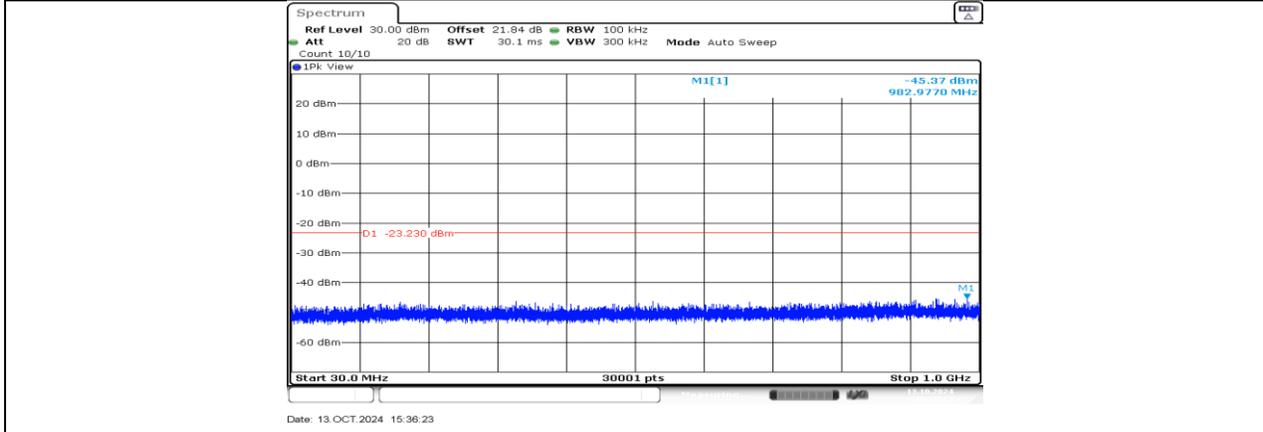
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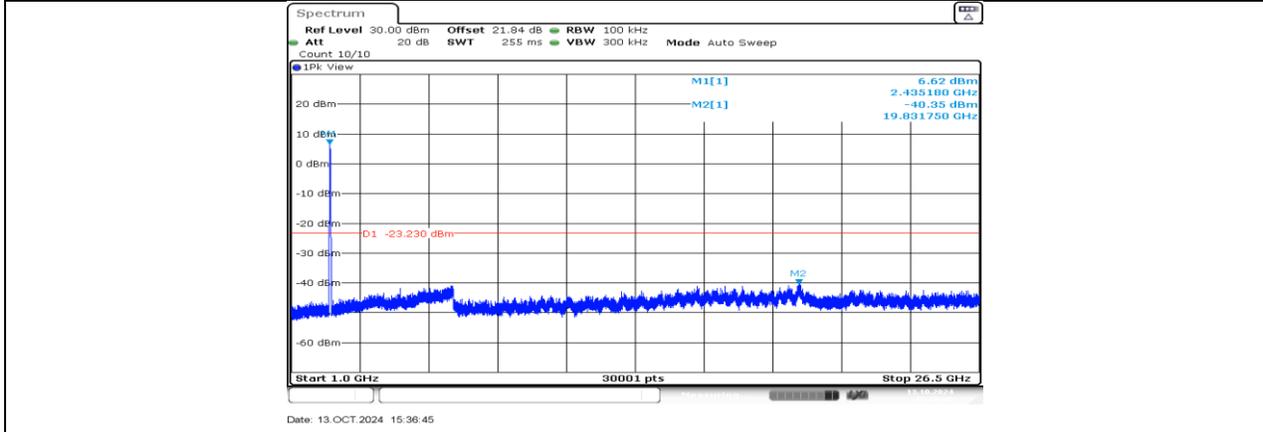
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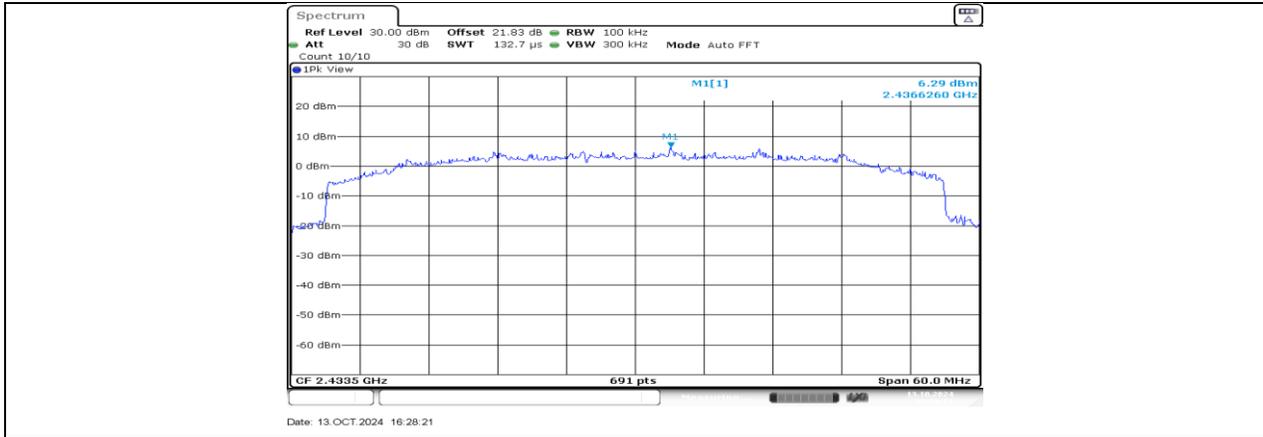
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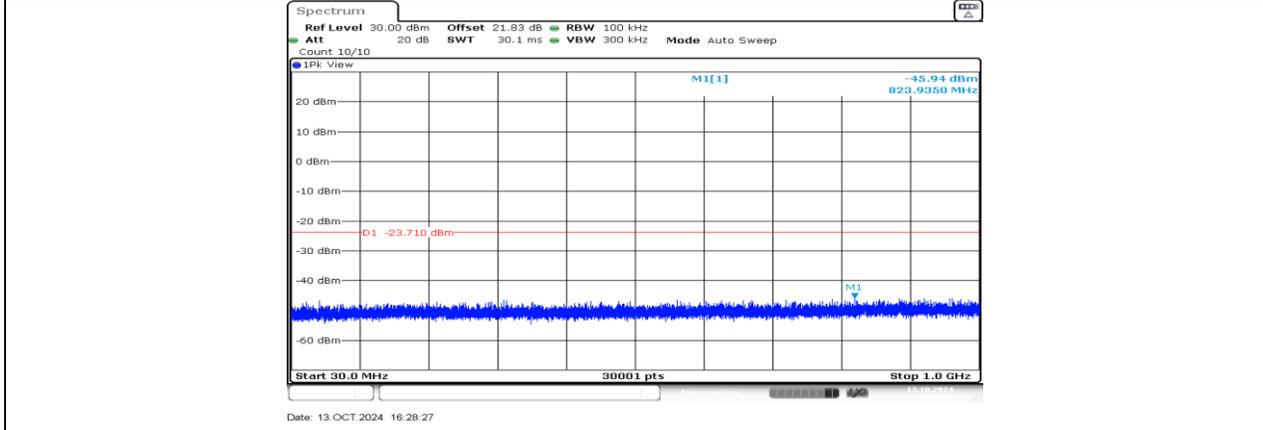
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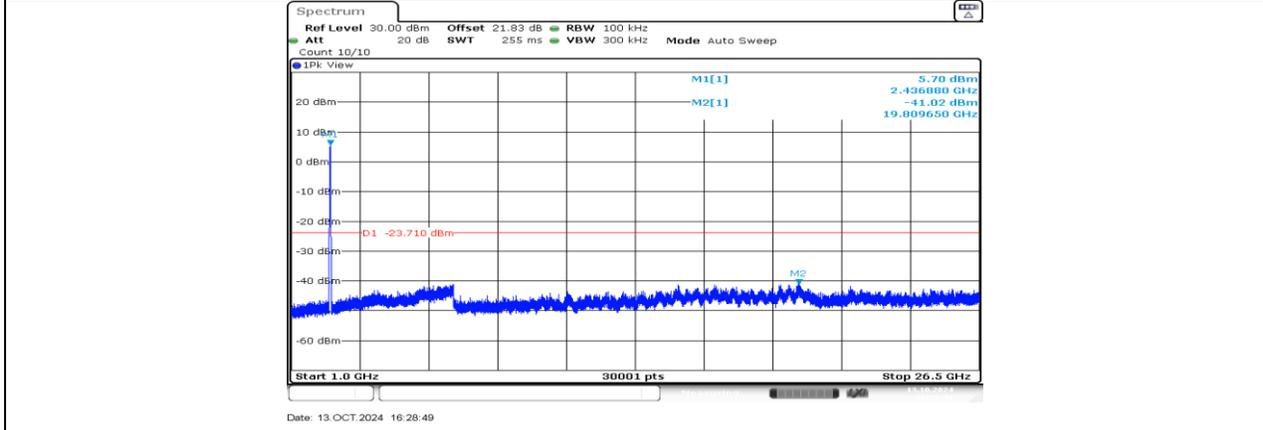
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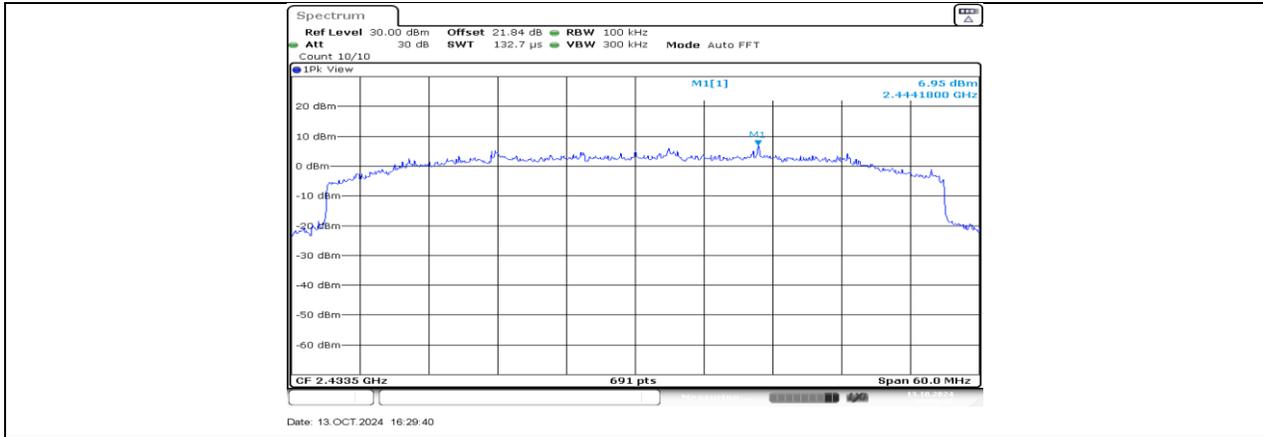
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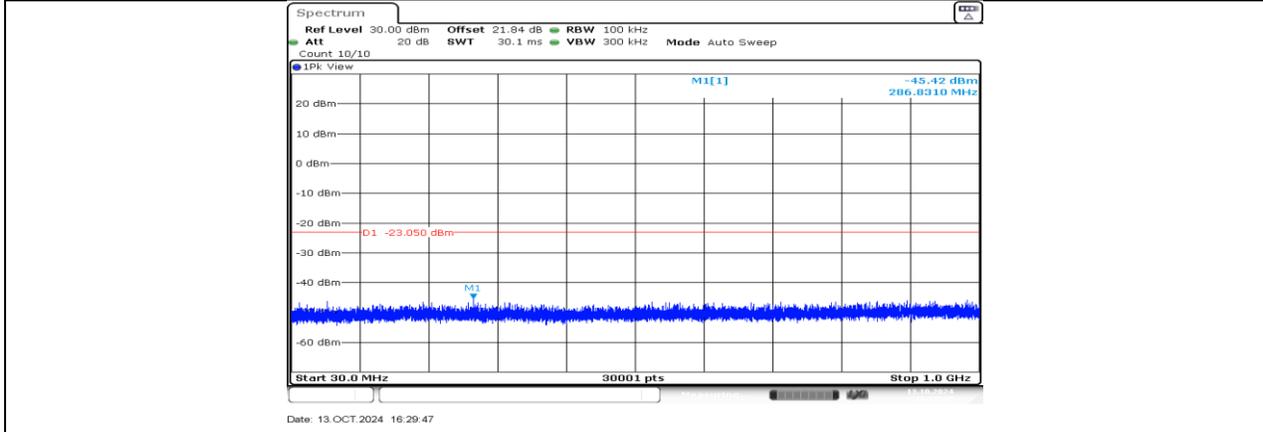
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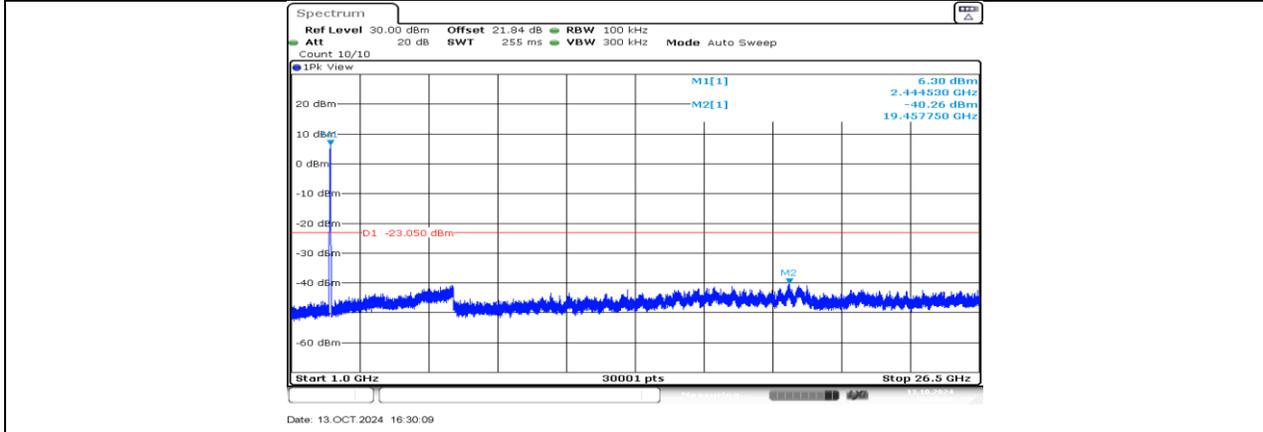
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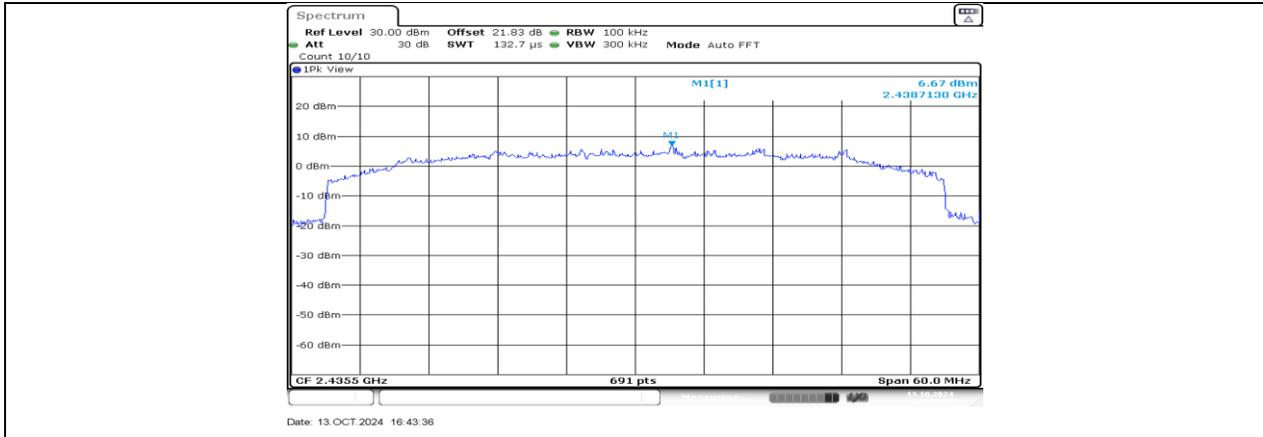
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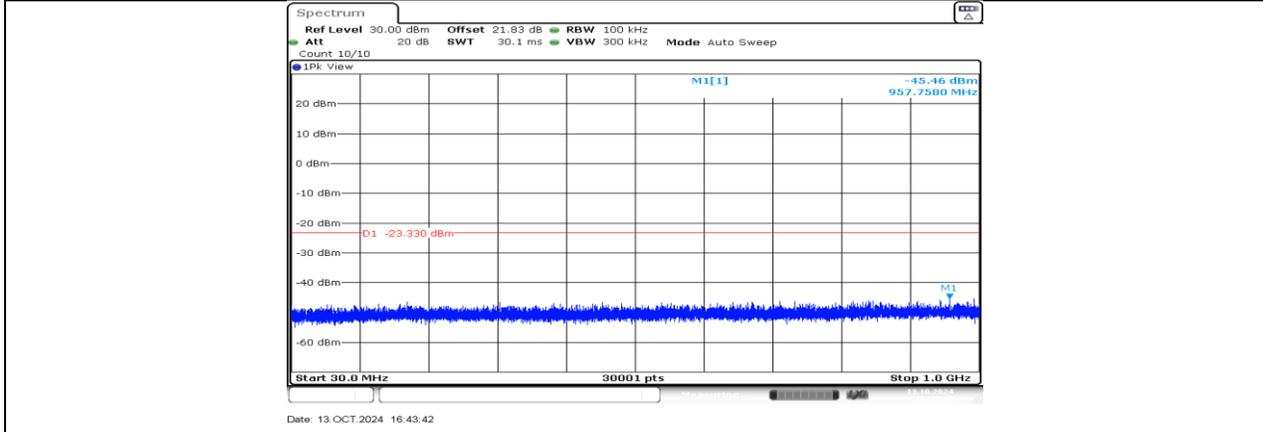
**SRD 60M\_Ant1\_2433.5\_30~1000**



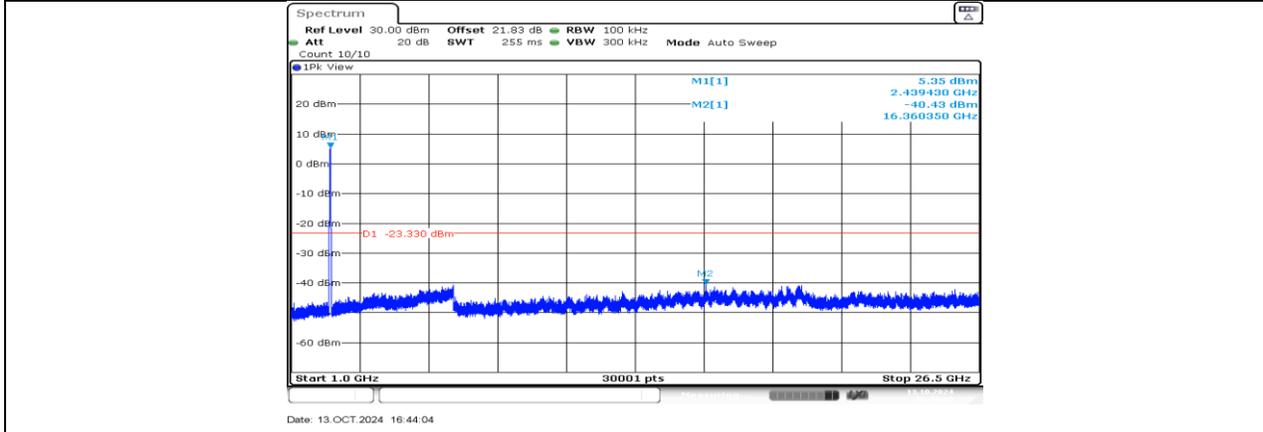
**SRD 60M\_Ant1\_2433.5\_1000~26500**



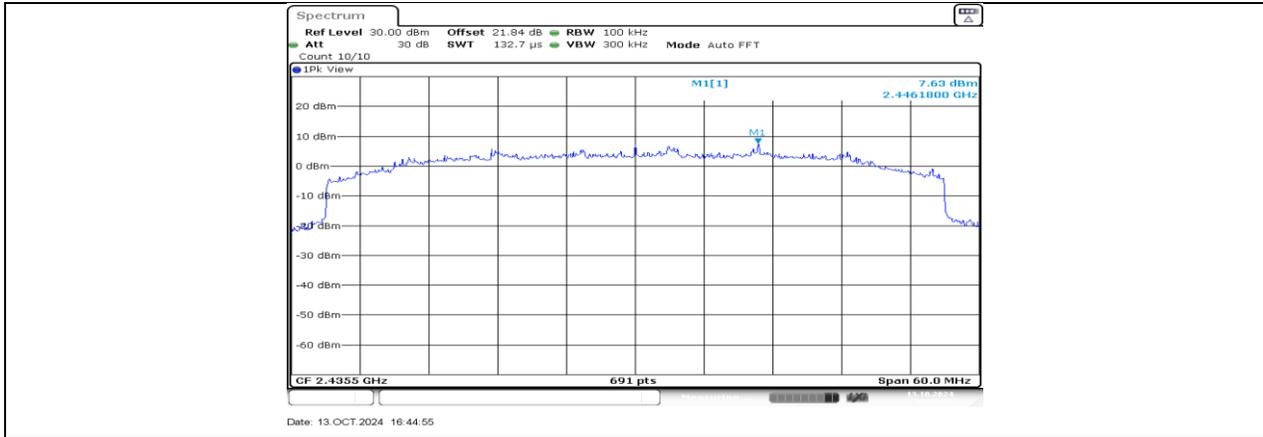
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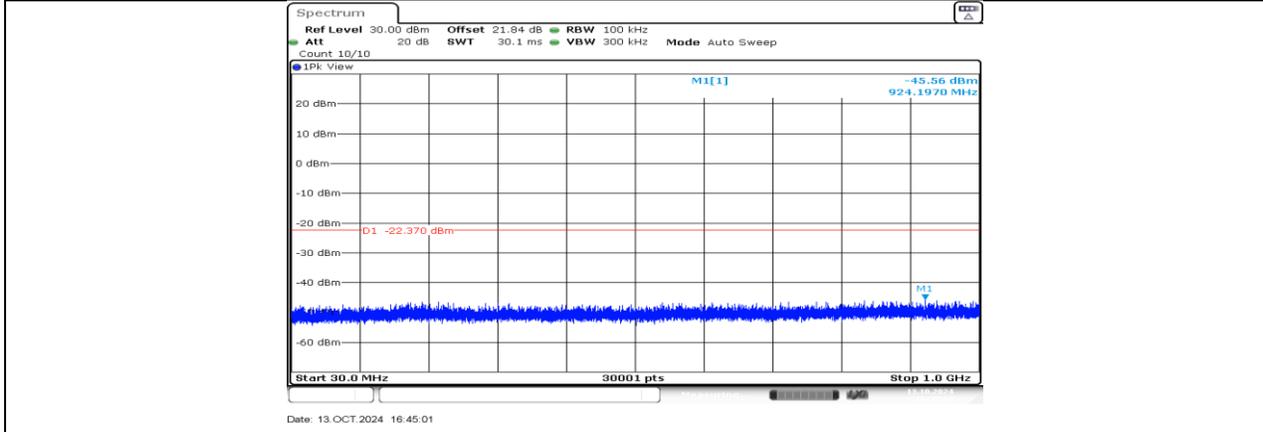
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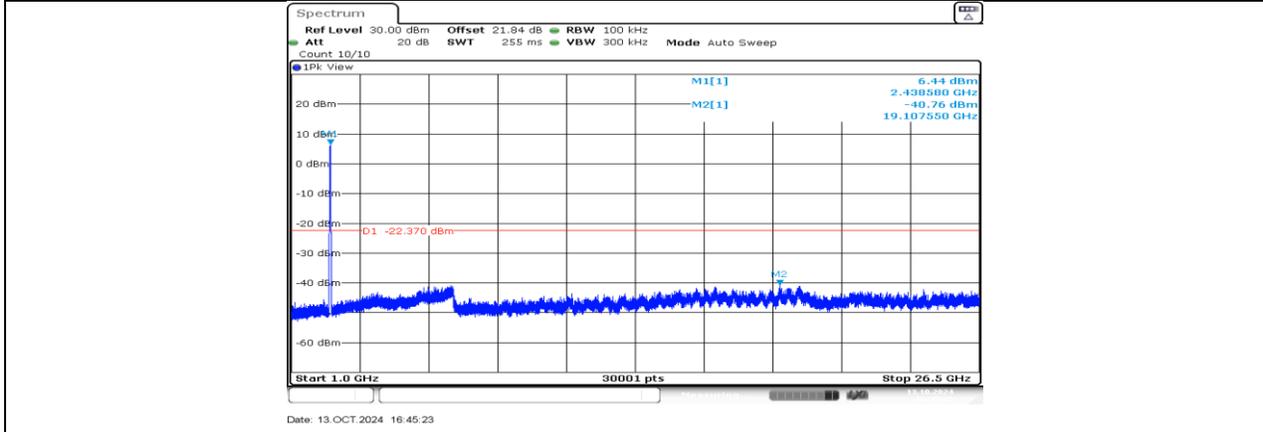
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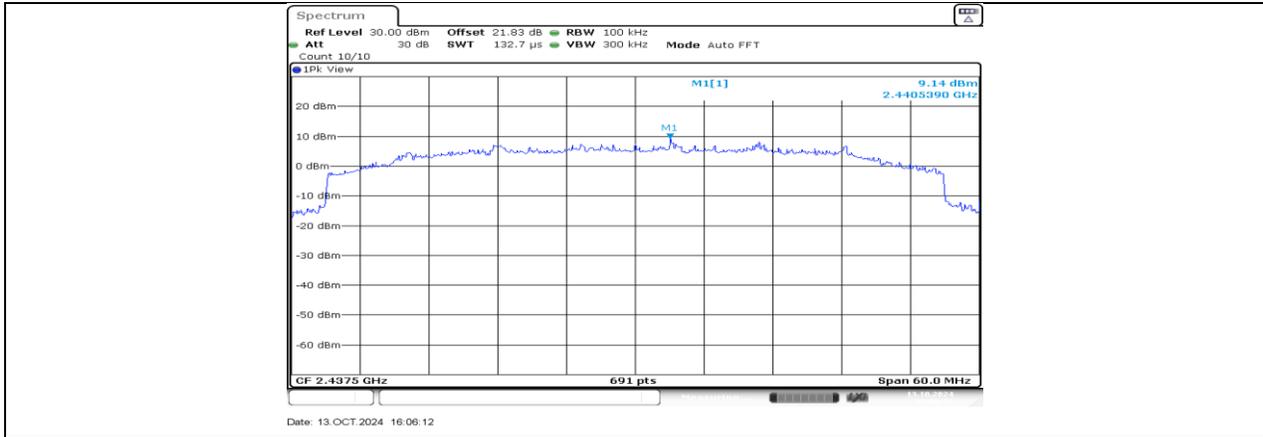
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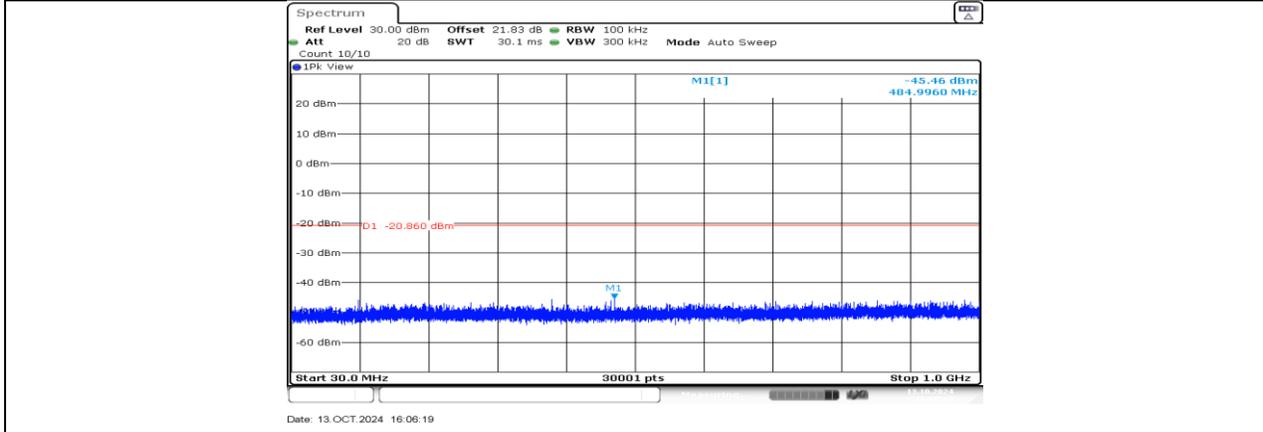
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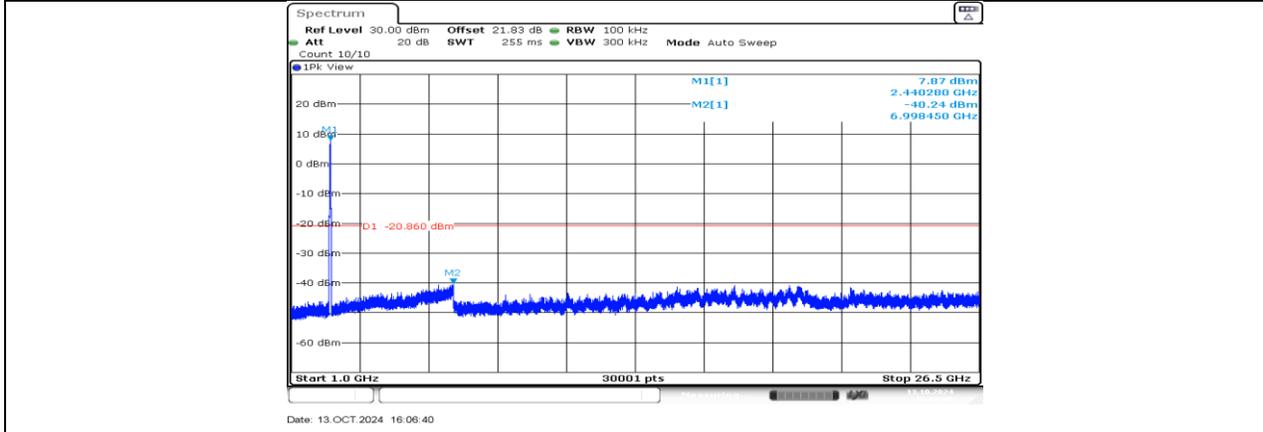
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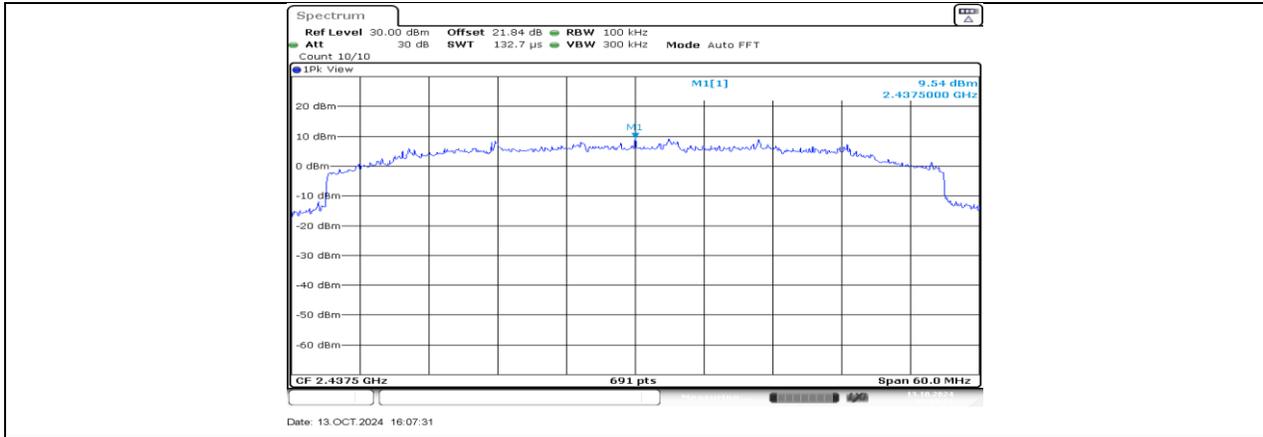
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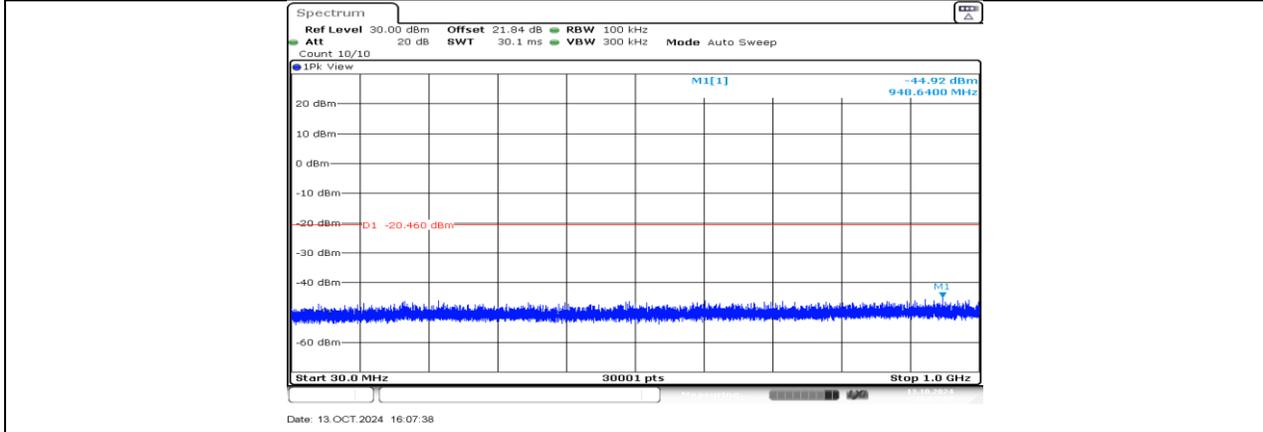
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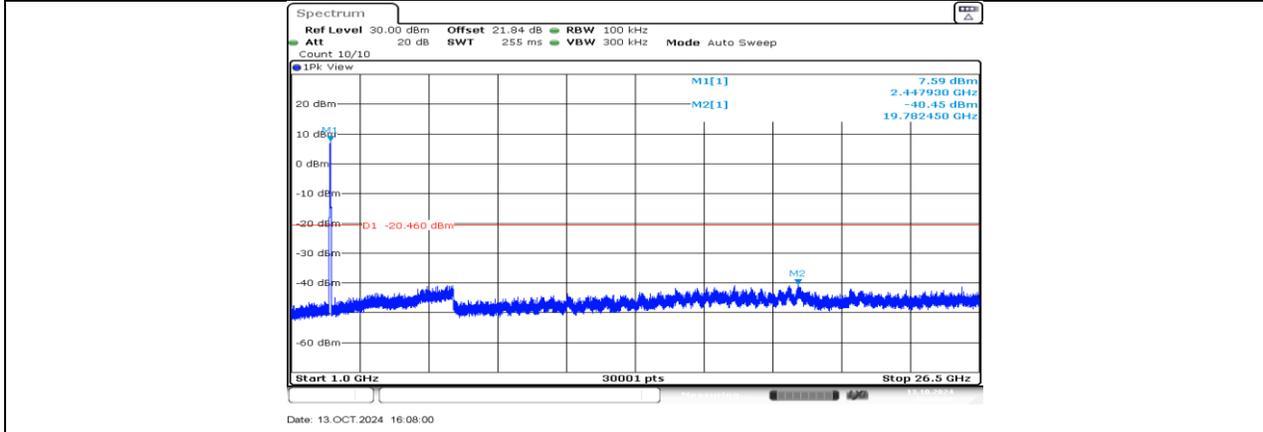
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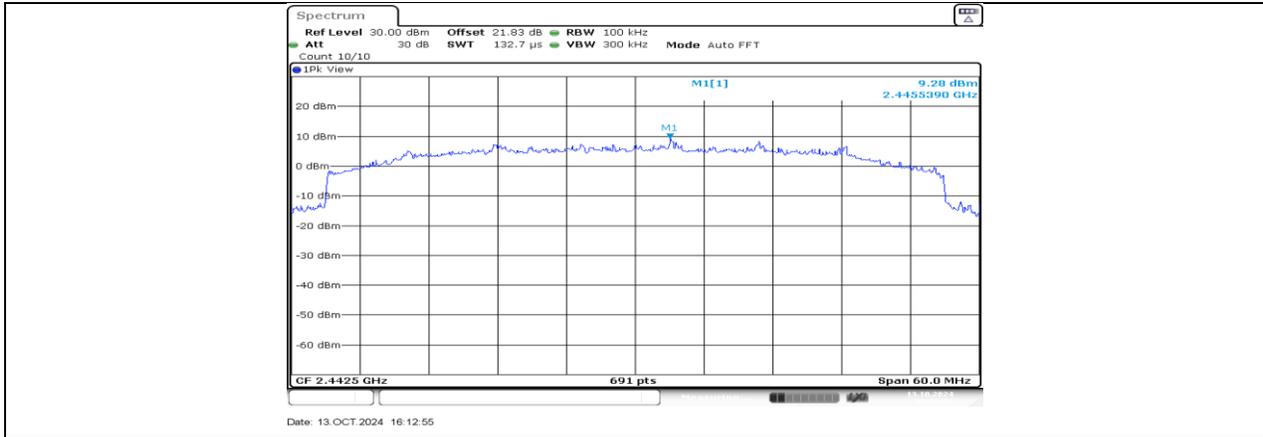
SRD 60M\_Ant1\_2437.5\_0~Reference



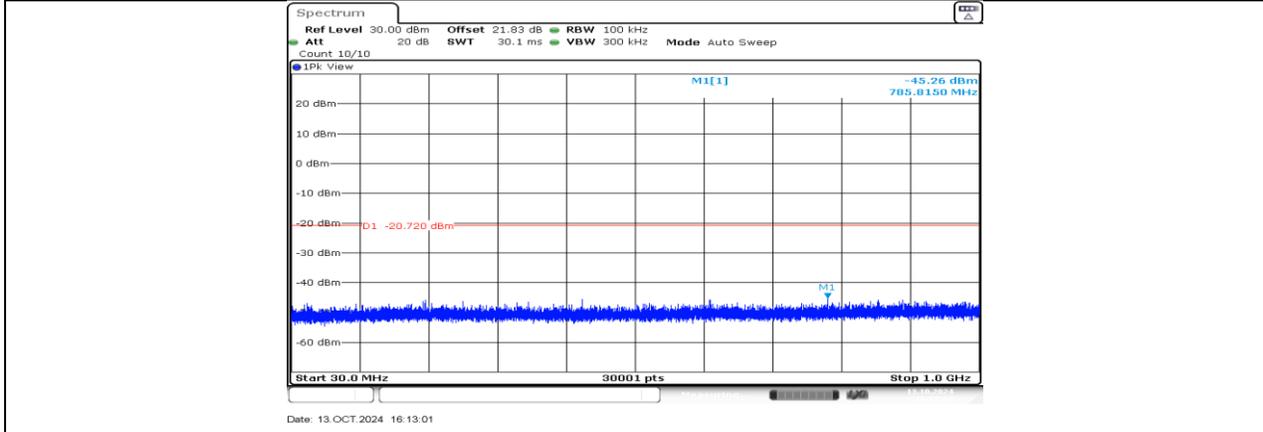
SRD 60M\_Ant1\_2437.5\_30~1000



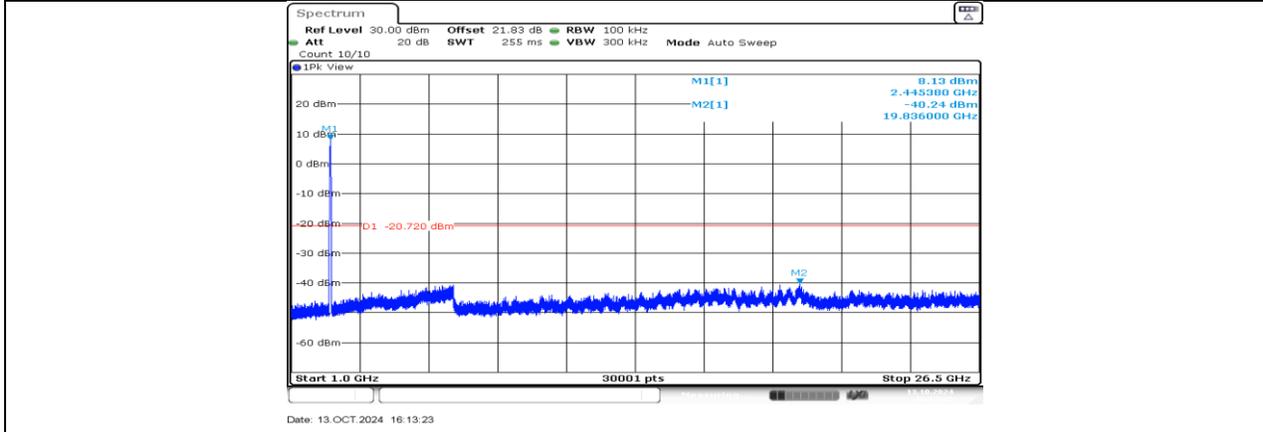
SRD 60M\_Ant1\_2437.5\_1000~26500



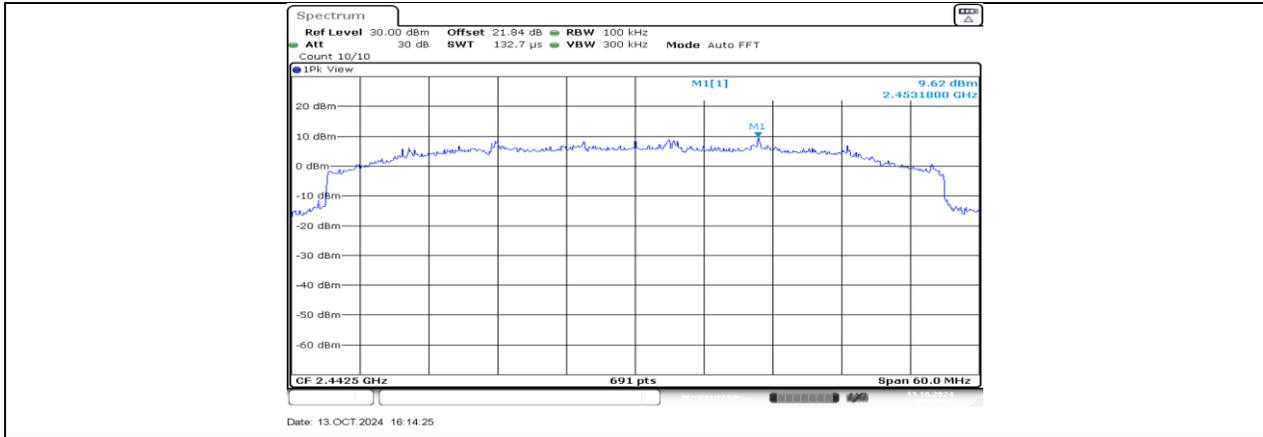
**SRD 60M\_Ant0\_2442.5\_0~Reference**



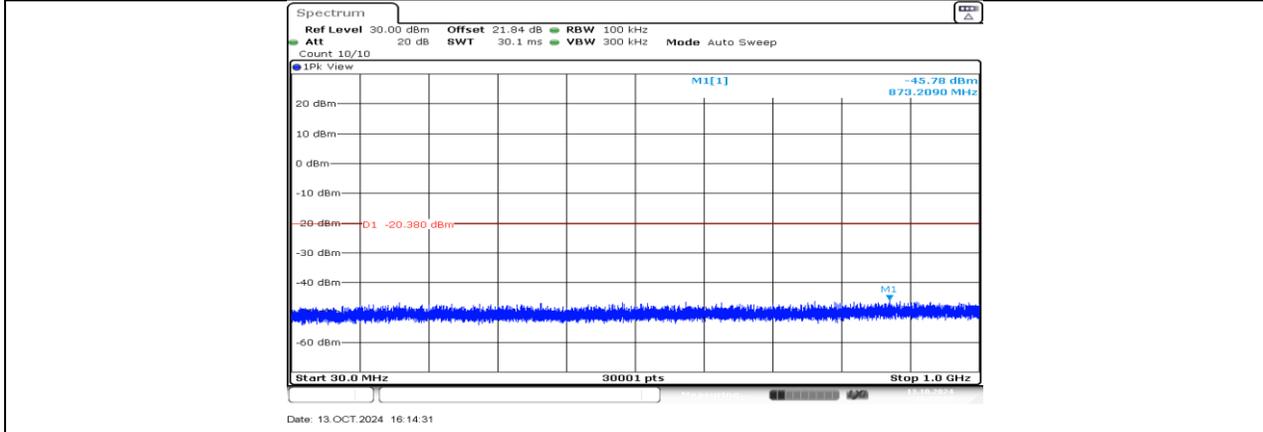
**SRD 60M\_Ant0\_2442.5\_30~1000**



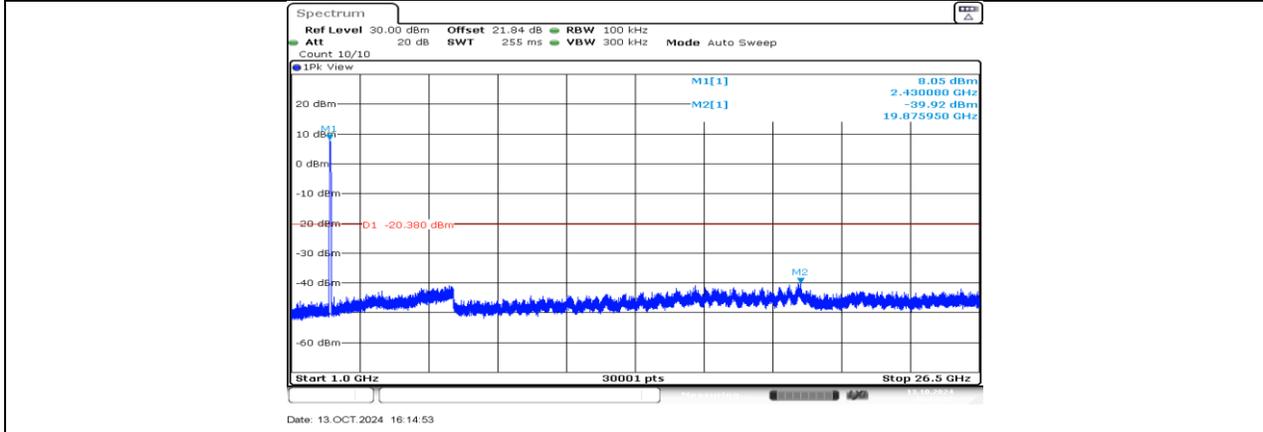
**SRD 60M\_Ant0\_2442.5\_1000~26500**



**SRD 60M\_Ant1\_2442.5\_0~Reference**



**SRD 60M\_Ant1\_2442.5\_30~1000**



**SRD 60M\_Ant1\_2442.5\_1000~26500**

## 11.7. APPENDIX G: DUTY CYCLE

### 11.7.1. Test Result

Test Mode	On Time (msec)	Period (msec)	Duty Cycle x (Linear)	Duty Cycle (%)	Duty Cycle Correction Factor (dB)	1/T Minimum VBW (kHz)	Final setting For VBW (kHz)
SRD 10M	105.00	105.00	1.0000	100.00	0.00	0.01	N/A
SRD 20M	105.00	105.00	1.0000	100.00	0.00	0.01	N/A
SRD 40M	105.00	105.00	1.0000	100.00	0.00	0.01	N/A
SRD 60M	105.00	105.00	1.0000	100.00	0.00	0.01	N/A

Note:

Duty Cycle Correction Factor=10log (1/x).

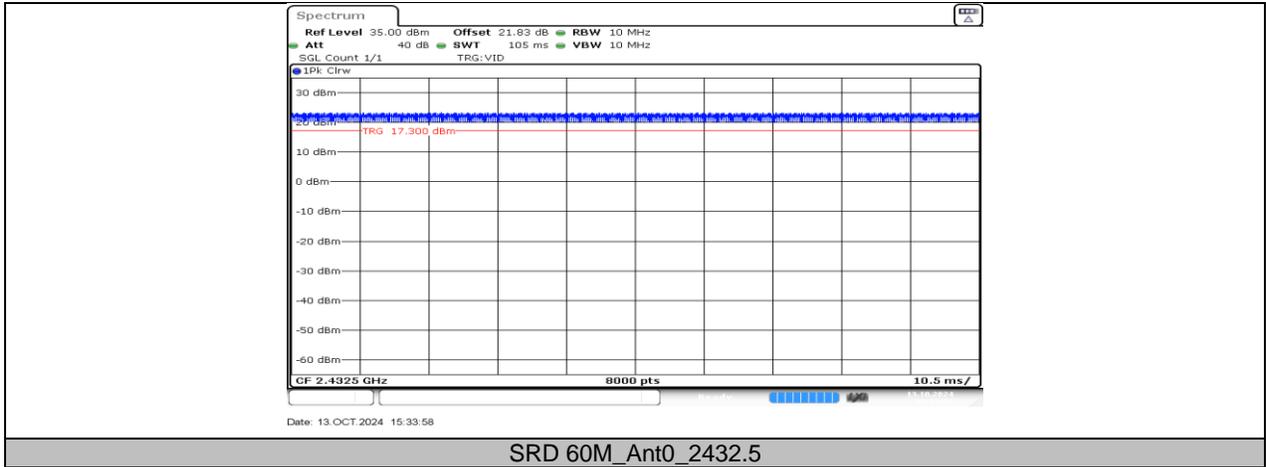
Where: x is Duty Cycle (Linear)

Where: T is On Time

If that calculated VBW is not available on the analyzer then the next higher value should be used.

### 11.7.2. Test Graphs





SRD 60M\_Ant0\_2432.5

**END OF REPORT**