5. System Connector Interface

5.1 Overview

Electrical connections to the radio device (except the antenna), are made through the System Connector Interface. The system connector is a 60-pin, standard 0.05 in (1.27 mm) pitch device.

The system connector allows both board-to-board and board-to-cable connections to be made. Use a board-board connector to connect the radio device directly to a PCB, and a board-cable connector to connect the radio device via a cable.

Figure 5.1 below shows the numbering of the connector pins.

A ground connection is provided at the mounting hole next to the RF connector on the radio device as shown below. Connect this ground point to the DGND pins of the radio device by the shortest, low-impedance path possible. The purpose of this connection is to allow any antenna ESD strikes to bypass the radio device's internal ground path.

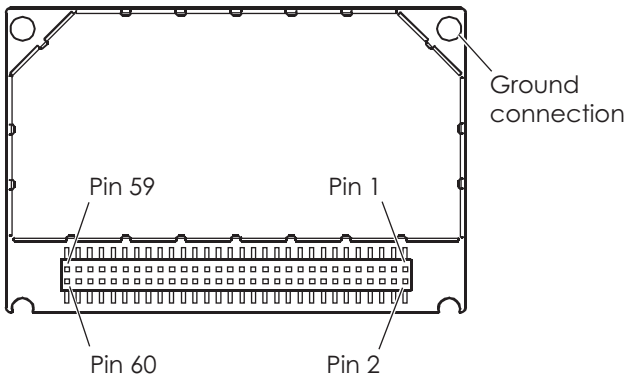

Figure 5.1 Radio Device, viewed from underneath

The following table gives the pin assignments for the system connector interface and a short description for each signal.

Note! Under the heading "Dir" in the table, radio device input and output signals are indicated by the letters I and O respectively.

Pin	*Signal Name*	*Dir*	*Signal Type*	*Description*
1	VCC	-	Supply	Power supply
2	DGND	-	-	Digital ground
3	VCC	-	Supply	Power supply
4	DGND	-	-	Digital ground
5	VCC	-	Supply	Power supply
6	DGND	-	-	Digital ground
7	VCC	-	Supply	Power supply
8	DGND	-	-	Digital ground
9	VCC	-	Supply	Power supply
10	DGND	-	-	Digital ground
11	CHG_IN	-	Battery charge power	Battery charging
12	DGND	-	-	Digital ground
13	IO5 ADC4	I/0 I	Digital 2.75V Analogue	General purpose input/output 5 Analogue to digital converter 4
14	ON/OFF	I	Internal pull up, open drain	Turns the radio device on and off.
15	SIMVCC	-	Digital 3V/5V	SIM card power supply. Power output from radio device for SIM Card
16	SIMPRESENCE	I	Internal pull up, open drain	SIM Presence A "1" indicates that the SIM is missing; a "0" that it is inserted
17	SIMRST	O	Digital 3V/5V	SIM card reset
18	SIMDATA	I/O	Digital 3V/5V	SIM card data
19	SIMCLK	O	Digital 3V/5V	SIM card clock
20	DAC	O	Analogue	Digital to analogue converter
21	IO1 KEYROW2	I/O I	Digital 2.75V	General purpose input/output 1 Keyboard row 2
22	IO2 ADC5	I/O I	Digital 2.75V Analogue	General purpose input/output 2 Analogue to digital converter 5
23	IO3 KEYROW3	I/O I	Digital 2.75V	General purpose input/output 3 Keyboard row 3
24	IO4 KEYROW4	I/O I	Digital 2.75V	General purpose input/output 4 Keyboard row 4
25	VRTC	I	Supply 1.8V	Supply for real time clock
26	ADC1	I	Analogue	Analogue to digital converter 1
27	ADC2	I	Analogue	Analogue to digital converter 2

Pin	*Signal Name*	*Dir*	*Signal Type*	*Description*
28	ADC3	I	Analogue	Analogue to digital converter 3
29	SDA	I/O	2.75V, internal pull up	I^2C data
30	SCL	O	2.75V, internal pull up	I^2C clock
31	BUZZER	O	Digital 2.75V	Buzzer output from radio device
32	OUT3 KEYCOL3 DSR	O O O	Digital 2.75V	General purpose output 3 Keyboard column 3 Data set ready (UART1)
33	LED IO6	O I/O	Digital 2.75V	Flashing LED General purpose I/O 6
34	VIO	O	Power Out 2.75V	Radio device power indication. VIO is a 2.75V at 75mA output supply that can be used to power external circuitry that interfaces to the radio device
35	TX_ON	O	Digital 2.75V	This output indicates when the GSM radio device is going to transmit the burst
36	RI KEYCOL2 O2	O O O	Digital 2.75V	Ring Indicator (UART1) Keyboard column 2 General purpose output 2
37	DTR KEYROW1 IN1	I I I	Digital 2.75V	Data Terminal Ready (UART1) Keyboard row 1 General purpose input 1
38	DCD KEYCOL1 O1	O O O	Digital 2.75V	Data Carrier Detect (UART1) Keyboard column 1 General purpose output 1
39	RTS IO9	I I/O	Digital 2.75V	Request To Send (UART1) General purpose I/O 9
40	CTS KEYCOL4 O4	O O O	Digital 2.75V	Clear To Send (UART1) Keyboard column 4 General purpose output 4
41	TD	I	Digital 2.75V	Transmitted Data (UART1). Data from DTE (host) to DCE (radio device).
42	RD	O	Digital 2.75V	Received Data (UART1). Data from DCE (radio device) to DTE (host).
43	TD3 I/O7	I I/O	Digital 2.75V	Transmitted data (UART3) General purpose I/O 7
44	RD3 I/O8	O I/O	Digital 2.75V	Received data (UART3) General purpose I/O 8
45	TD2	I	Digital 2.75V	Transmitted data (UART2). Used for flashing the memory.
46	RD2	O	Digital 2.75V	Received data (UART2). Used for flashing the memory.
47	PCMULD	I	Digital 2.75V	DSP PCM digital audio input
48	PCMDLD	O	Digital 2.75V	DSP PCM digital audio output

Pin	*Signal Name*	*Dir*	*Signal Type*	*Description*
49	PCMO	O	Digital 2.75V	Codec PCM digital audio output
50	PCMI	I	Digital 2.75V	Codec PCM digital audio input
51	PCMSYNC	O	Digital 2.75V	DSP PCM frame sync
52	PCMCLK	O	Digital 2.75V	DSP PCM clock output
53	MICP	I	Analogue	Microphone Input positive
54	MICN	I	Analogue	Microphone Input negative
55	BEARP	O	Analogue	Speaker output positive
56	BEARN	O	Analogue	Speaker output negative
57	AFMS	O	Analogue	Audio output from radio device
58	SERVICE	I	2.7V	Flash programming voltage for the MS. Enable logger information if not flashing.
59	ATMS	I	Analogue	Audio input to radio device
60	AGND	-	Analogue	Analogue ground

5.2 General Electrical and Logical Characteristics

Many of the signals, as indicated in the table above, are high-speed CMOS logic inputs or outputs powered from a 2.75 V ± 5 % internal voltage regulator, and are defined as Digital 2.75 V. Whenever a signal is defined as Digital 2.75 V, the following electrical characteristics apply.

Parameter	*Min.*	*Max.*	*Units*
High Level Output Voltage (V_{OH}), I_O = –2mA	2.2	2.75	V
Low Level Output Voltage (V_{OL}), I_O = 2mA	0	0.6	V
High Level Input Voltage (V_{IH})	1.93	2.75	V
Low Level Input voltage (V_{IL})	0	0.5	V

Note! Unused pins can be left floating.

5.2.1 General Protection Requirements

- All 2.75 V digital inputs will continuously withstand and suffer no damage in the power-on or power-off condition when subjected to any voltage from -0.5 V to 3.47 V (3.3 V + 5 %).
- All 2.75 V digital outputs will continuously withstand a short circuit to any other voltage within the range 0 V to 3 V.
- All analogue outputs will continuously withstand a short circuit to any voltage within the range 0 V to 3 V.

- The SIM output signals and the SIMVCC supply will continuously withstand a short circuit to any voltage within the range 0V to 4.1V.

5.3 Grounds

Pin	*Signal*	*Description*
2, 4, 6, 8, 10, 12	DGND	Digital ground
60	AGND	Analogue ground

There are two ground connections in the radio device, AGND (analogue ground) and DGND (digital ground). Pin assignments are shown in the table above.

Note! AGND and DGND are connected at a single point inside the radio device. They must *not* be joined together in your application.

5.3.1 Analogue Ground - AGND

AGND is the return signal, or analogue audio reference, for ATMS (Audio To Mobile Station) and AFMS (Audio From Mobile Station). It is connected to the DGND inside the radio device only. The application must not connect DGND and AGND.

Parameter	*Limit*
I_{max}	≅12.5mA

5.3.2 Digital Ground - DGND

DGND is the reference or return signal for all system interface digital signals and is also the d.c. return for SERVICE and the power supply, VCC. Connect all DGND pins together in your application in order to carry the current drawn by the radio device.

Parameter	*Per Pin*	*Total (5 Pins)*
I_{max}	< 6.0A	< 3.0A
I_{avg}	< 100mA	< 600mA

5.4 VCC - Regulated Power Supply Input

Pins	*Signal*	*Description*
1, 3, 5, 7, 9	VCC	regulated power supply input

Power is supplied to the radio device VCC pins, from an external source.

Connect all VCC pins together in your application in order to carry the current drawn by the radio device.

The electrical characteristics for VCC are shown in the table below.

Parameter	*Mode*	*Limit*
Vcc supply voltage	Nominal	3.6V
	Tolerance including ripple [a]	3.4V - 4.0V
	Over-voltage limit	5.5V
	Maximum ripple	<100mV @ <200kHz; <20mV @ >200kHz
Maximum allowable voltage drop	Burst transmission	200mV
Current drawn, at full TX power		<500mA (average)
		<2A (peak)

a. Measured at system connector pins.

Note! The radio device has no internal capacitance to supply the large current peaks during GSM burst transmission. We recommend you follow these general guidelines:

- Fit a low ESR electrolytic capacitor close to the radio device:
  > 1,000µF;
  < 100mΩ ESR.
- Make sure power supply to radio device line resistance is < 200mΩ.

5.5 Battery Charging Input (CHG_IN)

For battery powered applications, the radio device has a connection to aid and support battery charging. The typical design where this may be applicable is to power the radio device directly from a battery source connected to VCC (pins 1, 3, 5, 7, 9) and to provide a 5V dc power source (600mA max) to the CHG_IN connection (pin 11). The radio device can control an internal switching FET which creates a charging pathway to the battery. While power is provided at CHG_IN, the battery charge can be maintained. If the power should fail or be removed at CHG_IN, the application will be supported by the battery alone. When CHG_IN voltage returns, the battery charging and maintenance will commence once more.

Caution! Battery charging algorithms are unique to different battery types. Sony Ericsson Mobile Communications will not accept any responsibility or liability for damage, product failures, even death or injury occurring as a result of incompatible battery and charging algorithms being applied without their prior knowledge and consent.

Safety considerations should be taken into account. For example, monitoring the temperature of the battery. If the temperature of the battery exceeds its specification limits, battery charging must be stopped immediately. If the battery temperature continues to rise the application should be suspended or the battery disconnected.

Note! When charging Lithium batteries, the battery pack must have an internal protection circuit in accordance with the manufacturer's instructions.

5.6 Turning the Radio Device ON/OFF and the External Power Signal

Turning the Radio Device On

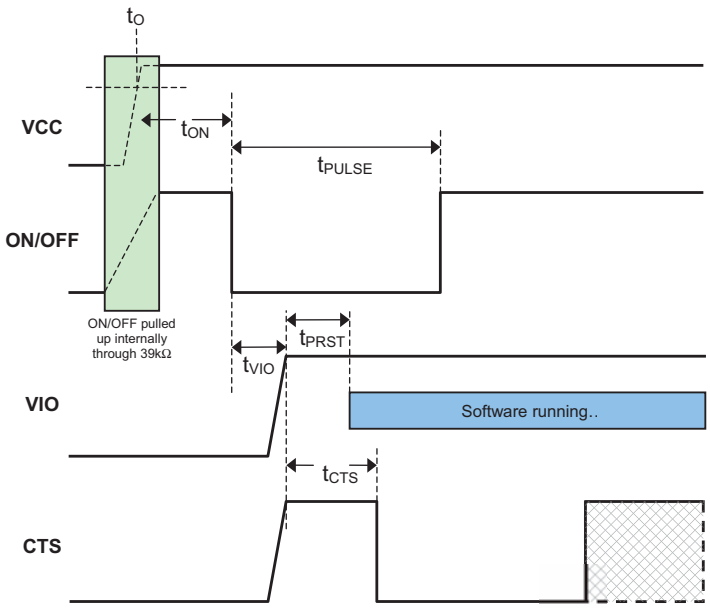

Figure 5.2 On timings and VIO performance

Symbol	*Parameters*	*Conditions*	*Min.*	*Typ*	*Max*	*Unit*
t_0	Reference time when VCC is within working limits (1)	VCC > 3.2V ON/OFF = VCC	-	-	-	-
t_{ON}	Time after t0 when the ON/OFF pulse can begin	VCC > 3.2V	0	-	-	ms

t_{VIO}	Time after start of ON/OFF pulse when VIO is active	VCC > 3.2V	-	45.0	-	ms
t_{PULSE}	Application ON/ OFF pulse width	ON/OFF held low until detected by software	400	500	-	ms
t_{PRST}	/nternal Power-on reset signal initiates software		100	-	200	ms
t_{CTS}	Time when software controlled CTS signal indicates module READY	CTS signal configured for RS232 hardware flow control, not GPIO pin	-	0.35	3.0(2)	s

(1) The GR47 measures the voltage at VCC during the power-up sequence. It is important that both VCC and ON/OFF reach a minimum of 3.2V before the ON/OFF low pulse is initiated.

(2) In SERVICE mode.

Turning the Radio Device Off

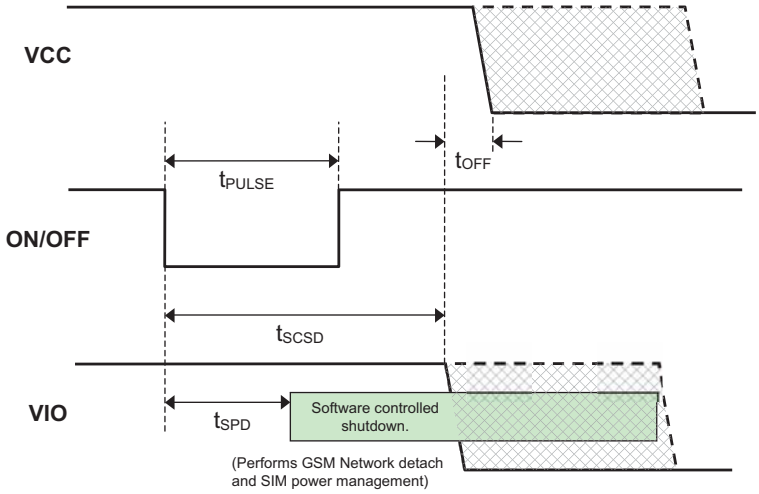

Figure 5.3 Off timings and VIO performance

Symbol	*Parameters*	*Conditions*	*Min.*	*Typ*	*Max*	*Unit*
t_{SPD}	Time for software pulse detection which initiates a software shutdown		800	-	-	ms
t_{PULSE}	Application ON/ OFF pulse width		1000	-	-	ms
t_{SCSD}	Software controlled shutdown deactivates VIO (2)		-	2.5	10(3)	s
t_{OFF}	Time when VCC power supply can be disabled	VIO is DISABLED	0	-	-	ms

(2) It is a requirement from most GSM network providers that GSM products properly detach from the network during a power-down sequence. In order to achieve this it is important that the VCC supply is not removed or turned off before VIO has been deactivated by the module.

Hard Shutdown Sequence

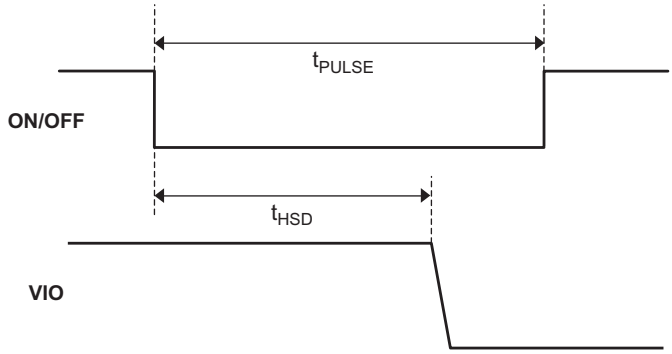

Figure 5.4 Hard Shutdown Sequence

Symbol	*Parameters*	*Conditions*	*Min.*	*Typ*	*Max*	*Unit*
t_{HSD}	Time to complete hardware shutdown		2	-	11	s
t_{PULSE}(4)	Application ON/ OFF pulse width	ON/OFF low until VIO is disabled	t_{HSD}	10	-	s

(4) To implement the Hard Shutdown of the GR47, the ON/OFF pulse must be held low until the sequence is complete. Ensure that ON/OFF is not released before VIO has been deactivated by the module.

5.6.1 VIO - 2.75V Supply

VIO provides an output voltage derived from an internal 2.75V regulator. Its electrical characteristics are shown below.

Parameter	*Min.*	*Typ.*	*Max.*	*Units*
Output Voltage (I_{load} = 50mA)	2.70	2.75	2.85	V
Load current			75	mA

You can use this output for the following:

- to indicate that the radio device is powered;
- to power interface circuits, external to the radio device.

5.7 Analogue Audio

Pin	*Signal*	*Dir*	*Description*
57	AFMS	O	Audio from mobile station
59	ATMS	I	Audio to mobile station
60	AGND	-	Ground (return) for analogue audio

ATMS is the audio input, and AFMS is the audio output, of the radio device. These signals can be used in car kit mode.

There are three factory-set audio profiles:

- portable handsfree
- handset
- car kit

Portable handsfree is the factory-set default profile. The modification, configuration, manipulation and storage of audio profiles is achieved with the AT*E2EAMS (Audio Profile Modification) and AT*E2APR (Audio Profile).

5.7.1 Audio To Mobile Station - ATMS

ATMS is the analogue audio input to the radio device. Internally, the signal is sent to the CODEC (COder/DECoder), where it is converted to digital audio in PCM (Pulse Code Modulation) format. The encoded audio is sent to PCMOUT via the internal PCM bus.

ATMS provides a DC bias when it is used as the microphone input in Portable Hands-free applications. All other sources must be a.c.-coupled to avoid attenuation of low frequencies, and to prevent incorrect biasing or damage to the ATMS input. Use a capacitor greater than the value shown in the table below.

The ATMS input is a passive network followed by the transmit part of the CODEC.

Parameter	*Limit*
Application driving impedance (0.3 - 3.5kHz)	≤300Ω
AC coupling capacitance	≥1 µF
Radio device input impedance (0.3 - 3.5kHz)	>50kΩ
Low frequency cut-off (-3dB)	300Hz ± 50Hz
High frequency cut-off (–3dB)	> 3500Hz ± 50Hz
Output d.c. bias level car kit mode	0V
Additional Gain in car kit mode	28.5dB

The following tables show the nominal PGA (programming gain settings). For more information see the relevant AT commands.

Maximum input voltage limit: 245 mV_{rms}

Input	*Input (mV_{rms})*	*TXAGC (dB)*	*AUX AMP gain*	*PCMOUT (dBm0)*
ATMS	245	0	13	3

Maximum input level at MICI, 61.4 mV_{rms} output at PCMOUT = 3 dBm0

Input	*Differential input (mV_{rms})*	*TXAGC (dB)*	*AUX AMP gain*	*PCMOUT (dBm0)*
MICN MICP	61.4	0	25	3

Output at AFMS for 3 dBm0 at PCMIN

Input	*dBm0*	*RXPGA*	*Volume control (dB)*	*AFMS (mV_{rms})*
PCMIN	3	0	0	436

Output at BEARN/BEARP for 3 dBm0 at PCMIN

Input	*dBm0*	*RXPGA*	*Volume control (dB)*	*BEAR (mV_{rms})*
PCMIN	3	0	0	388

5.7.2 Audio From Mobile Station - AFMS

AFMS is the analogue audio output from the radio device and may be used to drive a speaker or the ear-piece in a car kit.

PCM digital audio signals, entering the radio device through the PCMIN pin, are translated to analogue signals by the CODEC. See 5.8 PCM Digital Audio, page 33 for further information.

The table below shows the audio signal levels for AFMS.

Parameter	*Limit*
Speaker impedance	64Ω to 1kΩ

Parameter		*Limit*
Output Capacitance		2.2µF ±10%
Levels (THD <5%)	Drive capability into 5kΩ (0.3 - 3.5kHz)	>2.4V_{p-p}
	Drive capability into 1.5kΩ (0.3 - 3.5kHz)	>2.2V_{p-p}
	Drive capability into 150Ω (at 1kHz)	>1.3V_{p-p}

5.7.3 Microphone Signals

Pin	*Speaker signals*	*Dir*	*Function*
53	MICP	I	Microphone positive input
54	MICN	I	Microphone negative input

MICP and MICN are balanced differential microphone input pins. These inputs are compatible with an electret microphone. The microphone contains an FET buffer with an open drain output, which is supplied with at least +2V relative to ground by the radio device as shown below.

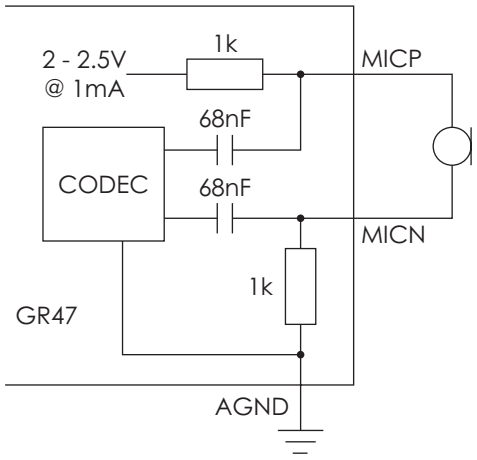

Figure 5.5 Microphone connections to the radio device

5.7.4 Speaker Signals

Pin	*Speaker signals*	*Dir*	*Function*
55	BEARP	O	Speaker positive output
56	BEARN	O	Speaker negative output

BEARP and BEARN are the speaker output pins. These are differential-mode outputs. The electrical characteristics are given in the table below.

Parameter	*Limit*
Output level (differential)	≥4.0V_{pp}
Output level (dynamic load = 32Ω)	≥2.8V_{pp}
Gain PCMIN[5] to BEARP/BEARN (differential)	−9dB ± 1
Distortion at 1kHz and maximum output level	≤5%
Offset, BEARP to BEARN	±30mV
Ear-piece mute-switch attenuation	≥40dB

[5] See PCMIN signal in 5.8 PCM Digital Audio, page 33.

The following table shows the ear piece impedances that can be connected to BEARP and BEARN.

Ear piece model	*Impedance*	*Tolerance*
Dynamic ear piece	(32Ω + 800µH) // 100pF	±20%
Dynamic ear piece	(150Ω + 800µH) // 100pF	±20%
Piezo ear piece	1kΩ + 60nF	±20%

5.8 PCM Digital Audio

Pin	*Signal*	*Dir*	*Function*
52	PCMCLK	O	PCM clock
51	PCMSYNC	O	PCM frame sync
47	PCMULD	I	PCM audio input to DSP
48	PCMDLD	O	PCM audio output from DSP
50	PCMIN	I	PCM audio input to Codec
49	PCMOUT	O	PCM audio output to Codec

Figure 5.6 shows the PCM (Pulse Code Modulation) digital audio connection for external devices. These connections can be used to process PCM digital audio signals, bypassing the radio device's internal analogue audio CODEC.

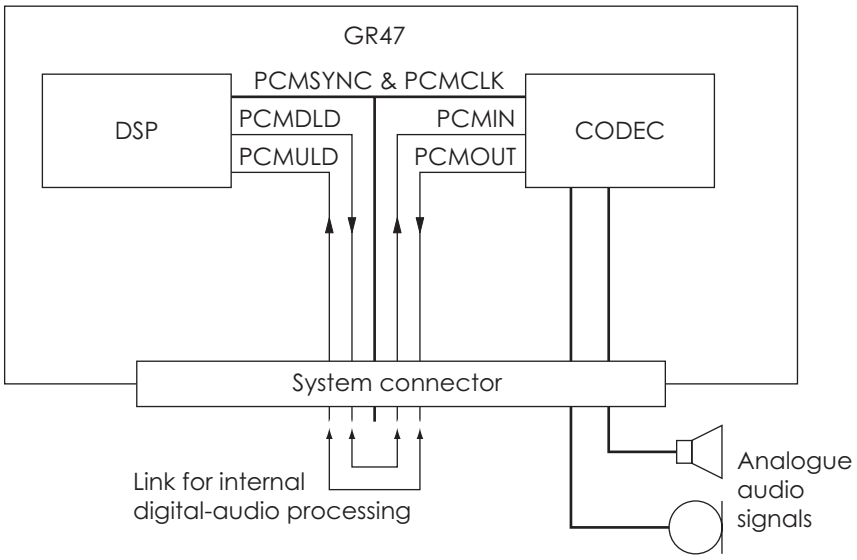

Figure 5.6 Pin connections to digital audio

Note! When no external audio processing is performed, the following pins must be connected together:

- PCMDLD to PCMIN
- PCMULD to PCMOUT

Electrical characteristics

Digital 2.75 V CMOS input/output electrical characteristics apply.

5.8.1 PCM Data Format

All of the radio device's PCM signals, including signals between its CODEC and DSP conform to the PCM data I/O format of the industry standard DSP from Texas Instruments.

PCMCLK (bit clock) and PCMSYNC (frame synchronisation) are both generated by the DSP within the radio device.

The DSP within the radio device is the master therefore all external PCM clocks and data from external devices must be synchronized to it

13-Bit PCM Mode

Bit	*Contents*
D15 to D14	Equal to D13
D13 to D1	Two's complement of the 13-bit PCM
D0	LSB, not used

The radio device implements 13-bit PCM with the 13-bit data embedded in a 16-bit word within a 24-bit frame (see Figure 5.8). Each PCM word contains 16-bits: D0 to D15. D13 to D1 is the two's complement value of the 13-bit PCM, with D13 as the sign bit. D14 and D15 are always set to be equivalent with D13. D0, the LSB, is not used as shown in Figure 5.7 below.

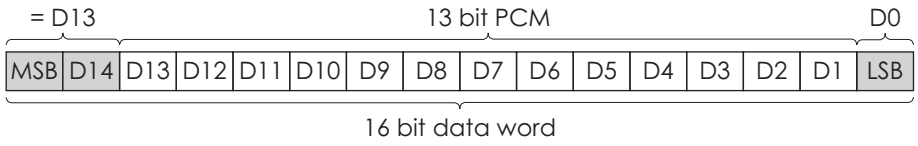

Figure 5.7 16-bit data word format

16-Bit PCM Mode

Bit	*Contents*
D15 - D0	Two's complement

The frame format is equal to the one shown in Figure 5.7, but with D15, D14 and D0 filled with significant bits. D15 to D0 is the two's complement value of the 16-bit PCM with bit 15 as the sign bit.

PCM Timing Diagrams

The PCM timing is shown in Figure 5.8 below and it is seen that the CPU has 45 µs to serve an interrupt and setup data channels. Data is sent on the falling edge of the sync pulse. The data bits in PCMULD and PCMDLD are aligned so that the MSB in each word occurs on the same clock edge as shown in Figure 5.9.

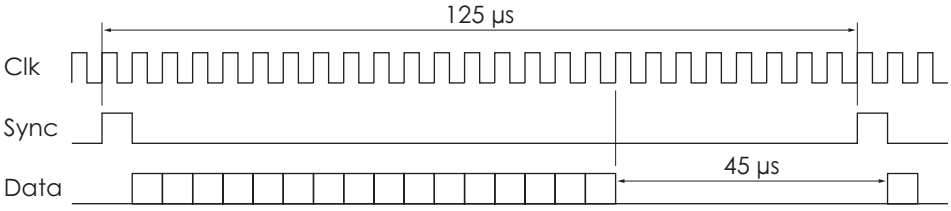

Figure 5.8 16-bit word within 24-bit frame

PCM signal timing is shown in Figure 5.9. The signals characteristics are described in the tables following Figure 5.9.

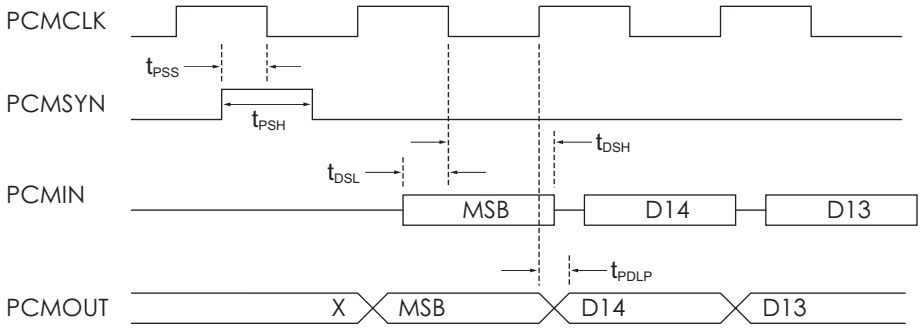

Figure 5.9 PCM Timing Diagram

Name	*Description*	*Typ.*	*Unit*
t_{PSS}	PCMSYN (setup) to PCMCLK (fall)	2.5	µs
t_{PSH}	PCMSYN pulse length	5	µs
t_{DSL}	PCMI (setup) to PCMCLK (fall)	2.5	µs
t_{DSH}	PCMI (hold) from PCMCLK (fall)	2.5	µs
t_{PDLP}	PCMO valid from PCMCLK (rise)	2.5	µs

Name	*Description*	*Typ.*	*Unit*
F_{PCMCLK}	PCM clock frequency	200	kHz
T_{PCMCLK}	PCM clock period with 50/50 mark space ratio	5	µs
F_{PCMSYN}	PCM sync frequency	8	kHz

Typical Rise/Fall times	*Rise Time*	*Fall Time*	*Unit*
PCMCLK	19	18	ns
PCMSYN	19	15	ns
PCMOUT	900	900	ns
PCMDLD	20	19	ns

5.9 Serial Data Interfaces

Pin	*Signal*	*Dir*	*Description*	*RS232 CCITT N°*
41	TD	I	Serial data to radio device (UART1)	103
42	RD	O	Serial data from radio device (UART1)	104
39	RTS IO9	I I/O	Request To Send (UART1) General purpose input/output 9	105
40	CTS KeyCOL4 O4	O O O	Clear To Send (UART1) Key column 4 General purpose output 4	106
37	DTR KeyROW1 IN1	I I	Data Terminal Ready (UART1) Keyboard row 1 General purpose input 1	108.2
32	DSR KeyCOL3 O3	O O O	Data Set Ready (UART) Key column 3 General purpose output 3	107
38	DCD KeyCOL 1 O1	O O O	Data Carrier Detect (UART1) Key column 1 General purpose output 1	109
36	RI KeyCOL 2 O2	O O O	Ring Indicator (UART1) Key Column 2 General output 2	125
45	TD2	I	Transmitted Data (UART2)	
46	RD2	O	Received Data (UART2)	
43	TD3	I	Transmitted Data (UART3)	
44	RD3	O	Received Data (UART3)	

The serial channels, consisting of three UARTs, are asynchronous communication links to the application or accessory units.

- UART1 has RS-232 functionality and is used for all on- and off -line communication.
- UART2 behaves as a general-purpose serial data link. For example, it can be used for GPS, downloading software and receiving logging information.
- UART3 behaves as a general-purpose serial data link. It can be used by an embedded application.

Digital 2.75 V CMOS input/output electrical characteristics apply.

The standard character format consists of 1 start bit, 8 bit data, no parity and 1 stop bit. In all, there are 10 bits per character.

5.9.1 UART1 (RS232) - RD, TD, RTS, CTS, DTR, DSR, DCD and RI

UART1 signals conform to a 9-pin RS232 (V.24) serial port.

Note! UART1 signal levels do not match standard RS232 (V.28) levels. The relationship between the levels is shown in the table below.

RS232 level	*RD, TD*	*RTS, CTS, DTR, DSR, DCD, RI*	*CMOS level*
<–3V	1	OFF	>1.93V
>+3V	0	ON	<0.80V

Conversion between the radio device CMOS levels and RS232 levels can be achieved using a standard interface IC, such as the Maxim Integrated Products MAX3237.

5.9.2 Serial Data Signals - RD, TD

The default baud rate is 9.6kbits/s, however higher bit rates of up to 460 kbits/s are supported, set by an AT command. UART1 starts at a rate of 9.6kbits/s in standard AT command mode. The radio device also supports GSM 07.10 multiplexing protocol and starts when the appropriate command is sent.

Serial Data From Radio Device (RD)

RD is an output signal that the radio device uses to send data via UART1 to the application.

Parameter	*Limit*
Application load resistance	<100kΩ
Application load capacitance	<100pF

Serial Data To Radio Device (TD)

TD is an input signal, used by the application to send data via UART1 to the radio device.

Parameter	*Limit*
Application driving impedance	<100Ω
Input capacitance	1nF
Input resistance	100kΩ to 2.75 V

5.9.3 Control Signals - RTS, CTS, DTR, DSR, DCD, RI

UART1 control signals are active low and need a standard interface IC, such as the MAX3237, to generate standard RS232 levels.

UART1 converted signals, together with DGND, RD and TD form a 9-pin RS232 data port.

RTS and CTS are capable of transmitting at $1/10^{th}$ of the data transmission speed for data rates up to 460 kbit/s (byte-oriented flow control mechanism).

Note! When hardware flow control is not used in communications between the application and the radio device, RTS and CTS must be connected to each other at the radio device.

Switching times for RTS and CTS

The table below shows the switching times.

Parameter	*Limit*
Time from Low to High level	<2 µs
Time from High to Low level	<2 µs

Request to Send (RTS)

Used to condition the DCE for data transmission. The default level is high by internal pull up.

The application must pull RTS low to enable data transmission from the radio device. Similarly, the radio device asserts CTS low, indicating it is ready to receive data transmission from the host.

Parameter	*Limit*
Application driving impedance	<100 Ω
Input capacitance	<2 nF
Input resistance (pull-up)	100 kΩ to DGND

Clear To Send (CTS)

CTS is asserted by the DCE to indicate that the host (DTE) may transmit data. When CTS is high, the host (DTE) is not permitted to transmit data.

The table below shows the load characteristics for this signal.

Parameter	*Limit*
Application load capacitance	<500 pF
Application load resistance	≥1 MΩ

Data Terminal Ready (DTR)

DTR indicates that the DTE is ready to receive data. It also acts as a hardware 'hang-up', terminating calls when switched high. The signal is active low. You can define the exact behaviour of DTR with an AT command.

Data Set Ready (DSR)

DSR indicates that the DCE is ready to receive data. The signal is active low.

Data Carrier Detect (DCD)

DCD indicates that the DCE is receiving a valid carrier (data signal) when low.

Ring Indicator (RI)

RI indicates that a ringing signal is being received by the DCE when low. You can define the exact behaviour of RI with an AT command.

5.9.4 UART2 - TD2, RD2

UART 2 consists of a full duplex serial communication port with transmission and reception lines.

This communication port works in a mode called Operation and Maintenance.

Operation and Maintenance mode works in combination with the SERVICE signal. Two events are possible if the SERVICE signal is active when the radio device is turned on. These are:

- the radio device is reprogrammed if UART2 is connected to a computer running Sony Ericsson update software;
- the radio device enters logging mode and sends data to UART2 if no reprogramming information is received.

Timing and electrical signals characteristics are the same as for UART1, TD and RD, except for maximum baud rate which could increase to 921 kbps.

Transmitted Data 2 (TD2)

TD2 is used by the application to send data to the radio device via UART2. It has the same electrical characteristics as TD.

Received Data 2 (RD2)

RD2 is used to send data to the application via UART2. It has the same electrical characteristics as RD.

5.9.5 UART3 - TD3, RD3

UART3 is a full duplex serial communication port with transmission and reception lines. It has the same timing and electrical signal characteristics as UART1, TD and RD.

Transmitted Data 3 (TD3)

TD3 is used by your application to send data to the radio device via UART3.

Received Data 3 (RD3)

RD3 is used to send data to your application via UART3.

5.10 SIM Card Related Signals

Pin	*Signal*	*Dir*	*Description*
15	SIMVCC	-	SIM card power supply
16	SIMPRESENCE	I	SIM card presence
17	SIMRST	O	SIM card reset
19	SIMCLK	O	SIM card clock
18	SIMDATA	I/O	SIM card data

These connections allow you to communicate with the SIM card holder in your application.

Note! The distance between the SIM card holder and the radio device can be up to 25cm.

This SIM interface allows the use of 3 V and 5 V SIM cards. By default it works on 3 V levels but will automatically switch to 5 V, if a 5 V SIM card is fitted.

SIM voltage levels, as shown in the following table, are dependent on the type of SIM card detected by the radio device.

Signal	*Parameter*	*Mode*	*Min.*	*Typ.*	*Max.*	*Unit*
SIMVCC	SIM supply voltage	3V	2.7	3.0	3.3	V
		5V	4.5	5.0	5.5	V
SIMDAT	High Level Input voltage (V_{IH})	3V	2.1		3.0	V
		5V	3.5		5.0	V
SIMDAT	Low Level Input voltage (V_{IL})	3V	0		0.9	V
		5V	0		1.5	V

Signal	*Parameter*	*Mode*	*Min.*	*Typ.*	*Max.*	*Unit*
SIMDAT	High Level Output voltage (V_{OH})	3V	2.7		3.0	V
		5V	4.7		5.0	V
SIMDAT	Low Level Output voltage (V_{OL})	3V	0		0.2	V
		5V	0		0.2	V
SIMCLK SIMRST	High Level Output voltage (V_{OH})	3V	2.4		3.0	V
		5V	4.4		5.0	V
SIMCLK SIMRST	Low Level Output voltage (V_{OL})	3V	0		0.35	V
		5V	0		0.3	V

5.10.1 SIM Detection - SIMPRESENCE

SIMPRESENCE is used to determine whether a SIM card has been inserted into or removed from the SIM card holder. You should normally wire it to the "card inserted switch" of the SIM card holder, but different implementations are possible.

When left open, an internal pull-up resistor maintains the signal high and means "SIM card missing" to the radio device. When pulled low the radio device assumes a SIM card is inserted.

SIMPRESENCE is a Digital 2.75V CMOS input with the following electrical characteristics.

Parameter	*Min.*	*Typ.*	*Max.*	*Units*
Pull-up resistance (at 2.75 V)	100			kΩ
Low Level Input voltage (SIM inserted)			0.80	V
High Level Input voltage (SIM missing)	>1.93		2.75	V

Note! To meet regulatory approvals SIMPRESENCE must be implemented.

5.11 Service/Programming

Pin	*Signal*	*Dir*	*Description*
58	SERVICE	I	Flash programming voltage

When the SERVICE input signal is active the radio device will:

- be reprogrammed if data is received through UART2 from a computer running Sony Ericsson reprogramming software;
- or it will output logging data on UART2.

The electrical characteristics are given below. The signal reference is DGND.

Mode	*SERVICE Voltage (V)*			*Drive Capacity*
	Min.	*Typ.*	*Max.*	
Normal Operation			0.8	-
Service/enable programming	1.9	2.75V	3.6	>1mA
Absolute maximum voltage			13.5	

5.12 Buzzer

Pin	*Signal*	*Dir*	*Description*
31	BUZZER	O	Buzzer output from radio device

Connecting the BUZZER signal to an inverting transistor-buffer followed by a piezoelectric transducer enables the radio device to play pre-programmed melodies or sounds.

5.13 LED

Pin	*Signal*	*Dir*	*Description*
33	LED	O	LED Output from radio device

The LED states shown below, are hard coded.

LED indication	*Operational status*
No indication	No power or in the OFF state
Green, steady	Power on, not connected to a network
Green, blinking	Power on, connected to a network

The following circuit can be used to connect an LED.

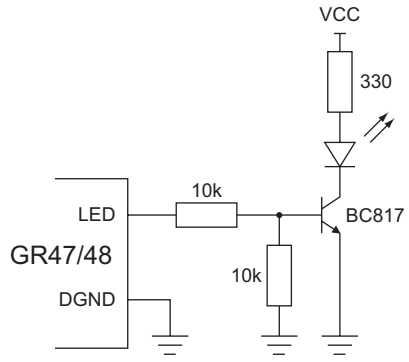

Figure 5.10 Electrical connections for the LED

5.14 General Purpose Digital I/O Ports

Pin	*I/O port signal*	*Default signal*	*Description*
21	IO1	IO1	Programmable Input/Output 1 KEYRow2
22	IO2	IO2	Programmable Input/Output 2 ADC5
23	IO3	IO3	Programmable Input/Output 3 KEYRow3
24	IO4	IO4	Programmable Input/Output 4 KEYRow4
13	IO5	IO5	Programmable Input/Output 5 ADC4
33	IO6	LED	Programmable Input/Output 6/LED
43	IO7	TD3	Programmable Input/Output 7/TD3
44	IO8	RD3	Programmable Input/Output 8/RD3
39	IO9	RTS	Programmable Input/Output 9/RTS
37	IN1	DTR	Programmable Input 1 Data Terminal Ready
32	OUT3	DSR	Programmable Output 3/DSR
36	OUT2	RI	Programmable Output 2/RI Ring Indicator
38	OUT1	DCD	Programmable Output 1/DCD Data Carrier Detect
40	OUT4	CTS	Programmable Input/Output 4/CTS

Signals which have an entry in the Default Signal column in the above table are multiplexed.

The operational modes of multiplexed signals are controlled by AT commands and also by intrinsic functions available to an embedded

The following table gives you the input impedance. These values only apply when the ports are configured as input signals.

Parameter	*Min.*	*Typ.*	*Max.*	*Units*
Input impedance (pull-up)	50	100	120	kΩ

Notes! I/O6 (LED) doesn't have an internal pull up. If this pin is configured as an input, it should not be left floating.
I/O7 (TD3) has a pull down instead of a pull up.

5.15 Extended I/O capabilities

To increase flexibility and variety of radio device peripherals, the RS232 hardware flow control shares its physical interface with the keypad scanning interface and the extended general purpose I/O capability. This sharing means that it is not feasible to operate all these features concurrently, however, with care, dynamic switching from one feature to another is possible.

Using Embedded Applications

When a particular I/O feature is required, the user sets the state of the relevant I/O blocks by disabling one set before enabling others.

The radio device checks the state of the I/O when the user requests a new function. The new function is rejected if the current function is not released first.

Note! Only the states of I/O1 - I/O5 are retained for the next power up. For example, inputs remain as inputs and outputs remain as outputs. The voltage of a defined output pin will still drop to 0 Volts in the radio device power down state.

5.15.1 LED/IO6 Capabilities

The LED function pin can be used as a general purpose digital I/O when the flashing LED function is not required. However, this pin does not have an on-board pull-up resistor. It is required that an external pull-up or pull-down resistor be provided by the host circuitry when either not used or when used as a digital input.

5.15.2 I#/O#

If pins labelled I# and O# are not being used for an alternative function they may be used for general purpose inputs or outputs respectively. The inputs have an on-board 100k pull-up resistor and the outputs are driven rail-to-rail at 2.75V levels.

5.15.3 UART3/IO#

The UART3 pins have been given alternative functions as general purpose I/O, both pins may be used for either input or output. However, the TX pin has a 100kΩ pull-down resistor to ground and the RX pin has a 100kΩ pull-up resistor to 2.75V. This must be taken into consideration when designing the host circuit.

5.15.4 IO#/ADC#

To increase analog input capabilities, the radio device optimises the I/O by multiplexing or sharing different features on single pins. There are two digital I/O pins which now have an additional ADC input. When configured as digital I/O, the software will not read the voltages at the two new ADC inputs. When configured as ADC inputs the software will configure the digital I/O pins as input or high impedance tri-state. In this state any applied voltage between 0V and 2.75V can be read as an 8 bit value.

Because the additional ADC inputs (ADC4 and ADC5) are common with digital I/O, the input circuit of the ADC is not the same as for the original circuits ADC1-3. It is important to understand the input structure of the pin so that the correct analog voltage is read by the application.

5.16 General Purpose Analogue I/O Ports

Pin	*Signal*	*Dir*	*Description*
20	DAC	O	Digital to analogue conversion output
26	ADC1	I	Analogue to digital conversion input 1
27	ADC2	I	Analogue to digital conversion input 2
28	ADC3	I	Analogue to digital conversion input 3
13	ADC4 (I/O5)	I (I/O)	Analogue to digital conversion input 4
22	ADC5 (I/O2)	I (I/O)	Analogue to digital conversion input 5

The radio device is able to convert digital to analogue signals and vice versa.

5.16.1 Digital to Analogue Converter - DAC

The DAC is an 8-bit converter. Conversion takes place when an AT command is sent to the radio device. The radio device sends the resulting analogue value to the DAC pin.
Tolerance on this internal voltage is ±5%

DAC output electrical characteristics are given in the following table.

Parameter	*Limit*	*Units*
Resolution	8	Bits
Output voltage for code = 0	(2.75[6] x 0.05) ± 0.05	V
Output voltage for code = 255	(2.75[6] x 0.95) ± 0.05	V
Nominal step size	(2.75[6] x 0.9)/256	mV
Absolute error[7]	≤ ± 0.5	mV
Output wide-band noise and clock feed-through 0-1.1MHz	≤0.5	mV_{rms}
Power-supply rejection ratio 50Hz - 10kHz	≥40	dB
Conversion rate ± 0.5LSB	≤2 (Load A)[8]	ms
	≤50 (Load B)[8]	ms
Output buffer impedance when disabled	≥50	kΩ
Output current source or sink	≥1	mA
Current consumption (active)	≤1.0	mA

[6]Tolerance on this internal voltage is ±5%
[7]Referred to the ideal conversion characteristic.
[8]See Figure 5.11, page 46

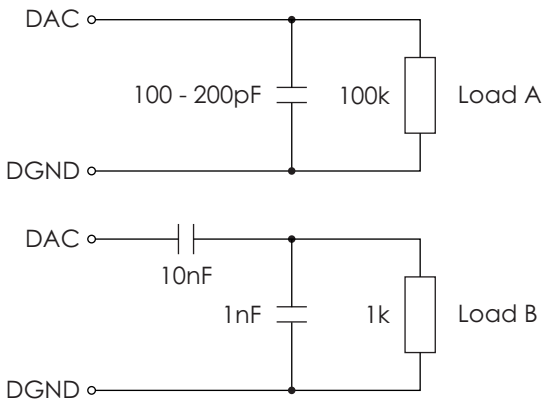

Figure 5.11 DAC loads

5.16.2 Analogue to Digital Converters 1, 2 and 3 - ADCx

The ADC is an 8-bit converter. An analogue value applied to any of the ADC pins is converted and stored in a register inside the radio device. When the appropriate AT command is received by the radio device, the digital value stored in the register is read.

ADC electrical characteristics are shown in the table below.

Parameter	*Min.*	*Max.*	*Units*
Resolution	8	8	Bits
Input voltage for 0000 0000 word	0	0.01 x 2.75[9]	V
Input voltage for 1111 1111 word	0.99 x 2.75[9]	2.75[9]	V
Differential Non-Linearity (DNL)		±0.75	LSB
Overall Non-Linearity (INL)		±0.60	LSB
Absolute accuracy		±1.5	LSB
Input impedance	1		MΩ
Average supply current (continuous conversion)		1	mA
External source impedance		50	kΩ

[9] Tolerance on this internal voltage is ±5%

5.16.3 Analogue to Digital Converters 4 and 5 - IOx/ADCx

To increase analog input capabilities, the GR47 optimises the I/O by multiplexing or sharing different features on single pins. There are two ADC inputs which share system connector pins with digital I/O signals. When configured as digital I/O, the software will not read the voltages at the two new ADC inputs. When configured as ADC inputs the software will configure the digital I/O pins as input or high impedance tri-state. In this state any applied voltage between 0V and 2.75V can be read as an 8 bit value.

Because the ADC inputs, ADC4 and ADC5, are common with digital I/O, the input circuit of these Adds is not the same as for the circuits ADC1, ADC2 and ADC3. It is important to understand the input structure of the pin so that the correct analog voltage is read by the application (at position 'A' in Figure 5.12 below). The input structure is provided in Figure 5.12. It consists of a 100kΩ pull-up to 2.75V followed by a series 10kΩ and 1nF capacitor to ground which make a low pass filter with a 3dB roll-off at about 16kHz. The input impedance of the analog IC is 1MΩ minimum. At position 'A' in Figure 5.12 below, the input characteristics are the same as for the table above.

Note! If the voltage of the signal to be measured may be altered by the internal circuitry of this shared signal, then the application should use ADC1, ADC2 or ADC3 instead.

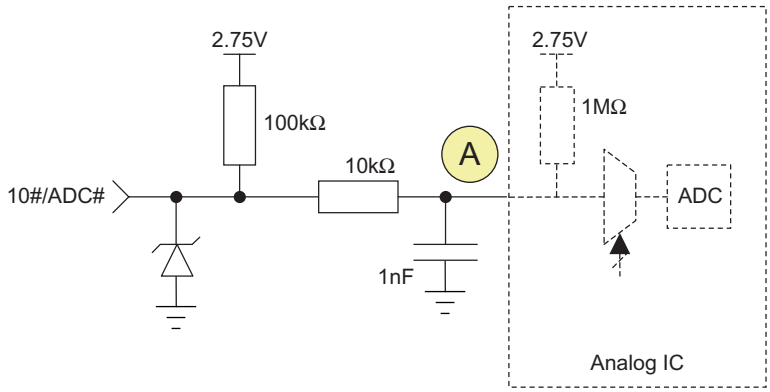

Figure 5.12 Input circuit for combined digital I/O and ADC pins

5.17 External I²C Serial Control Bus

Pin	*Signal*	*Dir*	*Description*
29	SDA	I/O	I²C serial data
30	SCL	O	I²C serial clock

The I²C bus is controlled by embedded application script commands.

The external I²C bus consists of two signals, SDA and SCL. This bus is isolated from the radio device's internal I²C bus to ensure proper operation of the radio device, in the event of the external I²C bus being damaged.

The electrical characteristics are shown below.

	Parameter	*Min.*	*Typ.*	*Max.*	*Units*
Transmit operation	Frequency I²C CLK	81.25		400	kHz
	High or low I²C CLK	1.2			µs
	Delay time after falling edge of I²C CLK	308	308-1230		ns
	Hold time after falling edge of I²C CLK	0			ns

	Parameter	Min.	Typ.	Max.	Units
Receive operation	Frequency I^2C CLK			400	kHz
	High or low I^2C CLK	1.2			µs
	Delay time after falling edge of I^2C CLK	100			ns
	Hold time after falling edge of I^2C CLK	0			ns

5.18 TX_ON - Burst Transmission

Pin	Signal	Dir	Description
35	TX_ON	O	GSM radio device to transmit

Burst transmission is the time when a GSM transceiver unit is transmitting RF signals. TX_ON indicates the radio device is going into transmission mode.

5.19 Real Time Clock

Pin	Signal	Dir	Description
25	VRTC	-	Voltage for the Real Time Clock

The Real Time Clock (RTC) provides the main microprocessor with a time-of-day calendar and alarm, and a one-hundred-year calendar. Its accuracy is shown in the table below

Parameter	Min.	Typ.	Max.	Units
RTC accuracy	25°C	8 (21)	20 (52)	ppm (s/month)
RTC accuracy	extreme temperatures	89 (231)	101 (262)	ppm (s/month)

The Real Time Clock operates in two modes when connected to a separate power supply:

- RTC normal mode: the radio device is in ON or OFF mode and it is supplied with power (VCC is applied).
- RTC back-up mode: VCC is disconnected and the RTC is maintained by a separate backup power supply connected to the VRTC input (see Figure 5.13 below).

Backup power is provided by a capacitor, golden-capacitor or battery in your application and must be connected to the VRTC pin. During RTC normal operation, the back up source will be charged.