APPENDIX I: MANUAL

Please refer to the following pages.

Pronghorn 802.11 Application Platform

Hardware Manual

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ADI Engineering guarantees that every Pronghorn 802.11 Application Platform will be free from physical defects in material and workmanship for one year from the date of purchase, when used within the limits set forth in the Specifications section of this User Guide. If the product proves defective during this warranty period, call ADI Engineering Technical Support in order to obtain a Return Authorization number. When returning a product, mark the Return Authorization number clearly on the outside of the package and include a copy of your original proof of purchase. All customers shall be held responsible for return shipping and handling charges.

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FCC STATEMENT

The Pronghorn 802.11 Application Platform has been tested and found to comply with the specifications for a Class B digital device, pursuant to Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and
(2) This device must accept any interference received, including interference that may cause undesired operation.

These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used according to the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which is found by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment or devices
- Connect the equipment to an outlet other than the receiver's
- Consult a dealer or an experienced radio/TV technician for assistance

FCC Caution: Any change or modification to the product not expressly approved by ADI Engineering could void the user's authority to operate the device.

FCC Caution: Operation within the 5150 to 5250GHz band is restricted to indoor use only.

FCC RF Radiation Exposure Statement

To comply with the FCC and ANSI C95.1 RF exposure limits, the antenna(s) for this device must comply with the following:

- Access points with 2.4 GHz or 5 GHz integrated antenna must operate with a separation distance of at least 20 cm from all persons using the cable provided and must not be co-located or operating in conjunction with any other antenna or transmitter.

End-users must be provided with specific operations for satisfying RF exposure compliance.
Note: Dual antennas used for diversity operation are not considered co-located.

Canadian Department of Communications Industry Canada (IC) Notice
This Class B digital apparatus complies with Canadian ICES-003 and RSS-210.
Cet appareil numérique de la classe B est conforme à la norme NMB-003 et CNR-210 du Canada.
"To prevent radio interference to the licensed service, this device is intended to be operated indoors and away from windows to provide maximum shielding. Equipment (or its transmit antenna) that is installed outdoors is subject to licensing."
" Pour empêcher que cet appareil cause du brouillage au service faisant l'objet d'une licence, il doit être utilisé à l'intérieur et devrait être placé loin des fenêtres afin de fournir un écran de blindage maximal. Si le matériel (ou son antenne d'émission) est installé à l'extérieur, il doit faire l'objet d'une licence. "

Revisions

Date	Revision	Page-paragraph	Remarks
6 Aug04	0.01	All	New Document based off Coyote manual
20Sep04	0.02	All	Incorporated comments from the team
25Sep04	0.03	All	Incorporated further comments from team
25Oct04	0.04	All	Added Antenna Gain, FCC language

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1 Introduction

This document provides an overview of the ADI Engineering Pronghorn 802.11 Application Platform based on the Intel ® IXP42x network processor. It contains the hardware description and outlines the procedures for demonstrating typical functionalities of an 802.11 access point.

The ADI Engineering Pronghorn 802.11 Application Platform consists of a set of building blocks and functionalities needed for a typical enterprise 802.11 wireless access point. The Pronghorn Development Kit has an IXP425 network processor, SDRAM memory, flash memory, two Ethernet ports (one with 802.3af power-over-Ethernet), and two Mini PCI interfaces (one for the 802.11 b/g or a/b/g radio, and another for optional customer hardware). It also contains two high-gain external antennas and enclosure.

Pronghorn is designed to be a turnkey hardware/software product solution for original equipment manufacturers (OEM). ADI Engineering can quickly adapt Pronghorn to meet specific OEM end product requirements. Pronghorn is also intended to demonstrate the scalability of the IXP425 network processor family for an 802.11 system by supporting new applications and incremental additions to existing applications with the available headroom at the core and network processing engines.

It is assumed the reader has a basic understanding of computing systems and the subsystems that support their operation.

1.1 Terms/Acronyms

AFE	- Analog Front End
ARM™	- uProcessor Architecture created by ARM (Advanced RISC Machines) Limited
BOM	- Bill of Material
CO	- Central Office
Pronghorn	- ADI Engineering 802.11 Application Platform based on the Intel ® IXP425 network processor
CPE	- Customer Premise Equipment
CS	- Chip Select
DLL	- Delay Locked-Loop (similar to phase-locked loop)
DMT	- Discrete Multi-tone
DNP	- Do not populate
DWORD	- Double Word, 32 bits of data
ECC	- Error Correction Code
EEPROM	- Electrically Erasable and Programmable, Read-only Memory
GPIO	- General purpose Input/Output
GUI	- Graphical User Interface
HPI	- Host Port Interface
HSS	- High Speed Serial
I2C	- Inter IC Communication
ICE	- In-circuit Emulator
IXP425	- Intel ® IXP425 Network Processor
JTAG	- Joint Test Access Group
LAN	- Local Area Network
LED	- Light Emitting Diode
LSP	- Linux Source Package
MII	- Media Independent Interface
PCB	- Printed Circuit Board
PCI	- Peripheral Component Interconnect
PHY	- Physical Layer
PLL	- Phase Lock Loop

PWA	- Printed Wiring Assembly
QWORD	- Quad Word, 64 bits of data
RMII	- Reduced, Media Independent Interface
ROM	- Read Only Memory
SME	- Small and Medium Enterprise
SOHO	- Small Office/Home Office
TCK	- Test Clock
TDI	- Test Data In
TDO	- Test Data Out
TFTP	- Trivial File Transfer Protocol
TMS	- Test Mode Strobe
TP	- Test Point
UART	- Universal Asynchronous Receiver Transceiver
URL	- Uniform Resource Locator (Internet address)
WAN	- Wide Area Network
WORD	- 16 bits of data

2 Platform Overview

The Pronghorn has all the components of a typical enterprise 802.11 access point including the interface for LAN, and WAN. The 802.11 WLAN connectivity is achieved through industry standard Mini PCI expansion cards. The platform specifications are shown in Table 1. The board block diagram is shown below in Figure 1.

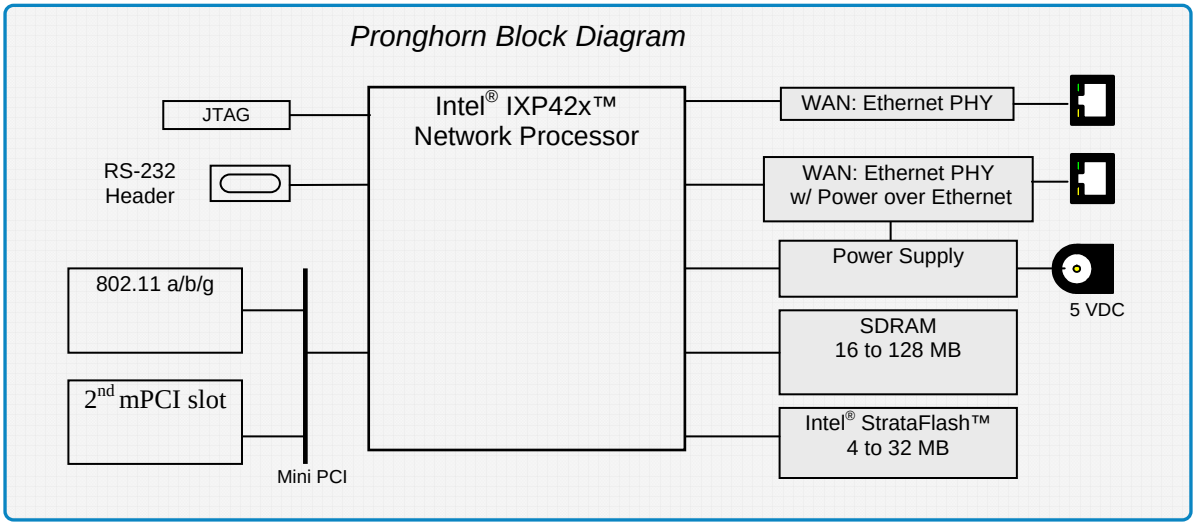


Figure 1. Pronghorn 802.11 Application Platform Block Diagram

Table 1. Pronghorn 802.11 Application Platform Specifications

Hardware Specification	***Development Kit***	***Platform options***
Processor	Intel ® IXP425, 533MHz	IXP42x in 266, 400, or 533 MHz
Memory		
SDRAM	64Mbyte, PC-133 compatible	16, 32, 64, or 128 MB
Flash	16Mbyte, 100 - 150nS	4, 8, 16, 32 MB
IO		
Ethernet	Two 10/100Base-T	One 10/100 Base-T is optional
Serial – Header	16550 compliant, 115.2Kbps, adapter required	
PCI	Two Mini PCI connectors Primary used for 802.11 WLAN	One Mini PCI connector is optional
Power		
Power-over-Ethernet	48VDC, via primary RJ-45 connector, 802.3af compliant	
External power brick	5VDC, 2.25A nominal, coax connector	Power brick is optional in production
On-board voltages	5.0V @ 2.5A, 3.3V @ 2.0A, 1.3V @ 2A	
Debug Support	IXP42x JTAG Header	JTAG optional in production
Other	4 LED's	One LED is optional

2.1 Processor

The IXP425 network processor can operate at clock speeds of 266 MHz, 400 MHz, or 533 MHz. An external 33.333-MHz oscillator (MMD M13050H48M) acts as the input clock signal at OSC_IN of the IXP425 network processor.

The IXP425 network processor's primary features are:

- Intel ® XScale™ Core running the system clock rate of 133 MHz at ratios of x2, x3, and x4.
- Three NPEs for Layer-2 packet/frame network processing.
- Two 10/100-Mbps, full-duplex IEEE-802.3 MAC's with MII interface
- Dedicated SDRAM with 32-bit memory interface operating at 133 MHz (equal to system clock frequency)
  - Supports up to two banks, each two chips, of two- and three-cycle CAS latency
  - 13-bit address: Maximum, 256 Mbyte; minimum, 32 Mbyte.
- Expansion Bus
  - 24-bit address
  - 16-bit data
  - Eight chip selects
  - Glueless interface to Intel flash and Motorola- and Intel-mode peripherals
- HPI bus (pins shared with expansion bus) — Compliant with Texas Instruments * HPI, HPI-8, HPI-16 bus host-peripheral-interface protocols
- UTOPIA-2 interface, 8-bit data path
- Two high-speed, serial TDM buses: HSS-0 and HSS-1.
- Two UARTS
  - One fast (921-Kbaud) used for supporting one Bluetooth * device (not supported on Pronghorn)
  - One standard (230.4-Kbaud) used for OS console monitoring
- PCI 2.2 bus:
  - 32-bit address/data bus
  - 33 and 66 MHz
  - Built-in arbiter supports up to four external bus masters
- 16 GPIOs
- USB 1.1 device controller supporting full-speed, USB v 1.1 data rate (port not available on Pronghorn)

The high-level view of the IXP425 network processor is shown in Figure 2. The internal bus is partitioned into two segments and data transactions between the network processing elements and RAM, and CPU may be performed concurrently. The CPU bus is bridged to the system PCI bus. The SDRAM controller can support fast SDRAMs with different organizations.

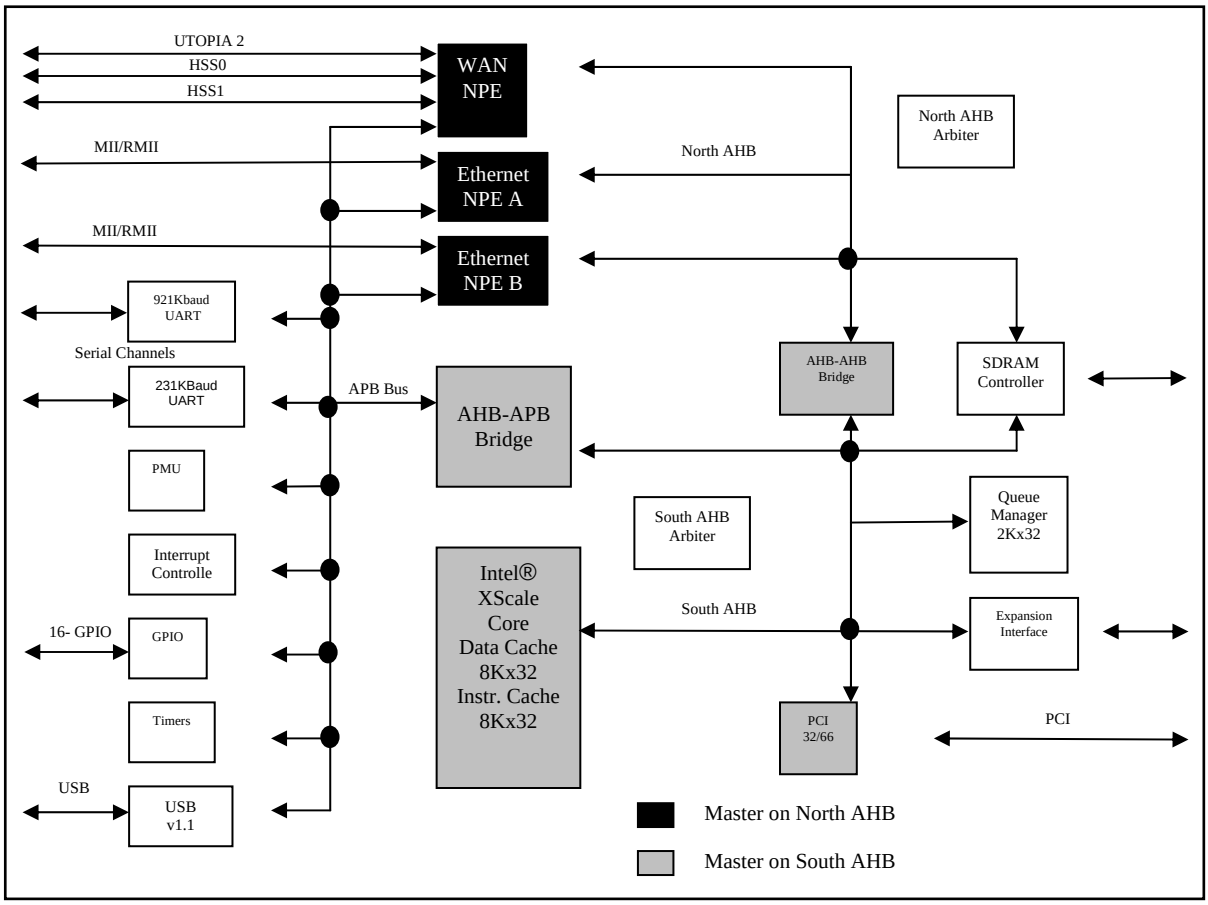


Figure 2. Intel ® IXP425 Network Processor: High-Level View

2.2 Memory Map

The IXP425 network processor implements a single address map that is used for all internal memory and register space. The complete address space consists of 2^32 byte addressable locations.

Table 2. Intel ® IXP425 Network Processor: Memory Map

Start Address	End Address	Size	Description
0000_0000	0FFF_FFFF	256 Mbyte	Expansion-bus data
0000_0000	3FFF_FFFF	1 Gbyte	SDRAM data
4000_0000	47FF_FFFF	128 Mbyte	Reserved
4800_0000	4FFF_FFFF	128 Mbyte	PCI data
5000_0000	5FFF_FFFF	256 Mbyte	Expansion-bus data
6000_0000	63FF_FFFF	64 Mbyte	Queue manager
6400_0000	BFFF_FFFF		Reserved
C000_0000	C000_00FF	256 Mbyte	PCI configuration registers
C000_0100	C3FF_FFFF		Reserved
C400_0000	C400_00FF	256 Mbyte	Expansion-bus configuration registers
C400_0100	C7FF_FFFF		Reserved
C800_0000	C800_0FFF	1 Kbyte	Fast UART (not available on Pronghorn)
C800_1000	C800_1FFF	1 Kbyte	Console UART

C800_2000	C800_2FFF	1 Kbyte	Internal Bus Performance Monitoring Unit (PMU)
C800_3000	C800_3FFF	1 Kbyte	Interrupt controller
C800_4000	C800_4FFF	1 Kbyte	GPIO controller
C800_5000	C800_5FFF	1 Kbyte	Timers
C800_6000	C800_6FFF	1 Kbyte	WAN/HSS NPE – Not user programmable
C800_7000	C800_7FFF	1 Kbyte	Ethernet NPE A – Not user programmable
C800_8000	C800_8FFF	1 Kbyte	Ethernet NPE B – Not user programmable
C800_9000	C800_9FFF	1 Kbyte	Ethernet MAC A (ETH-0)
C800_A000	C800_AFFF	1 Kbyte	Ethernet MAC B (ETH-1)
C800_B000	C800_BFFF	1 Kbyte	USB controller (not available on Pronghorn)
C800_C000	C800_FFFF		Reserved
C801_0000	CBFF_FFFF		Reserved
CC00_0000	CC00_00FF	256 byte	SDRAM configuration registers
CC00_0100	CEFF_FFFF		Reserved
D000_0000	FFFF_FFFF		Reserved

The lowest 256 Mbyte of address space is configurable, based on the value of a configuration register located in the expansion-bus controller. When the configuration register is set to logic 1, the expansion bus occupies the lowest 256 Mbyte of address space. When the configuration register is set to logic 0, the SDRAM occupies the lowest 256 Mbyte of address.

In both cases, the SDRAM occupies the 768 Mbyte immediately following the lowest 256 Mbyte. On reset, the configuration register in the expansion bus is set to logic 1. This setting is required because the dedicated boot memory is flash memory located in the expansion bus.

2.3 SDRAM Memory

The IXP425 network processor supports PC-133-compatible SDRAM for 16-bit-wide devices only. The banks are accessed 32 bits at a time. The Pronghorn supports 32-Mbyte, using two chips in 2 M x 16 x 4 banks configuration.

The SDRAM controller is optimized for handling eight-word bursts from the SDRAM. The SDRAM controller throttles the data throughput by controlling the CKE pin of the SDRAM and Wait signal of internal bus.

Byte-handling is performed only for write operations to the SDRAM by controlling the DQM pins of the SDRAM. All read operations are performed by reading the complete bus width of data.

The SDRAM controller has a policy to keep up to eight pages open simultaneously. If a request is received for an open page, the row access (RAS) address cycle is not performed. If the requested page is not currently open, the SDRAM controller first closes the currently open page in that bank, then opens the new page.

2.4 Expansion Bus

The expansion bus in the IXP425 network processor has 16-bit data and 24-bit address for each of its eight, independent chip selects. This allows an addressing range of 512 bytes to 16 Mbyte and connection of up to eight independent external devices.

2.5 Devices on the Expansion Bus

The chip selects of Pronghorn devices that are connected to the expansion bus are listed in Table 3.

Table 3. Chip Selects For Devices Connected to Expansion Bus

Chip Select	Assignment
CS0	Flash 0
CS1	Flash 0
CS2-CS7	(Not used)

Note: there is only one flash device partitioned onto two chip selects. This is useful when using a 256Mbit flash device.

2.6 Configuration Straps

The expansion bus address lines (EXPB_ADDR[23:0]) are used for configuration strapping options during boot-up or whenever the reset is de-asserted. At the first cycle after the de-assertion of reset, the values on these lines are read (the expansion bus address outputs are switched to inputs) to determine the configuration of the Pronghorn and its plug-in cards.

These values are stored in Configuration Register 0, bit [23:0]. All defined configuration strappings are shown in Table 4.

More information about Configuration Register 0 can be found in the *Intel ® IXP425 Network Processor Based on Intel ® XScale™ Microarchitecture Component Specificatio*n.

Table 4. Pronghorn Configuration Strappings

Bit	Name	Description
23:21	Xscale Clock Set [2:0]	Processor Speed Select 111 = Specified processor speed 23 22 21 = Processor Frequency Core Speed Selected 1 x x 533 MHz = 533 MHz 1 x x 400 MHz = 400 MHz 1 x x 266 MHz = 266 MHz The pull-down resistors will be included in the schematics, allowing test and debug at different speeds, though not assembled on the platform.
20:17	Flash Select	General Flags for BootAddress Select Bit 20 • 0 = Select Flash0 • 1 = Select Flash1 Bits 19:17 – The three most significant address lines on the flash
16:14		Reserved
13:11	Data/Voice	Voice Feature Selection 111 = No voice capability on platform
10:6		Reserved for Pronghorn

5		No connection may be made. Internal only strap.
4	PCI_CLK	Clock speed of the PCI interface 0 = 33 MHz (Pronghorn setting) 1 = 66 MHz
3		No connection may be made. Internal only strap.
2	PCI_ARB	Enables the PCI Arbiter 0 = PCI arbiter disabled 1 = PCI arbiter enabled (Pronghorn setting)
1	PCI_HOST	Configures the IXP425 network processor as PCI Bus Host 0 = IXP425 network processor as non-host 1 = IXP425 network processor as host (Pronghorn setting)
0	8/16 Flash	Specifies the data bus width of the FLASH memory device 0 = 16-bit data bus (Pronghorn setting) 1 = 8-bit data bus

2.7 Boot ROM

The boot ROM of Pronghorn is the Intel StrataFlash ® E28F128J3A-150 16-Mbyte memory connected through the expansion bus. The flash is organized as 16 Mbyte or 8 Mwords (128-Mbit) or 128 128-Kbyte (131,072 Bytes) erase blocks. The E28F128J3A supports the common flash interface (CFI).

For more information about the E28F128J3A Intel StrataFlash ® Memory, see the *3-Volt Intel StrataFlash ® Memory Datasheet*.

Multiple images may be written into the flash. The boot image is chosen by changing the location of the boot address determined by the BSP from bits [20:17] of the processor configuration register 0. These bits are programmed with shorting bars on J12, which strap the expansion bus address bits [20:17] to a logic zero. Following power-up or reset, the logic values on expansion bus address bits [20:17] are transferred to configuration register 0. Bit [20] selects between the two flash devices and bits [19:17] represent the high-order three bits (address line 23, 22 and 21) of the expansion address bus. The process boot code reads the states of the bits and calculates the start address for the boot. With these three bits, each flash can boot from one of eight address locations.

The size of the data transfer (8 bit or 16 bit) is set on the board using the expansion bus address 0 strapping jumper. The EXPB_A0 strap is set to 0 at the de-assertion of reset to select 16-bit data bus. The FLASH_STS pin on the flash is unused on the IXP425 network processor. It will be pulled up through a 4.7-KΩ resistor since it is an open drain output.

2.8 Mini PCI and 802.11 WLAN Interface

The Pronghorn Development Kit comes with an Atheros-based 802.11 a/b/g Mini PCI card installed. There are also two dual-band external antennas installed as well. Other Mini PCI cards and antennas are available.

802.11 a/b/g Mini PCI Specifications	
Standards	IEEE 802.11a
	IEEE 802.11b
	IEEE 802.11g
Bus Type	Mini-PCI REV:1.0
	32-bit Interface
Data Rates With Automatic Fallback	54, 48, 36, 24, 18, 12, 11, 9, 6, 5.5, 2, and 1 Mbps
Security	64-, 128-WEP

	802.1x
	WPA -- Wi-Fi Protected Access
	WPA —PSK (Pre-Shared Key)
	CSMAbCA with ACK
Media Access Control Frequency Range	2.4GHz to 2.497GHz
	5.150GHz to 5.850GHz
	Indoors: Up to 328 feet (100 meters)
Range	Orthogonal Frequency Division Multiplexing (OFDM)
Modulation Technology	Complementary Code Keying (CCK)
	Direct Sequence Spread Spectrum (DSSS)
Transmitter Output Power	17 dBm (typical)
Antenna Connector Type	Dual Hirose U-FL
Receiver Sensitivity	54 Mbps OFDM, 10% PER, -72 dBm)
	48 Mbps OFDM, 10% PER, -75 dBm)
	36 Mbps OFDM, 10% PER, -77 dBm)
	24 Mbps OFDM, 10% PER, -79 dBm)
	18 Mbps OFDM, 10% PER, -82 dBm)
	12 Mbps OFDM, 10% PER, -84 dBm)
	11 Mbps CCK, 8% PER, -82 dBm)
	9 Mbps OFDM, 10% PER, -87 dBm)
	6 Mbps OFDM, 10% PER, -89 dBm)
	5.5 Mbps CCK, 8% PER, -85 dBm)
	2 Mbps QPSK, 8% PER, -86 dBm)
	1 Mbps BPSK, 8% PER, -89 dBm)
Operating Voltage	3.3 VDC ±5%
Operating Temperature	0℃ to 50℃
Humidity	95% maximum (non-condensing)
Dimensions	Type 3B
Weight	70g

The Pronghorn supports two Mini PCI connectors with the PCI interface configured as a PCI host. One Mini PCI slot is used for the 802.11 card. Only 33-MHz PCI bus operations are supported as shipped. A 66MHz option is supported by special request.

The details of the Mini PCI interface include:

- Chip Select — PCI_REQ1 and PCI_GNT1 for slot 1 and PCI_REQ2 and PCI_GNT2 for slot 2
- Interrupts — GPIO 11 and GPIO6, active low, PCI-IRQAn or PCI_IRQBn
- Clock — GPIO 14
- Programmed reset — GPIO 12, active low

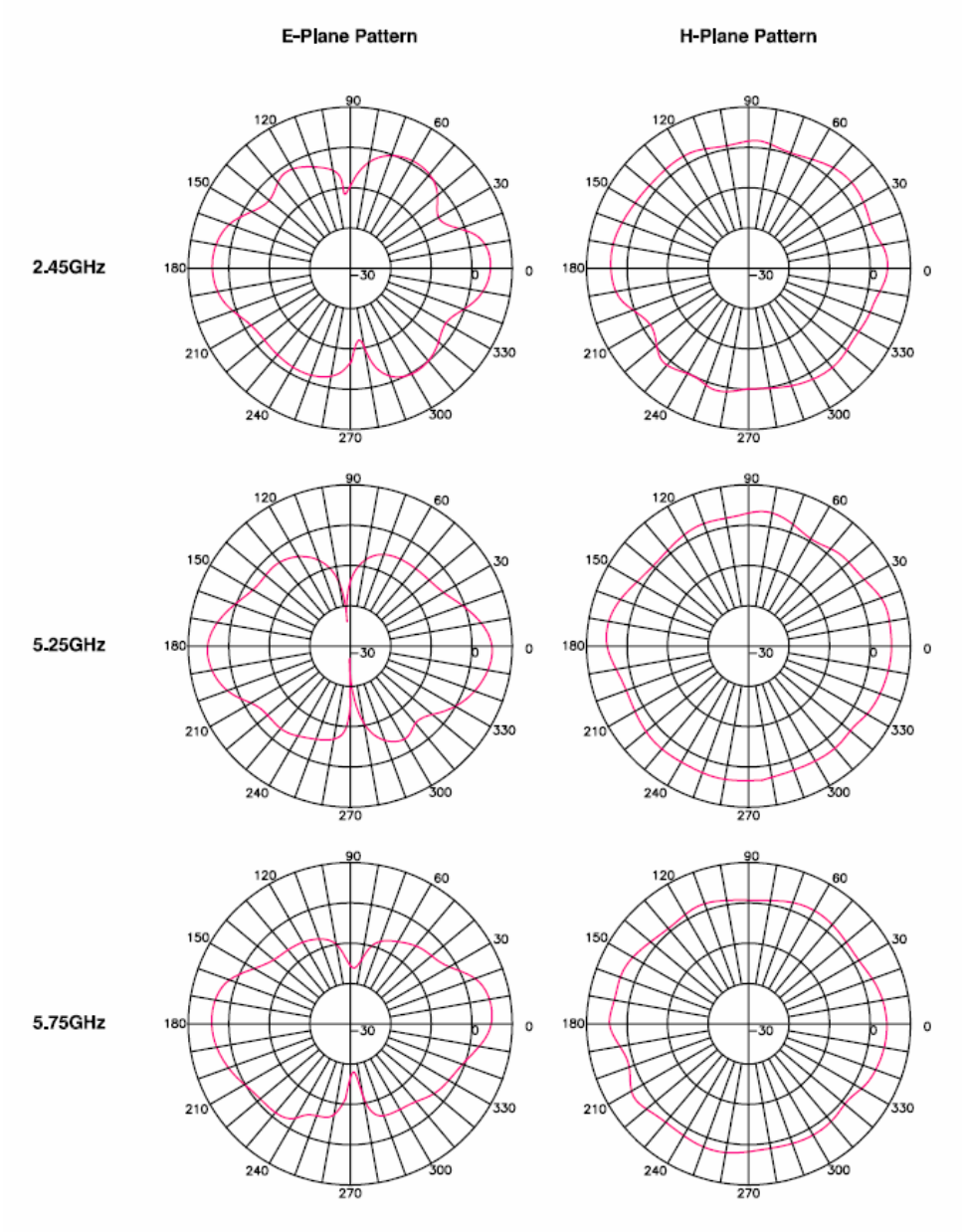
As the IXP425 network processor is the PCI host, reset will be driven to the PCI devices from the system reset circuit.

The PCI_IDSEL pin on the processor is pulled up to 3.3 V. The IDSEL's on the Mini PCI slots are connected to PCI_AD17 and PCI_AD18 respectively, giving each a unique device number on the PCI bus.

2.9 Antennae

Pronghorn has two dipole antennae with the following specifications:

Type	Dipole ½ wave	
Frequency Range	2.4~2.5 GHz 5.15~5.85 GHz	
Impedance	50 ohm nominal	
VSWR		<2.0:1
Gain	2.45 GHz 5.25 GHz 5.75 GHz	4.0 dBi 5.0 dBi 4.5 dBi



2.10 Ethernet Interfaces

- Interface: MDC/MDIO
  - Programmed reset: GPIO 12, active low
- Interface: Ethernet 0 to primary Ethernet port (ETH)
  - Clock: External, 25 MHz
- Interface: Ethernet 1 to secondary Ethernet port (ETH 2)
  - Clock: External, 25 MHz

The IXP425 network processor has two Ethernet 10/100BaseT interfaces, implemented with Ethernet coprocessors built into the NPEs.

The coprocessors provide support for MII and RMII interfaces to the external PHY. They support both full-duplex and half-duplex mode of operation and also contain two 256-byte FIFO: one for transmit data and the other for receive data.

The processor includes a single management data interface — Management Data Input Output (MDIO) — and Management Data Clock (MDC) to program the Ethernet PHYs.

The two Ethernet ports are directly connected to the Ethernet controller via the MII interface as shown in Figure 3.

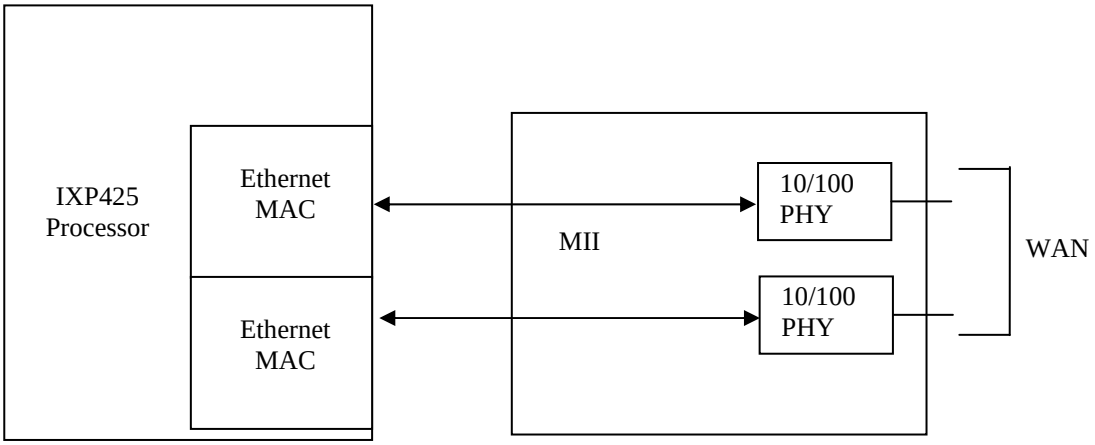


Figure 3. Implementation of Ethernet Ports

2.11 Console Serial Port

The IXP425 network processor provides two dedicated asynchronous, serial, I/O ports (UART0 and UART1). These UARTs are 16550-compliant with flow control and enhanced with larger 64-byte transmit and receive buffers. Only UART1 will be used on the Pronghorn.

The console serial interface is connected to (UART1) Port 1. Port 1 is routed to the 6-pin header (J5). Pin 1 is marked with a ^. A special adapter must be used, along with a straight serial cable to connect to a host PC.

Table 5. Serial Port, 6-Pin Header

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	2	3.3V
3	URT1_RXD	4	URT1_TXD
5	Not Connected	6	Not Connected

2.12 VisionICE/Raven Emulator Interface

The IXP425 network processor may be controlled during debug through a JTAG interface to the processor. The Macraigor * Raven * and Wind River Systems * visionPROBE * / visionICE * systems will plug into the JTAG interface through a 20-pin connector, defined in Table 8.

The Pronghorn reset circuit requires that the JTAG reset be open drain and active low. It is wire ORed with push-button reset and power-on reset to generate a reset to the processor.

Table 6. Emulator Connector

Pin #	Pin Name	Connect To	Pin #	Pin Name	Connect To
1	VTREF	+3.3V	2	VSUPPLY	+3.3V
3	TRST_N	JTG_TRST 10-K Ω pull-down – TRST also generated from reset circuit whenever system reset asserted and from Corelis test equipment	4	GND	GND
5	TDI	JTG_TDI	6	GND	GND
7	TMS	JTG_TMS 10-K Ω pull-up	8	GND	GND
9	TCK	JTG_TCK 10-K Ω pull-up	10	GND	GND
11	RTCK	GND	12	GND	GND
13	TDO	JTG_TDO	14	GND	GND
15	SRST_N	Reset circuitry	16	GND	GND
17	DBGRQ	Not Connected	18	GND	GND
19	DGBACK	Not Connected	20	GND	GND

2.13 Indicator LED's

The platform will have LEDs (light-emitting diodes) indicating the activities shown in Table 10.
Please note that the Wireless, Ethernet, and Ethernet 2 LED's can be configured under software control and the actions specified are merely guidelines.

Table 7. Pronghorn LED's

LED	Color	Description
Power	Green	Power to the system is on
Wireless	Off	Wireless disabled
	Green	Wireless enabled
	Blinking	Data transfer
Ethernet	Off	No connection found
	Green	10/100-Mbps link
	Blinking	Data transfer
	Off	No connection found

Ethernet 2	Green	10/100-Mbps link
	Blinking	Data transfer

2.14 Platform Reset Circuitry

The board generates a power-on reset upon the required voltages reaching valid levels. Power-on reset signal resets all the circuitry.

A reset switch provided on the board also resets the entire board.

Additionally GPIO 12 (as an active-low signal) is used to reset all the peripherals on the platform.

2.15 Power Supplies, Regulators

The input power to the platform is through an external AC/DC converter power supply at +5 V DC, 2.25 A nominal.

There are three power regulators on the platform; two regulators (3.3V and 1.3V) when operating from an AC/DC converter, and a third that generates +5V when operating from PoE. These are rated at:

- 5.0 V at 2.25 A
- 3.3 V at 2.0 A
- 1.3 V at 2.0 A

Maximum component current draw (for reference only) of the functional blocks are shown in the table below.

Table 8. Maximum current draw of Functional Blocks

Voltage	Device	Current Requirement (mA)
5.0V	Mini PCI (x2)	500 (x2)
3.3V	IXP425 processor	455
	LED's	25
	SDRAM	285
	SDRAM	285
	FLASH	80
	Mini PCI (x2)	606 (x2)
1.3V	IXP425 processor	1000

2.16 Mechanical

The Pronghorn enclosures is made of ABS plastic and measures approximately 5" x 7 ½" x 1 ¾". It weighs less than 16 ounces. The Pronghorn printed circuit board (PCB) is 6 ½" by 4 ¾" with notched cutouts on the four corners.

Pronghorn Enclosure Specifications
Dimensions: 5 x 7 x 1.75 inches
Weight: Less than 16 ounces
Surface: Textured finish
Material: Flame retardant ABS plastic
Flame Rating: UL's best flame rating of 94-5VA
Closure: Screw-on
Case: Textured
Base: Recessed area for labeling I.D.
End Panel: Removable end panel is easily modified for addition or removal of connectors

For volume production, the enclosure is available in various colors. Custom printing is also available for production orders.

3 Installing and Configuring the Hardware

3.1 Kit Contents and Inspection

Please inspect the contents of the Pronghorn 802.11 Application Platform kit and verify that you have following:

- Pronghorn 802.11 Application Platform (1)
- External power supply (1)
- Cat5 Ethernet cable (2)
- RS232 cable (1)
- Custom serial adapter/cable (1)
- Documentation and software CD
- Instant802 SMAP Documentation CD

Inspect the Pronghorn for obvious damage. If your kit has missing or damaged items, please contact ADI Engineering, Inc. to resolve the discrepancy.

4 RedBoot Operation

Follow the steps below to setup Pronghorn for RedBoot operation:

1. Disconnect power from Pronghorn
2. Unscrew the four (4) screws on the bottom of the case and carefully remove the top-cover.
3. Connect the serial adapter to J5
4. Connect a serial cable from Pronghorn to a console configured for 115200-8-N-1-N.
5. Connect a CAT5 Ethernet cable from the ETH0 (J6, the RJ-45 closest to the edge) to your network
6. Connect the power module to Pronghorn
7. Power Pronghorn and look for activity on the console.

The RedBoot Boot Monitor included in the Pronghorn is primarily used as a basis for further software development. RedBoot communicates to a host computer through the Pronghorn serial port. The host computer must use a terminal emulator like Window's **HyperTerminal** or Linux's **minicom**. The following table specifies the default parameters for correct serial port operation.

Parameter	Value
Bits per second	115200
Data bits	8
Parity	None
Stop bits	1
Flow control	None

4.1 Power Up

When the Pronghorn is powered on, RedBoot starts and the following is displayed:

```
+Ethernet eth0: MAC address 00:00:84:60:50:02
IP: 192.0.0.106/255.255.255.0, Gateway: 0.0.0.0
Default server: 192.0.0.64, DNS server IP: 0.0.0.0

RedBoot(tm) bootstrap and debug environment [ROM]
Red Hat certified release, version 1.92 - built 17:40:17, Aug 20
2004

Platform: ADI Pronghorn WiFi Router (XScale)
Copyright (C) 2000, 2001, 2002, Red Hat, Inc.

RAM: 0x00000000-0x04000000, 0x0001f960-0x03fd1000 available
FLASH: 0x50000000 - 0x51000000, 128 blocks of 0x00020000 bytes
each.
RedBoot>
```

The MAC and IP addresses in the following banner are those of the NPE ETH0 port. (Actually, Redboot will use eth0 to refer to any port that is providing the Ethernet connection.) The IP and Default Server addresses can be configured as needed to be compatible with any network through the `fconfig` command.

NOTE: If no Ethernet connection is configured or present, the board may take about 45 seconds to get to a Redboot prompt.

4.2 RedBoot Commands

This section provides a brief summary of RedBoot commands and is intended only as a quick reference. For a thorough overview of RedBoot functionality please refer to the RedBoot User's Guide on the Pronghorn CDRom.

RedBoot provides three basic classes of commands:

- Program loading and execution
- Flash image and configuration management
- Miscellaneous commands

The basic format for commands is:

RedBoot> COMMAND [-S] [-s val] operand

Commands may require additional information beyond the basic command name. In most cases this additional information is optional, with suitable default values provided if they are not present. The type of information required affects how it is specified.

1. **[-S]** indicates an optional switch. If this switch is present, then some particular action will take place. For example in the command

   RedBoot> fis init –f

   the -f switch indicates to perform a full file system initialization.

2. **[-s val]** indicates an optional switch that requires an associated value. For example the command:

   RedBoot> load -b 0x20000 data_file

   specifies downloading a file (via TFTP) into memory, relocating it to location 0x20000.

3. **operand** This format is used in a case where a command has one operand which must always be present (no -s is required since it is always implied). For example the command

   RedBoot> go 0x20000

   specifies executing the code starting at location 0x20000.

The list of available commands, and their syntax, can be obtained by typing help at the command line:

```
RedBoot> help
Manage aliases kept in FLASH memory
   alias name [value]
Set/Query the system console baud rate
   baudrate [-b <rate>]
Manage machine caches
   cache [ON | OFF]
Display/switch console channel
   channel [-1|<channel number>]
Compute a 32bit checksum [POSIX algorithm] for a range of memory
   cksum -b <location> -l <length>
Display (hex dump) a range of memory
   dump -b <location> [-l <length>] [-s] [-1|2|4]
Execute an image - with MMU off
```

```
   exec [-w timeout] [-b <load addr> [-l <length>]]
        [-r <ramdisk addr> [-s <ramdisk length>]]
        [-c "kernel command line"] [<entry_point>]
Manage FLASH images
   fis {cmds}
Manage configuration kept in FLASH memory
   fconfig [-i] [-l] [-n] [-f] [-d] | [-d] nickname [value]
Execute code at a location
   go [-w <timeout>] [entry]
Help about help?
   help [<topic>]
Set/change IP addresses
   ip_address [-l <local_ip_address>] [-h <server_address>]
Load a file
   load [-r] [-v] [-d] [-h <host>] [-m <varies>] [-c
<channel_number>]
        [-b <base_address>] <file_name>
Compare two blocks of memory
   mcmp -s <location> -d <location> -l <length> [-1|-2|-4]
Copy memory
   mcopy -s <location> -d <location> -l <length> [-1|-2|-4]
Compute a 128bit checksum [RSA Data Security, Inc. MD5 Message-
Digest Algorithm] for a range of memory.
   md5sum -b <location> -l <length>
Set/Fill memory location(s)
   mem [-b <location>] [-l <length>] [-1|2|4] [-w] <data>
Fill a block of memory with a pattern
   mfill -b <location> -l <length> -p <pattern> [-1|-2|-4]
Scans PCI devices and reports findings
   pciscan
Converts a virtual to a physical address
   physaddr <virtual address>
Network connectivity test
   ping [-v] [-n <count>] [-l <length>] [-t <timeout>]
      [-r <rate>] [-i <IP_addr>] -h <IP_addr>
Print information about the current settings within the main
processor
   processor
Reset the system
   reset
Display RedBoot version information
   version
Converts a physical to a virtual address
   virtaddr <physical address>
Display (hex dump) a range of memory
   x -b <location> [-l <length>] [-s] [-1|2|4]
RedBoot>
```

Commands can be abbreviated to their shortest unique string. Thus in the list above, d,du,dum and dump are all valid for the dump command. The fconfig command can be abbreviated fc, but f would be ambiguous with fis.

4.3 Configure Pronghorn

Use the command **`fconfig -i`** to set the configuration parameters. Use **`fconfig -l`** to list the configuration parameters, example below:

```
RedBoot> fconfig -l
Run script at boot: false
Use BOOTP for network configuration: false
Gateway IP address: 0.0.0.0
Local IP address: 192.0.0.106
Local IP address mask: 0.0.0.0
Default server IP address: 192.0.0.64
Console baud rate: 115200
DNS server IP address: 0.0.0.0
GDB connection port: 9000
Force console for special debug messages: false
Network debug at boot time: false
Default network device: npe_eth0
Network hardware address [MAC] for NPE eth0:
0x00:0x00:0x84:0x60:0x50:0x02
Network hardware address [MAC] for NPE eth1:
0x00:0x00:0x84:0x88:0x50:0x02
RedBoot>
```

The above represents the default RedBoot parameter settings for Pronghorn. Note that static local and server IP addresses are used. If your Pronghorn resides on network that includes a DHCP server, change the **`"Use BOOTP for network configuration:"`** parameter to "**true"**. Entering the <**`fconfig`**> command without any switches will enable you to change parameters.

```
RedBoot> fconfig
```

RedBoot will display the first parameter and its value. If you are satisfied with the current value, hit **`[enter]`**. Otherwise, type the desired value and then hit **`[enter]`**. When you have gone through the entire parameter list, a final confirmation is required before the modified configuration is written to flash. Upon completion, issue the <**`fconfig –l`**> command again to verify that your changes have been made. Then reboot the Pronghorn to have the new boot parameters take effect.